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RAPID COMMUNICATION

Nano-crystallized titanium oxide resistive memory with uniform switching and long endurance

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Abstract We report a novel resistive random access memory using tri-layer dielectrics of GeO_x/nano-crystal TiO_2/TaON and low cost top Ni and bottom TaN electrodes. Excellent device performance of ultra-low 720 fJ switching energy, tight distributions of set/reset currents, and exceptionally long endurance of 5×10^9 cycles were achieved simultaneously. Such excellent endurance may create new applications such as those used for Data Centers that are ascribed to the higher-κ nano-crystal TiO_2, hopping pass via grain boundaries, and fast switching speed of 100 ns to improve the dielectric fatigue during endurance stress.

1 Introduction

According to *International Technology Roadmap for Semiconductors* (*ITRS*) [1], the Flash non-volatile memory (NVM) continues to scale down into sub-20 nm, by replacing the current poly-Si floating-gate (FG) with SiN charge-trapping (CT) structure [2–4]. However, the degraded endurance from 10^5 to 10^4 program/erase cycles is the fundamental physics limitation due to the smaller number of charges stored in the sub-20 nm cell size. Such degraded endurance is unsuitable for high-end products; therefore, new NVM devices should be developed. To address this concern, non-charge-based resistive random access memory (RRAM) has attracted considerable attention [5–13]. However, the high set/reset currents, high forming power, poor endurance, and required extra large-size transistor for current compliance are the difficult challenges for RRAM. However, the set/reset cycle times of 10^6 must still be improved to realize the ideal green NVM with low switching energy, long endurance, and high switching speed. In this letter, we report a novel high endurance and ultra-low switching power RRAM device, where only 4 μW setting power, ultra-low reset power of 200 nW, large resistance window >50X, favorable switching uniformity, and excellent cycling endurance (up to 5×10^9 cycles) were achieved simultaneously. Such high performances were reached in designing the Ni/GeO_x/nano-crystal (nc) TiO_2/TaON/TaN RRAM device, where the excellent endurance is 4 to 5 orders of magnitude larger than the highest quality Flash memory [1–4]. The excellent endurance is related to hopping conduction via grain boundaries of nc-TiO_2, fast switching speed of 100 ns, and the using high-κ dielectrics to lessen the dielectric fatigue during stress. The exceptionally long endurance and low switching energy RRAM not only satisfy the portable Solid-State Drive (SSD) in computers, but may also create new applications such as those used for Data Center, to replace the high power consumption of hard discs.

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2 Experiments

The RRAM devices were integrated into a VLSI backend for an embedded memory application. First, a 200-nm-thick backend SiO_2 was formed on the Si substrates. Then 100 nm TaN was deposited by sputtering. After patterning the bottom TaN electrode, the 24-nm-thick TaON film was deposited *by sputtering* and followed by *oxygen annealing at*

400 °C *for* 10 min. Subsequently, the 26-nm-thick TiO_2 film was deposited *by sputtering in a gas mixture with* 5 % O_2 *in Ar ambient on the* TaON/TaN. *Then the* TiO_2 *film was annealed at* 400 °C *for* 5 min *to form crystallized* TiO_2, where the crystallinity of TiO_2 [14] was measured by transmission electron microscopy (TEM) and a fast Fourier transition (FFT) technique. The amorphous TiO_2 (a-TiO_2) control sample was also fabricated for performance comparison. Following that, a 6-nm-thick GeO_x was deposited to form the tri-layer dielectrics of the GeO_x/TiO_2/TaON. Finally, a 50-nm-thick Ni was deposited and patterned to form the top electrode *by a metal mask with an area of* 11300 μm^2. The fabricated devices were characterized by capacitance-voltage (C-V), current-voltage (I-V), switching speed, and endurance measurements using an Agilent 4284 LCR meter, 4156 semiconductor parameter analyzer, and 81110 pulse generator, respectively. *The bottom TaN of RRAM was grounded for related electrical measurement.*

3 Results and discussion

Figure 1(a) shows the swept I-V curves of the Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM. Favorable resistive switching characteristics were measured, where a large resistance window >100 at 0.5 V was obtained. In addition to the forming-free and self-compliance switching, this RRAM can be set to a low resistance state (LRS) at a low power of 4 μW (1 μA at 4 V) and reset to a high resistance state (HRS) at an extremely low power of 200 nW (−40 nA at −5 V). The low LRS current is attributed to the large internal resistance by hopping conduction [15], which also results in the measured forming-free and self-compliance operation. The RRAM with asymmetric I-V and exceptionally small reset current are similar to the asymmetric I-V and very low revise leakage current in a Schottky diode. The asymmetric switching I-V curves are ascribed to the different work functions of the bottom TaN (4.6 eV) and top Ni electrodes (5.1 eV) [16]. The top GeO_x layer is vital in forming the resistive switching behavior, as the control devices without GeO_x have no resistance hysteresis loops (not shown). To explore such low switching currents, the current conduction mechanism was analyzed. Figure 1(b) shows the measured and simulated I-V characteristics at HRS and LRS, respectively. The small HRS current is due to the Frenkel–Poole emission via the top Ni. The current at LRS is governed by a space-charge-limited current (SCLC) via dielectric defects, for electrons injected from the bottom TaN. Such resistive switching with negative TC has been previously attributed to the hopping conduction via charged oxygen and nitrogen vacancies [12, 13], and is further verified by the hysteresis loop found in C-V measurements shown in Fig. 1(c). Here the voltage change for set and reset operation is 5 V and −6 V, respectively. It is important to notice that the C-V hysteresis loop represents the change of charges by $\Delta Q = \Delta C \times V$. However, the C-V hysteresis curve in this RRAM device is quite different from the C-V hysteresis loop found in Flash

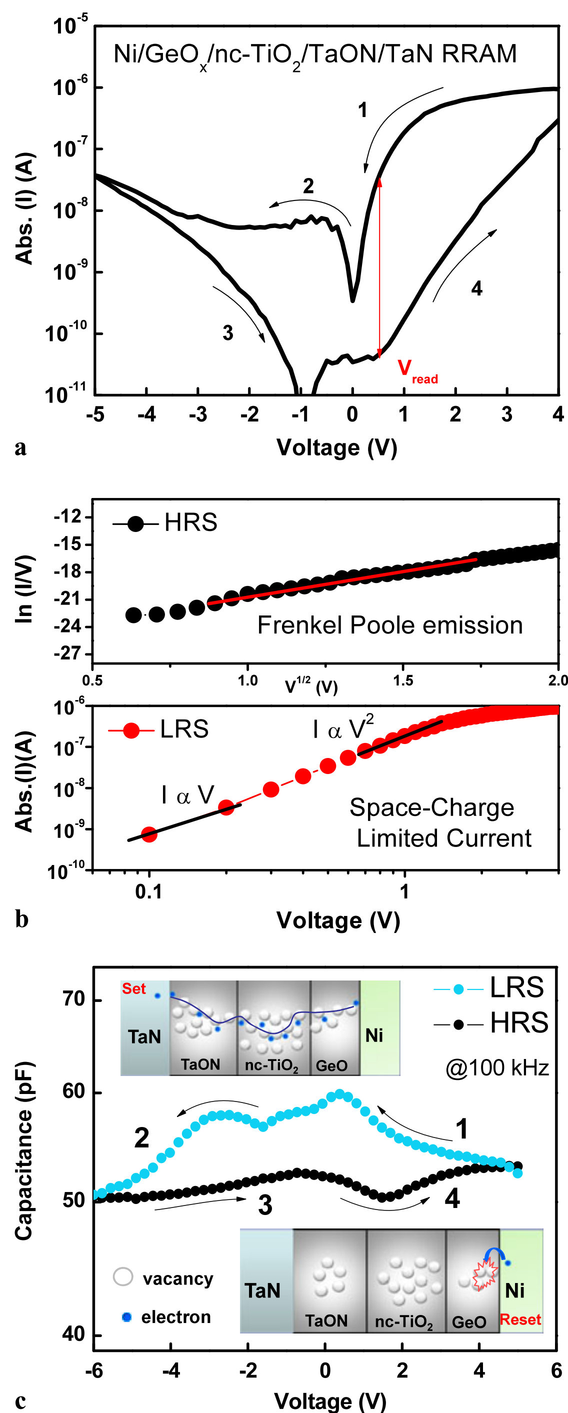


Fig. 1 (**a**) Swept I-V curve, (**b**) I-V at HRS and LRS by fitting with Frenkel–Poole and SCLC conduction mechanisms, respectively, and (**c**) 100 kHz C-V curves of Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM devices. The inset figures are the schematic energy band diagram with charged oxygen vacancies under set and reset conditions

memory [2–4]. This is due to the different MIM and MIS structure used for RRAM and Flash, respectively. During the set with a positive voltage, the charged oxygen vacancies can be formed by injected electrons from the bottom TaN electrode, resulting in a higher capacitance, shown in the inserts of Fig. 1(c). During the reset, the injected electrons from the top Ni electrode can disrupt the weakly linked hopping conduction pass by annihilating the charged vacancies at ultra-low energy:

$$V^{2+}_{\mathrm{Ge\text{–}O}_x} + 2e^- + \mathrm{Ge\text{–}O}_x \rightarrow \mathrm{Ge\text{–}O}_x^*. \quad (1)$$

Here, the $V^{2+}_{\mathrm{Ge\text{–}O}_x}$ is the oxygen vacancy in GeO_x for the hopping conduction. The change of vacancies charges, shown in the area of C-V hysteresis loop, in turn decreases the capacitance density at HRS state.

The nc-TiO_2 performs a vital function in attaining low switching power in RRAM. Figures 2(a), 2(b), and 2(c) show the switching I-V curves, 60-ms pulsed switching stress, and cross-sectional TEM of the Ni/GeO_x/a-TiO_2/TaON/TaN RRAM devices, respectively, where different nc-TiO_2 (anatase phase) or a-TiO_2 in the RRAM devices were used for comparison. As shown in Fig. 2(c), the anatase TiO_2 with native shallow-level defects may contribute superior electron transport for fast resistive switching. Although similar I-V switching behavior can be observed, the control device with a-TiO_2 requires larger set and reset voltages of 6 V and −8 V, respectively. Furthermore, significantly higher switching currents for the set (18 μA) and reset (1.2 μA) were found in the RRAM device with a-TiO_2 layer, as opposed to those with nc-TiO_2. To investigate further such large differences in nc-TiO_2 and a-TiO_2 RRAM, the devices were under 60 ms set and 60 ms reset stress. Highly stable switching cycles were discovered in the RRAM device with an nc-TiO_2 layer. By sharp contrast, the control device with a-TiO_2 yields a small initial HRS/LRS ratio $<$10X at a read voltage of 1 V, where the HRS/LRS memory window shrinks with increasing set/reset cycles. The decreased LRS current after continuous set/reset cycling stress may be related to the redistribution of charged oxygen and nitrogen vacancies [13] under a continuous switching electric field. From the cross-sectional TEM images of the Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM, a small size of 3–9 nm nc-TiO_2 can be clearly observed in the enlarged TEM picture. The nc-TiO_2 was confirmed by FFT patterns that further forms the higher dielectric constant (κ) anatase phase structure from X-Ray Diffraction (XRD) measurements. Therefore, the lower switching power and more favorable long-pulsed switching endurance should be related to the existing grain boundaries in nc-TiO_2. Research has shown that the grain boundaries exhibit an exceptionally high density of dangling bands; this in turn allows the hopping conduction pass to form via grain boundaries at a lower set power. By contrast,

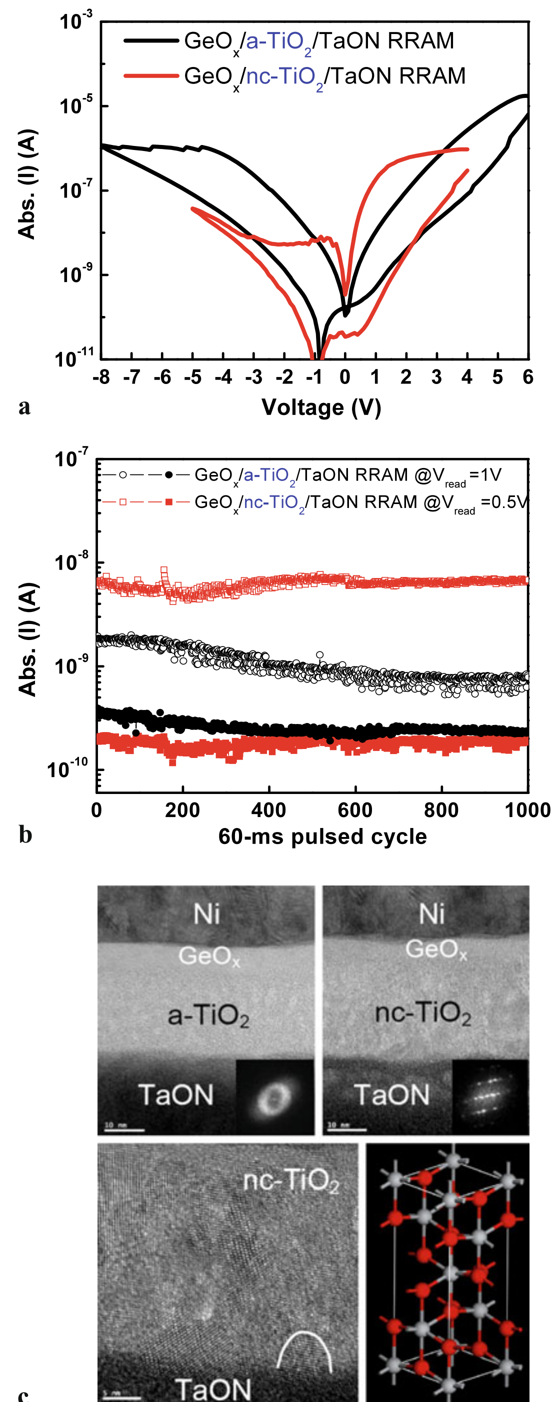
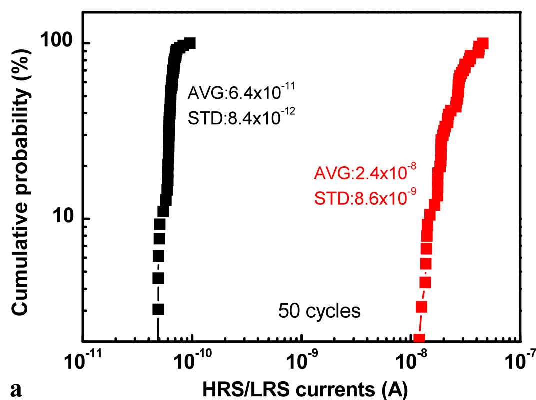


Fig. 2 (**a**) Swept I-V curves, (**b**) resistive switching behaviors under 60 ms set/reset stress cycles and (**c**) cross-sectional TEM images of Ni/GeO_x/TiO_2/TaON/TaN RRAM with nc-TiO_2 (anatase structure) or control a-TiO_2 layer

a high set power is required to form defects for hopping conduction in the densified amorphous material.

The distribution of resistance states is a critical concern for RRAM. Figure 3(a) shows the measured current distributions of Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM,



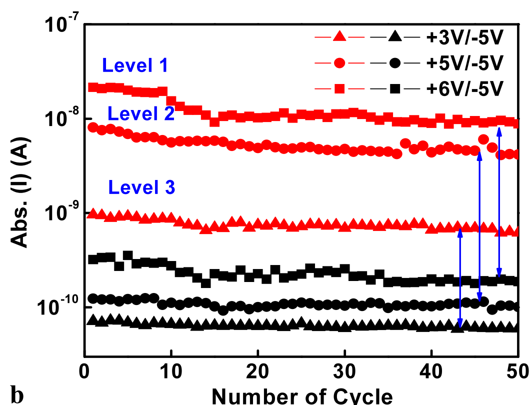
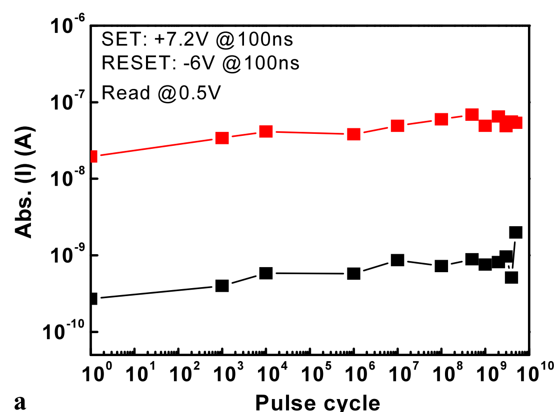


Fig. 3 (**a**) Current distributions and (**b**) MLC operation of Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM



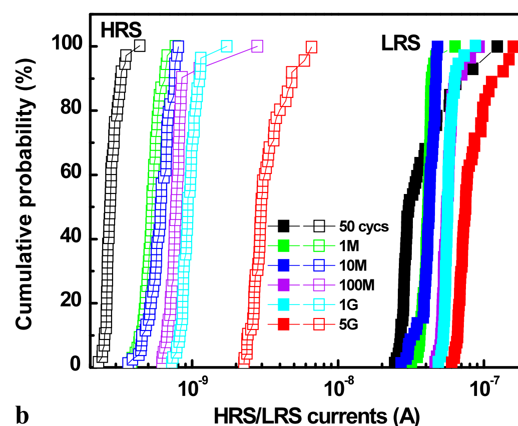


Fig. 4 (**a**) 100-ns-pulsed set/reset endurance characteristics and (**b**) current distribution during cycling endurance test of Ni/GeO_x/nc-TiO_2/TaON/TaN RRAM

where tight current distribution for both LRS and HRS was achieved. The excellent switching uniformity is linked to the low power operation with low set/reset currents and self-compliance set/reset operation, which is significantly more favorable than conventional RRAM using metallic filament conduction. As seen in Fig. 3(b), the RRAM is also capable for multi-level cell (MLC) storage. The MLC function explains that HRS current dominated by Frenkel–Poole emission has various trap levels, which can be set and reset using appropriate bias conditions for mass storage applications.

Endurance is a severe limiting factor for conventional metallic filament RRAM. Figure 4(a) shows the measured endurance characteristics under an over-stressed 7.2 V set pulse and −6 V reset pulse at switching speed of 100 ns. The endurance to 5×10^9 cycles for fast 100 ns pulse was obtained, which is 4 to 6 orders of magnitude higher than the existing Flash memory at an ultra-low 720 fJ switching energy. Excellent uniformity $\geq 10^9$ cycles are also obtained at 100 ns switching that is a strong merit of this device. Such excellent endurance is ascribed to the fast switching speed, low switching power, easy hopping via grain boundaries, and higher-κ nc-TiO_2 ($\kappa > 40$) to a lower stress electrical field.

Figure 4(b) shows HRS/LRS currents distribution during long endurance cycling. The current distribution is not degraded during the endurance cycles of $<10^9$ cycles, except for slight variation on HRS/LRS distributions. However, the continued cycling stress results in degraded switching uniformity and small resistance window at the end of 5×10^9 cycles, indicating that increased conductive trap centers in RRAM deteriorate trap dependence of Frenkel–Poole HRS and SCLC LRS currents.

4 Conclusion

We demonstrate an ultra-low switching energy RRAM with self-compliance operation, large resistance window, favorable switching uniformity, and excellent endurance cycles of 5×10^9. The excellent endurance is attributed to the combined contribution of low switching energy, easy hopping via grain boundaries and a lower stress electric field in higher-κ anatase TiO_2, lessening the dielectric fatigue under continuous set/reset cycling stress.

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