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Enhanced active feedback technique with dynamic compensation for low-dropout voltage regulator

Chia-Min Chen · Chung-Chih Hung

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Abstract This paper presents a novel frequency compensation technique for a low-dropout (LDO) voltage regulator. Enhanced active feedback frequency compensation is employed to improve the frequency response. The proposed LDO is capable of providing high stability for current loads up to 150 mA with or without loading capacitors. The proposed LDO voltage regulator provides a loop bandwidth of 7.8 MHz under light loads and 6.5 MHz under heavy loads. The maximum undershoot and overshoot are 59 and 90 mV, respectively, for changes in load current within a 200-ns edge time, while the compensation capacitors only require a total value of 7 pF. This enables easy integration of the compensation capacitors within the LDO chip. The proposed LDO regulator was designed using TSMC 0.35-μm CMOS technology. With an active area of 0.14 mm^2 (including feedback resistors), the quiescent current is only 40 μA. The input voltage ranges from 1.73 to 5 V for a loading current of 150 mA and an output voltage of 1.5 V. The main advantage of this approach is the stability of the LDO circuit when external load capacitors are connected, or even without load capacitors.

Keywords Low dropout (LDO) voltage regulator · Frequency compensation · Loop stability · Transient response · Output ripple noise · Power management

C.-M. Chen · C.-C. Hung (✉)
Analog Integrated Circuit Laboratory, Department of Electrical Engineering, National Chiao Tung University, Hsinchu, Taiwan
e-mail: cchung@mail.nctu.edu.tw

C.-M. Chen
e-mail: jeremy.cm97g@g2.nctu.edu.tw

1 Introduction

Portable devices require an efficient power management system to extend battery life. These devices usually employ multiple on-chip voltage levels, which has led to the widespread adoption of low dropout (LDO) voltage regulators for electronic devices, such as MP3 players, cellular phones, and digital cameras [1, 2]. LDO voltage regulators result in a small voltage drop across the power transistor and provide a well regulated low-noise voltage. These are particularly suitable for applications such as RF IC and audio IC, which require low noise [3, 4]. Another advantage of linear regulators is the low standby current, due to the absence of switching. In portable devices, a crucial design consideration is reducing quiescent current to maximize the lifespan of the battery [5, 6, 7].

For different applications, LDO regulators are able to support load current capacity ranging from several hundred mA to several A. In the design of SoC solutions, a higher output voltage (e.g., 3.3 V) is usually used for I/O ports, and a lower voltage (e.g., 1.5 V) is used for digital cores, as shown in Fig. 1 [8, 9, 10, 11, 12].

Recently, an increasing number of designs have focused on low supply voltage and low power consumption. A lower supply voltage is required to decrease power consumption and extend battery life in portable electronic devices. Conventional LDO error amplifiers must be designed to provide high gain for precision output voltage and good regulation. A cascode architecture precludes the implementation of the amplifier under low supply voltage; therefore, amplifiers with multiple stages are also usually required [13]. However, multiple amplification stages increases the number of poles, which reduces the phase margin, resulting in stability problems. Moreover, because the transconductance and resistance of the output stage of

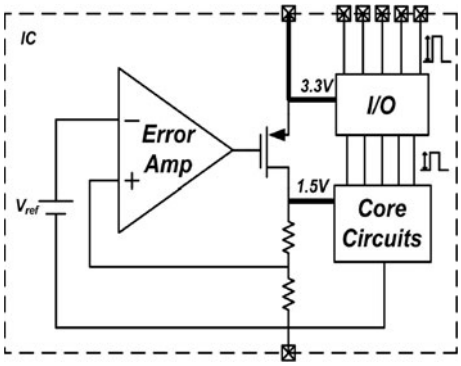

Fig. 1 Application of voltage step-down on chip

the LDO regulator vary according to load conditions, the phase margin must be designed high enough to maintain stability. Thus, this paper proposes a new compensation topology capable of overcoming these drawbacks. The proposed circuit provides zeros to maintain appropriate phase margins under various load conditions. This enables us to maintain the stability using the proposed compensation technique, regardless of whether the LDO regulator is capacitorless or has C_{out} connected to the output, where [8, 9, 10, 11, 12] are only suitable for the SoC applications without off-chip capacitor, not suitable for the applications with large load capacitance. This paper discusses not only the capacitorless case but also the condition with external load capacitor. All circuit analyses and measurements have covered the both conditions. The proposed LDO regulator with enhanced active feedback technique is capable of providing load current up to 150 mA.

The proposed LDO regulator with a new compensation topology maintains high stability even without external load capacitors and features fast transient response, enabling it to reduce undershoot and overshoot of output voltage. Section II provides a brief review on the architecture typically used in linear regulators as well as a discussion on stability. Operating principles, compensation methods, and details regarding the implementation of the circuits are discussed in Section III. Measurement results are provided in Section IV, followed by the conclusion in Section V.

2 Conventional topology of linear regulators

2.1 Basic architecture

An LDO regulator usually comprises a pass element (power transistor), an error amplifier, a driver, a voltage reference, and a resistive feedback network, as shown in Fig. 2. The topology of an LDO is a closed loop. Series-shunt negative feedback is used to dynamically control the pass element, usually a power PMOS transistor. Because the power PMOS must provide a large transconductance and large load current, it is a large element on the order of ten thousand μm. Unfortunately, the gate capacitance of the power PMOS contributes a parasitic pole at low frequencies, thereby degrading the stability of the system. Because the external load capacitor is also very large, it contributes a dominant pole. Three low-frequency poles at the output of the pass element, the driver, and the error amplifier make the structure intrinsically unstable. Nonetheless, with the series connection of the load capacitor and its equivalent series resistance (ESR), it generates a zero, which provides the required stability, as shown by the solid line in Fig. 3. If the loop gain is too high (the dashed line in Fig. 3), and P_{o1} is located before the unity-gain frequency,

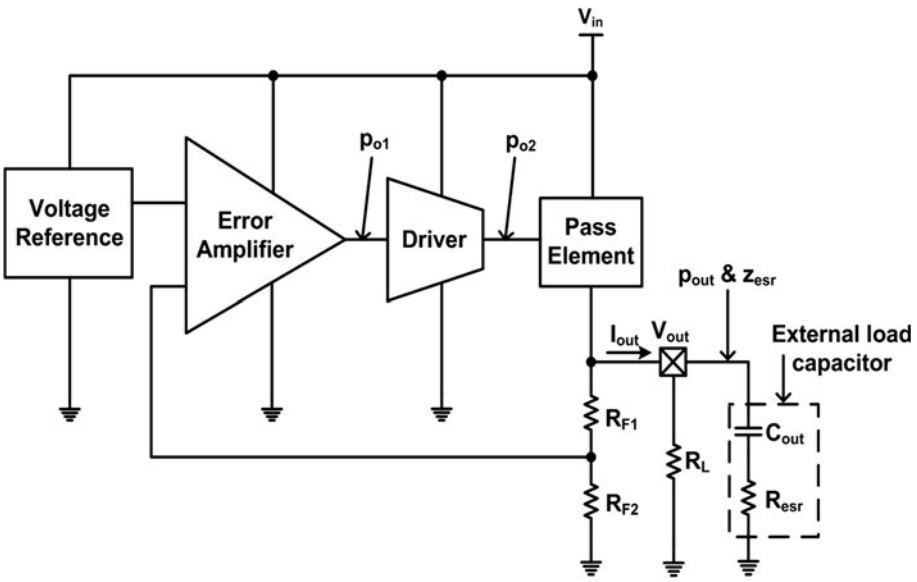

Fig. 2 Topology of conventional LDO regulator

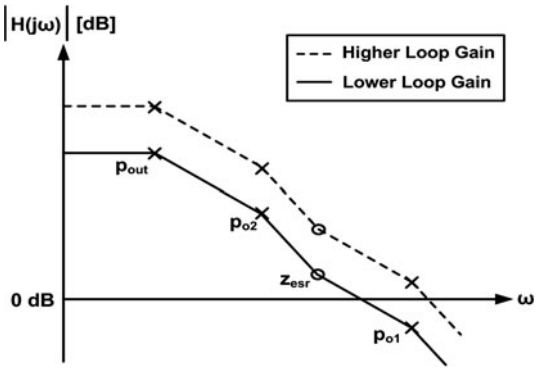

Fig. 3 Frequency response of conventional LDO regulator

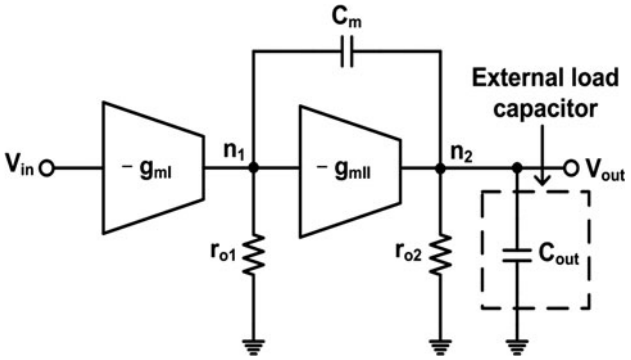

Fig. 4 Two-stage Miller-compensated LDO regulator

an even larger load capacitance is required to maintain stability. This compensation method usually results in a narrow bandwidth [14, 15].

The LDO regulator operates as a closed loop system, which requires compensation to ensure stability under all operating conditions. The fundamental requirements for stability are: (1) the zero must be located below the unity gain frequency of the loop; and (2) all high-frequency poles must be at least three times higher than the unity gain frequency [16]. However, the ESR values differ according to the material used in the load capacitors making it very difficult to accurately control the value of the ESR.

2.2 Existing techniques

One popular compensation method is the Miller compensation technique, as presented in Fig. 4 [17]. This technique involves connecting a capacitor between the output and input of the second stage g_{mII}. The poles of the two-stage amplifier are split, one toward low frequency and the other toward high frequency. In this manner, the dominant pole is located at the output node of the first stage. The dominant low-frequency pole, P_{n1}, is located at node n_1 and is given by

$$P_{n1} \approx \frac{1}{r_{o1}(A_2 C_m)} = \frac{1}{r_{o1}(g_{mII} r_{o2} C_m)} \quad (1)$$

where A_2 refers to the gain of the second stage. At high frequencies, the compensation capacitor C_m shunts the output to node n_1, converting the input transistor of the second stage into a diode connected device. This moves the output pole toward higher frequencies

$$P_{n2} \approx \frac{g_{mII}}{C_{out}} \quad (2)$$

A right-half plane zero also results from the topology described by ($Z_{RHP} = g_{mII}/C_m$). This zero is the result of capacitor C_m providing a noninverting feedforward path, which degrades the phase margin. Variations in load cause very wide variations in g_{mII}, and thus in the high frequency pole (P_{n2}). Consequently, the Miller capacitor must be very large to keep the poles separated, which results in a very large chip area. Other compensation techniques providing amplification greater than that from the Miller effect are capable of improving the performance and reducing the area significantly [18, 19, 20].

3 Proposed LDO regulator

3.1 Architecture

Figure 5 shows the block diagram of the proposed LDO regulator. The architecture of the proposed error amplifier is basically a two stage gain amplifier driving the power transistor. Thus, this LDO regulator can be viewed as a three stage amplifier driving a capacitive load with a parallel resistive load. The first stage is designed as a high gain error amplifier using a folded cascode topology to enhance the dynamic range of the input and the output impedance for higher gain. The first stage provides a gain of approximately 60 dB. An enhanced active feedback (EAF) block comprises g_{mk1}, g_{mk2}, C_k, R_k. This block utilizes the compensation capacitor C_k by multiplying the gain factors of two stages (g_{mII}, g_{mk1}) to form a low-frequency pole (dominant pole for $C_{out} = 0$). Compared with traditional Miller compensation, EAF compensation appears to have one more gain stage factor, enabling the compensated capacitance C_k to have a much smaller value. This block also generates a zero Z_1 to cancel the non-dominant pole.

The second stage, which must be able to turn the power transistor (power PMOS MPO) on and turn off quickly, provides high signal swing and 25 dB gain. The bias current of the second stage is proportional to the slew rate, while the charge time of the power transistor gate is inversely

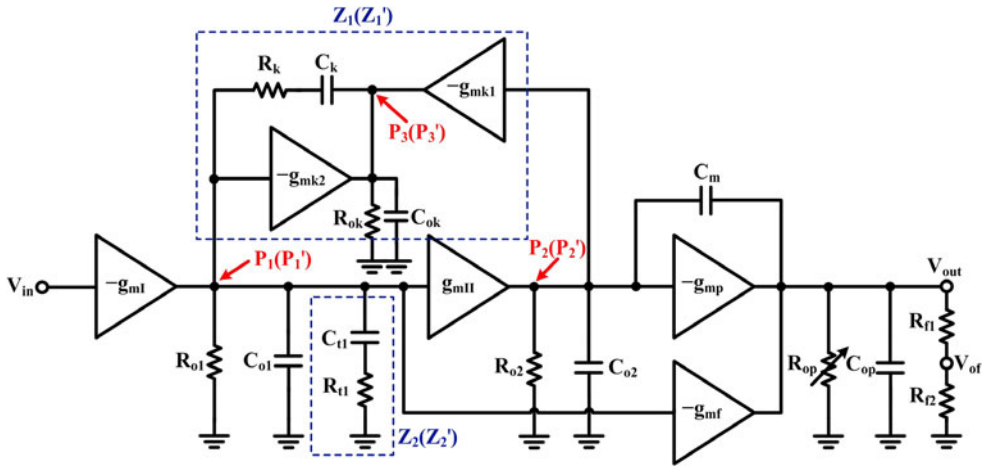

Fig. 5 Block diagram of the proposed LDO regulator without external load capacitor

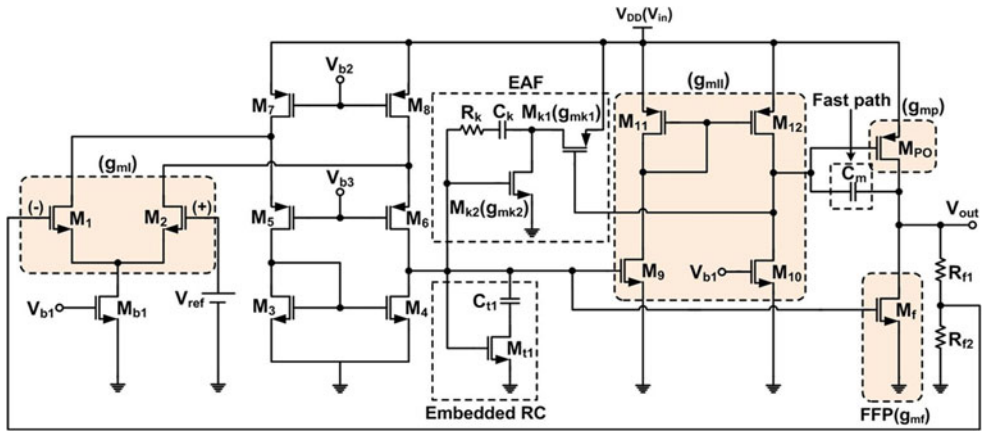

Fig. 6 Schematic of the proposed LDO regulator

proportional to the parasitic gate capacitance; therefore, the bias circuit must be carefully designed to enhance overall efficiency. Capacitor C_m constitutes a fast path capable of reducing response time. Due to the small value of capacitor C_m (3 pF), the combination of feed-forward path (FFP) g_{mf} and the fast path does not produce a right-half plane (RHP) zero inside the unity-gain frequency to degrade phase margin. In addition, capacitor C_m pushes the pole of the second stage output to a lower frequency. The feedforward stage (g_{mf}) accelerates the transient discharge time of the output terminal. We have also designed an embedded RC block (C_{t1}, R_{t1}) to add another internal zero compensation to reduce phase shift at high frequencies.

In Fig. 5, $P_1(P_1')$ is the dominant pole, contributed by the output of the first amplifier stage. $P_2(P_2')$ represents the second pole, contributed by the output of the second amplifier stage. $P_3(P_3')$ is the third pole, contributed by node n_3 of the enhanced active feedback. $Z_1(Z_1')$ is the first LHP zero, generated by the enhanced active feedback circuit. $Z_2(Z_2')$ represents the second LHP zero, generated by compensation capacitor C_{t1} and compensation resistor R_{t1}. The pole and zero symbols marked "′" represent the poles and zeros generated under heavy loads; otherwise, they refer to light load conditions.

The negative gain of the output stage (power transistor) depends heavily on the load. The gain of the power transistor ($g_{mp}R_{op}$) is inversely proportional to $\sqrt{I_{out}}$. The distribution of gain among the stages is an important consideration. To prevent front stages from forwarding noise, DC gain is distributed such that $A_{V1} > A_{V2} > A_{VP}$. A resistive feedback network was added at the output of the three stage amplifier to form a negative feedback system. The feedback resistors must be large enough to reduce quiescent current for low power design. This architecture requires a high loop gain to provide high-precision LDO output voltage.

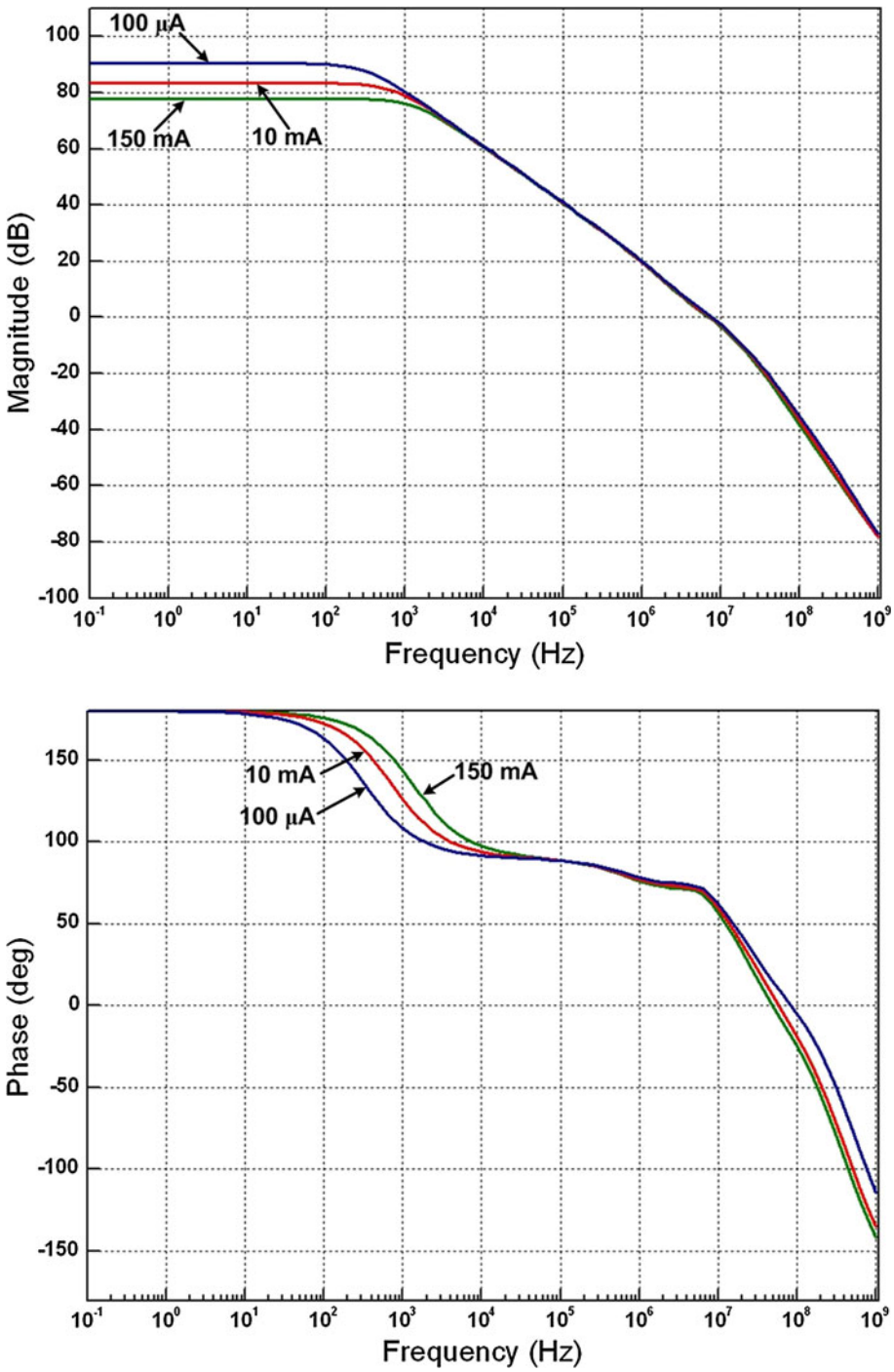

Fig. 7 Simulated loop gain and phase responses of the proposed LDO regulator under different loads without external load capacitor ($C_{out} = 0$, $C_{op} = 100$ pF)

3.2 Analysis of stability without external load capacitor

The circuitry of the proposed LDO regulator is detailed in Fig. 6. Transistors M_1–M_8 form the first stage of the error amplifier while transistors M_9–M_{12} form the second stage. The dominant pole is contributed by the output of the first stage. Capacitor C_k, the transconductance of the second stage g_{mII}, and the gain stage g_{mk1} introduce the pole-splitting effect, which pushes the pole of the first stage output toward very low frequencies, resulting in a new dominant pole for the system. Meanwhile, the pole produced by the output node of the negative gain stages g_{mk1} and g_{mk2} is pushed toward a higher frequency, resulting in the third pole of the feedback loop. The feedforward stage (g_{mf}) reduces the output impedance at the output node of the LDO regulator. Compensation capacitor C_m splits the poles at the input and output nodes of the power transistor

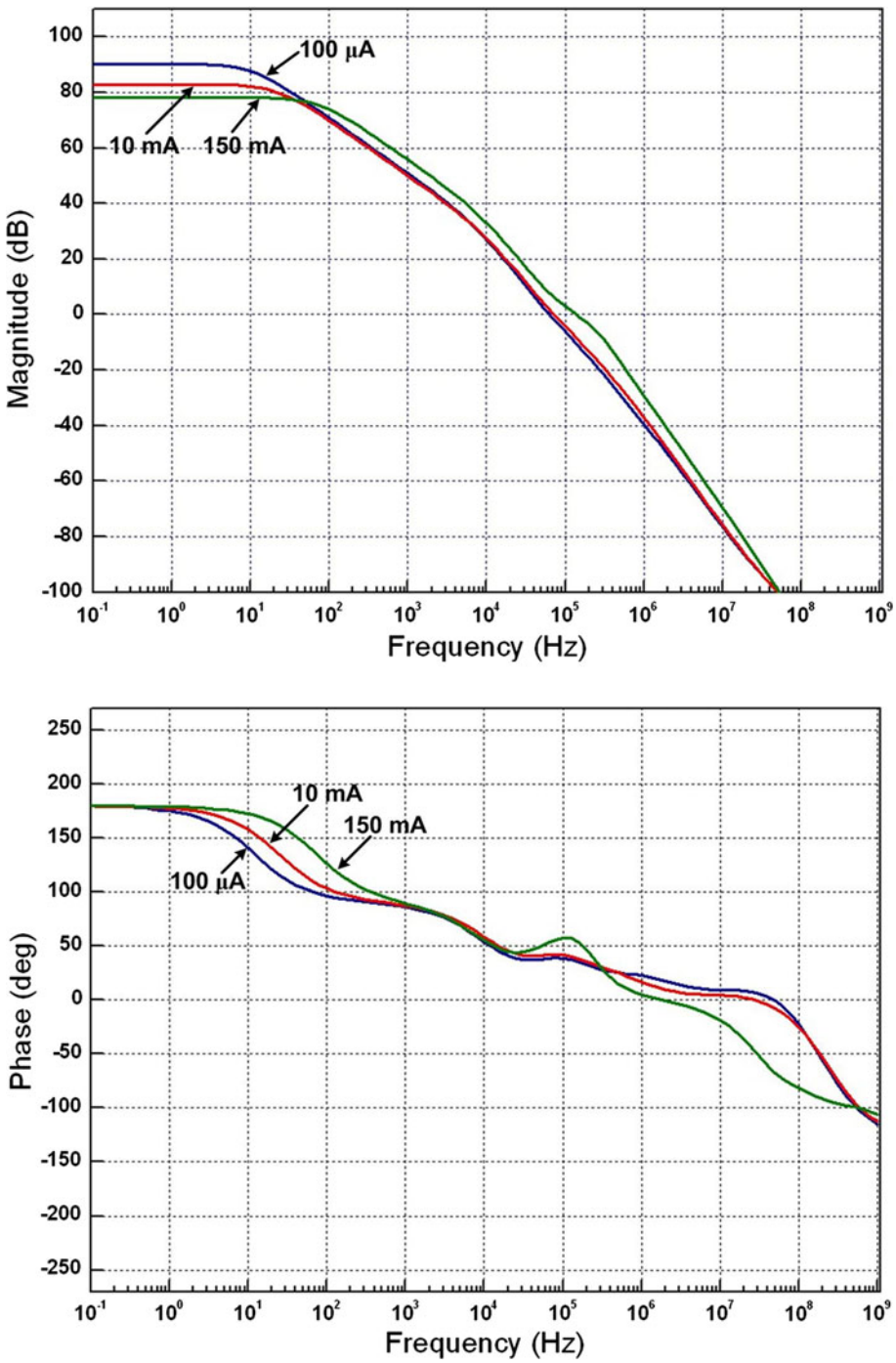

Fig. 8 Simulated loop gain and phase responses of the proposed LDO regulator under different loads using external load capacitor ($C_{out} = 10$ µF, $R_{esr} = 0.1$ Ω)

stage. Thus, the pole at the LDO regulator output node is pushed toward frequencies higher than the unity gain frequency, by the transconductance of the power transistor and compensation capacitor C_m. The pole at the power transistor M_{PO} gate node is then pushed toward lower frequencies, forming the second pole of the feedback loop.

Compensation resistor R_k, compensation capacitor C_k, negative gain stages g_{mk1}, g_{mk2}, and g_{mII} introduce a first LHP zero, Z_1. The first LHP zero cancels the third pole. Resistor R_k and capacitor C_k allow independent adjustment over the placement of the first zero. Resistor R_{t1} and capacitor C_{t1} can also introduce a second LHP zero, Z_2. The second LHP zero is presented to improve the phase margin of the LDO regulator. Resistance R_{t1} is the small signal equivalent resistance of the transistor M_{t1}. Capacitor C_{t1} also allows independent adjustment over the placement of the second zero. All of the major zero and pole relationships are indicated in Fig. 5.

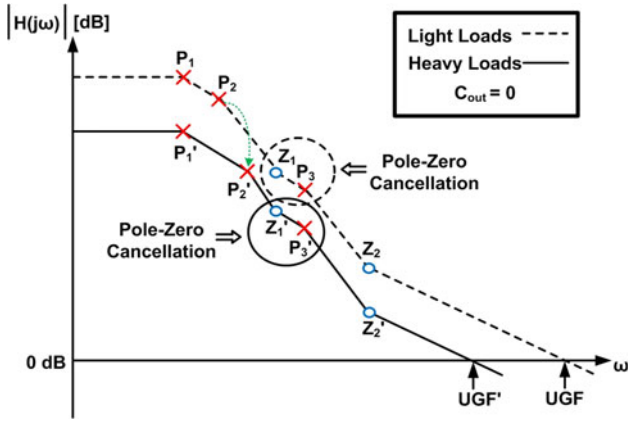

Fig. 9 Frequency response of the proposed LDO regulator with $C_{out} = 0$

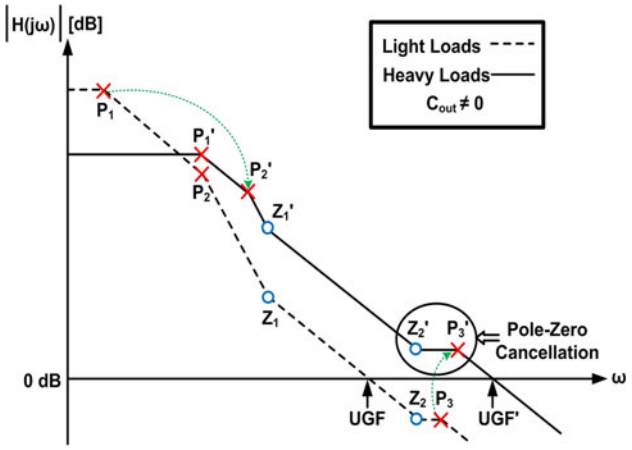

Fig. 11 Frequency response of the proposed LDO regulator with $C_{out} \neq 0$

Figures 7 and 8 are the simulated loop gain and phase responses of the proposed LDO regulator under different loads with different C_{out} conditions. The frequency response of the proposed LDO regulator without external load capacitor is divided into two states: light load and heavy load, as shown in Fig. 9. The open loop gain transfer function of the proposed structure is given by

$$H_{(cap-less)}(s) \approx \frac{A_{DC}\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{\left(1+\frac{s}{P_{-3dB}}\right)\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)} \tag{3}$$

$$A_{DC} = g_{mI}g_{mII}g_{mp}R_{o1}R_{o2}R_{op}\left(\frac{R_{f2}}{R_{f1}+R_{f2}}\right) \tag{4}$$

$$P_{-3dB} = P_1 = P_1' = \frac{1}{C_k g_{mk1} g_{mII} R_{ok} R_{o1} R_{o2}} \tag{5}$$

$$P_2 = P_2' = \frac{g_{mII}g_{mk1}}{\left(C_m g_{mp} g_{mk2} R_{op} - C_m g_{mk1} g_{mf} R_{op} + C_{t1} g_{mII} g_{mk1} R_{t1}\right)} \tag{6}$$

$$P_3 = P_3' = \frac{g_{mk2}C_k}{C_{o1}C_{ok} + C_k C_{o1} + C_k C_{ok}} \tag{7}$$

$$Z_1 = Z_1' = \frac{g_{mk2}(g_{mII} + g_{mk1})}{C_k[(g_{mk2} - g_{mII} - g_{mk1}) - g_{mk2}(g_{mII} + g_{mk1})R_k]} \tag{8}$$

$$Z_2 = Z_2' = \frac{1}{C_{t1}R_{t1}} \tag{9}$$

$$UGF = UGF' = \frac{g_{mI}g_{mp}R_{op}}{C_k g_{mk1} R_{ok}}\left(\frac{R_{f2}}{R_{f1}+R_{f2}}\right) \tag{10}$$

where g_{mI}, g_{mII}, g_{mp}, C_{o1}, C_{o2}, C_{op}, R_{o1}, R_{o2}, and R_{op} are the transconductance, output capacitance and output resistance of the three stages, respectively. Because C_{o2} and C_{op} are smaller than the other parameters in the derivation process and are thus neglected, these two symbols do not appear in the above equations.

The elements g_{mk1}, g_{mk2}, C_k, and R_k represent the transconductance, compensation capacitance, and compensation

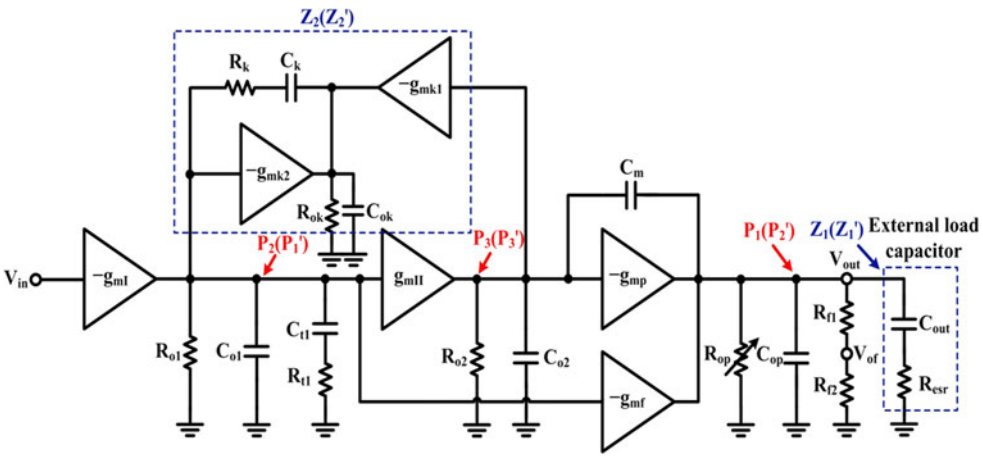

Fig. 10 Block diagram of the proposed LDO regulator with external load capacitor

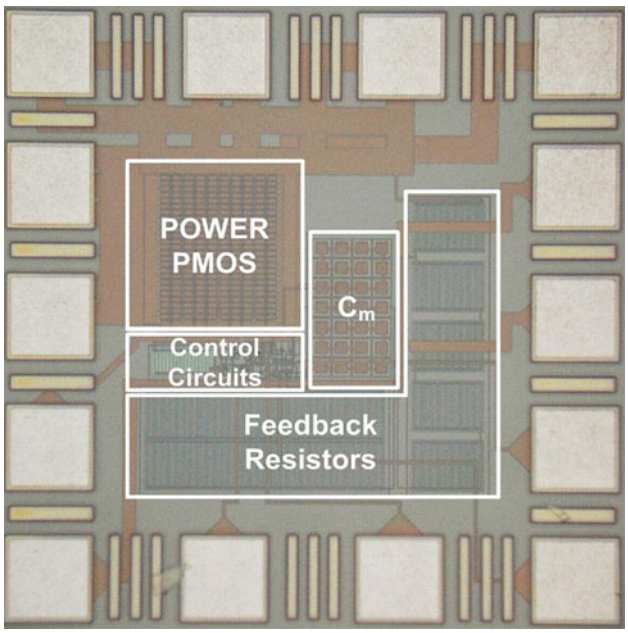

Fig. 12 Microphotograph of the proposed LDO

resistance of the enhanced active feedback block, respectively. The small signal elements C_{t1} and R_{t1} are the equivalent capacitance and equivalent resistance of the embedded RC block. g_{mf} and C_m are the transconductance of the feedforward stage and the fast path capacitance, respectively.

The unity gain bandwidth location changes with load current. When there is no load capacitor, the loop bandwidth is larger. This large bandwidth improves signal transient response at $C_{out} = 0$ resulting in fast line transient and load transient states. The loop bandwidth under light load is larger than under heavy load, which degrades stability under light loads. The proposed LDO voltage regulator provides a loop bandwidth of 7.8 MHz under light loads and 6.5 MHz under heavy loads. Three poles and two LHP zeros were designed in the loop, as shown in Fig. 9. Pole-zero cancellation was achieved by Z_1 and P_3. Z_2 reduces phase shift and maintains an adequate phase margin. Even when heavily loaded, the system still provides three poles and two zeros, which ensure that stability is maintained.

3.3 Analysis of stability using external load capacitor

The other situation involves load capacitors at the output terminal of the LDO regulator. Figure 10 shows the block diagram of the proposed LDO regulator with external load capacitor, which also illustrates all of the major zero and pole relationships. Under light loads, the dominant pole (P_1) is formed by the large load capacitor and the second pole (P_2) is contributed by the output of the first stage, while the dominant pole (P'_1) is contributed by the output of the first stage and the second pole (P'_2) is formed by the large load capacitor under heavy loads. The third pole ($P_3(P'_3)$) is contributed by the output of the second stage, the first LHP zero ($Z_1(Z'_1)$) is formed by the load capacitor and the ESR, and the second LHP zero ($Z_2(Z'_2)$) is formed by the EAF circuit. The pole and zero symbols marked "′" represent the poles and zeros generated under heavy loads; otherwise they refer to light load conditions. The transfer function can be derived, and three poles and two LHP zeros are shown as follows.

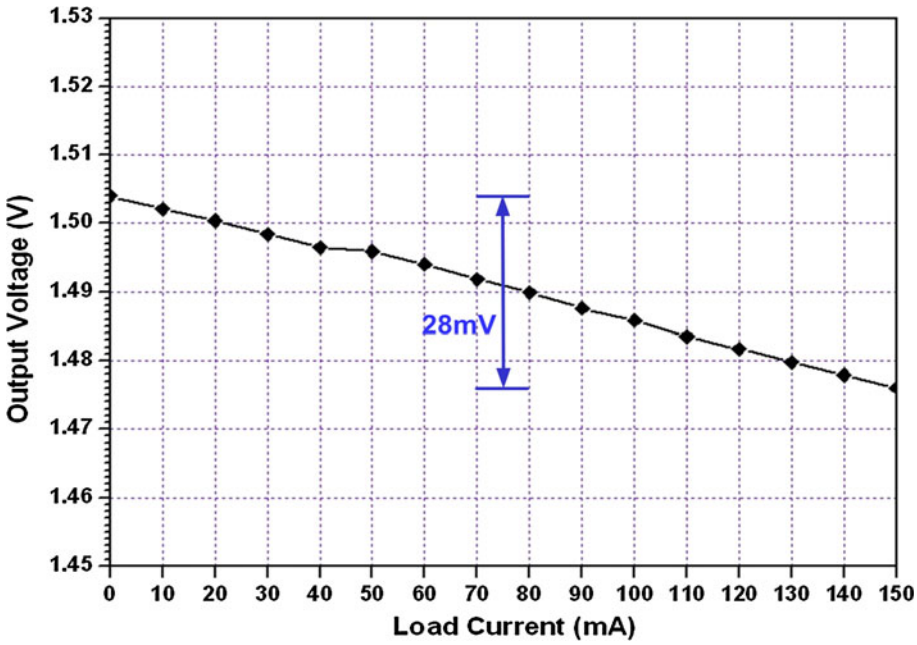

Fig. 13 Measured load regulation of the proposed LDO

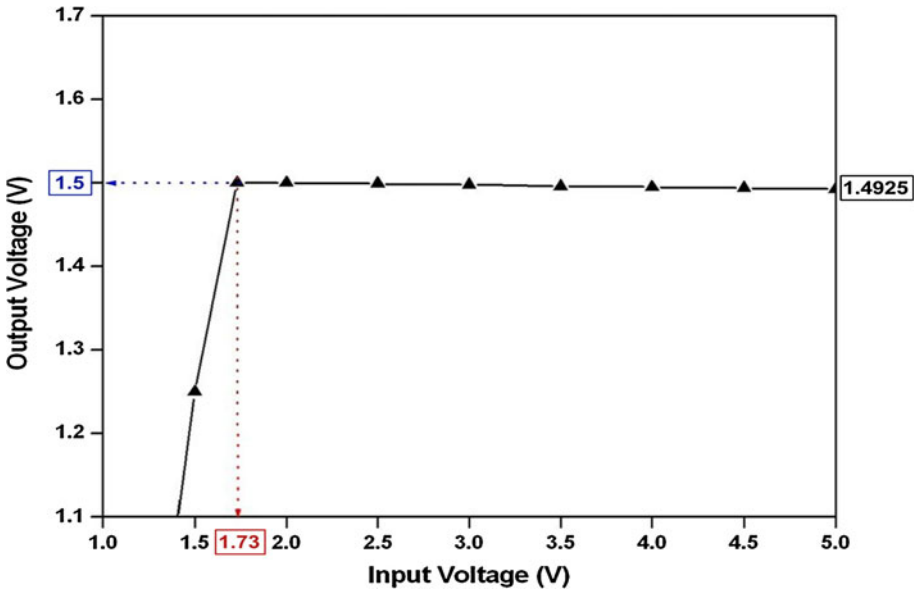

Fig. 14 Dropout voltage performance at 150 mA load current

$$A_{DC} = g_{mI}g_{mII}g_{mp}R_{o1}R_{o2}R_{op}\left(\frac{R_{f2}}{R_{f1}+R_{f2}}\right) \tag{11}$$

$$P_1 = P_2' = \frac{1}{C_{out}\left(R_{esr}+R_{op}\right)} \tag{12}$$

$$P_2 = P_1' = \frac{1}{C_k g_{mk1} g_{mII} R_{ok} R_{o1} R_{o2}} \tag{13}$$

$$P_3 = P_3' = \frac{g_{mII}g_{mk1}\left(R_{esr}+R_{op}\right)}{\left[\begin{array}{l} C_m g_{mp} g_{mk2}\left(R_{esr}+R_{op}\right) \\ -C_m g_{mk1} g_{mf}\left(R_{esr}+R_{op}\right) \\ +C_{t1} g_{mII} g_{mk1} R_{t1} \end{array}\right] R_{op}} \tag{14}$$

$$Z_1 = Z_1' = \frac{1}{C_{out}R_{esr}} \tag{15}$$

$$Z_2 = Z_2' = \frac{g_{mk2}(g_{mII}+g_{mk1})}{C_k[(g_{mk2}-g_{mII}-g_{mk1})-g_{mk2}(g_{mII}+g_{mk1})R_k]} \tag{16}$$

$$UGF = \frac{g_{mI}g_{mII}g_{mp}R_{o1}R_{o2}R_{op}}{C_{out}\left(R_{esr}+R_{op}\right)}\left(\frac{R_{f2}}{R_{f1}+R_{f2}}\right) \tag{17}$$

$$UGF' = \frac{g_{mI}g_{mp}R_{op}}{C_k g_{mk1} R_{ok}}\left(\frac{R_{f2}}{R_{f1}+R_{f2}}\right) \tag{18}$$

When load capacitors are added, the loop bandwidth is reduced. When the load current is small, the system generates two low frequency poles and one zero located at a frequency below the unity-gain frequency. When the load current increases continuously, the dominant pole P_1 shifts to higher frequency pole P_2', and pole P_3' show up below the unity gain frequency. The proposed EAF compensation network creates one new dominant pole P_1' at lower

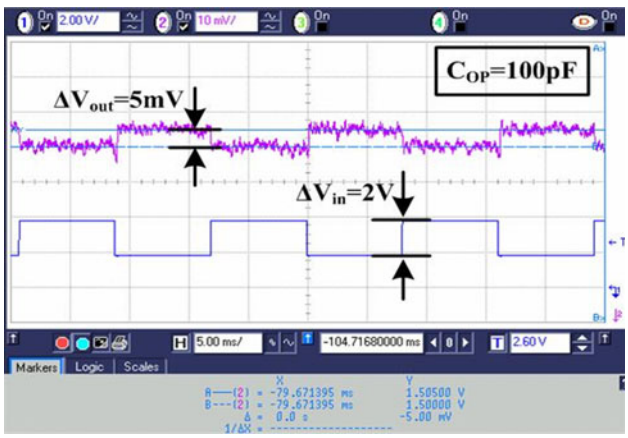

Fig. 15 Measured line transient response and line regulation with $C_{OP} = 100pF$

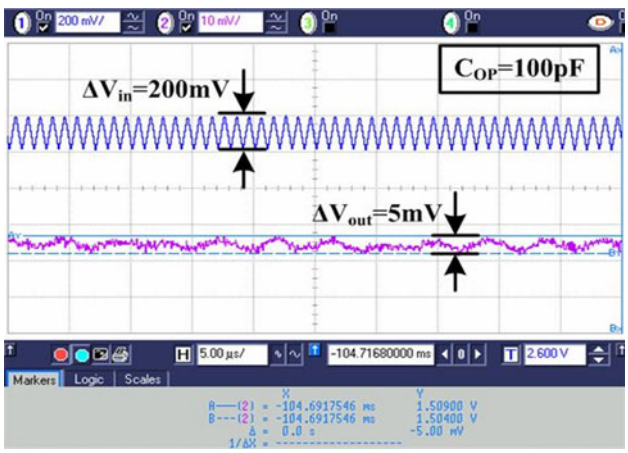

Fig. 16 Measured ripple rejection with $C_{OP} = 100pF$

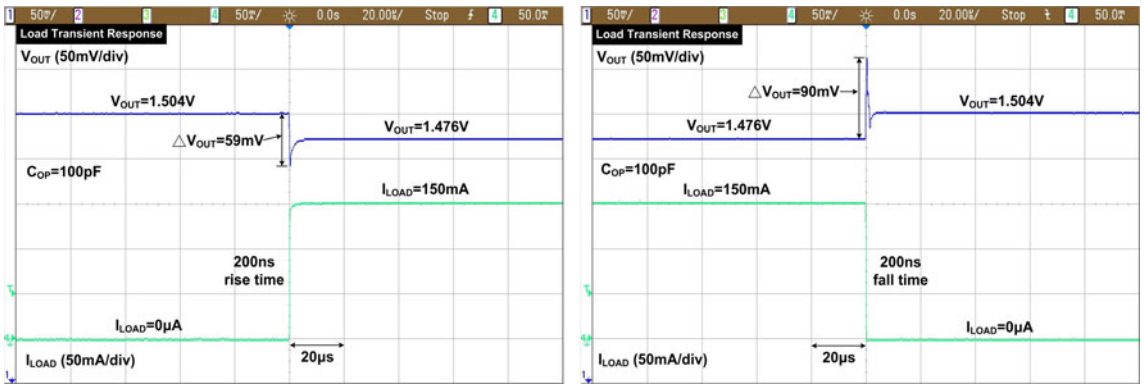

Fig. 17 Measured load transient response with $C_{OP} = 100$ pF

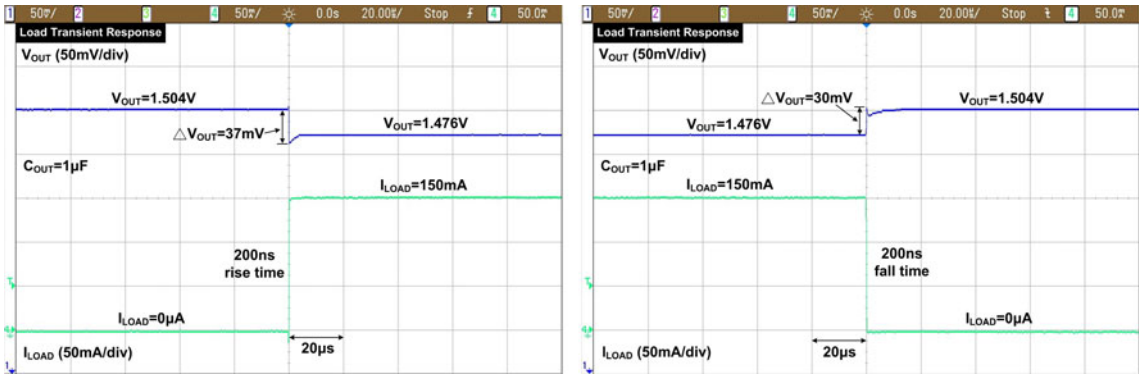

Fig. 18 Measured load transient response with $C_{out} = 1$ μF

frequencies and one new zero Z_2' to cancel out pole P_3', as shown in Fig. 11. When $C_{out} = 10$ μF, the proposed LDO voltage regulator provides a loop bandwidth of 71.4 kHz under light loads and 139 kHz under heavy loads, respectively. Nevertheless, the circuit must still be rendered carefully to guarantee adequate phase margin to avoid oscillation and over-ringing instability during supply voltage startup or transient state change.

4 Measurement results

The LDO regulator was implemented using TSMC 0.35-μm standard CMOS technology. Figure 12 shows the die microphotograph of the proposed LDO regulator, with an effective die area of 0.14 mm^2, including feedback resistors. The output voltage of the regulator is shown in Fig. 13 as the load current is varied from 0 to 150 mA. The output voltage of the regulator is shown in Fig. 14 as the supply voltage is varied from 1 to 5 V. The DC load and line regulation performance of the LDO regulator are 0.187 mV/mA and 2.5 mV/V, respectively. The high loop gain architecture of the LDO limits error in the output voltage. The negative feedback of the LDO regulator adjusts the source-gate voltage of the power PMOS with the change of load current. A continuous increase in load current decreases the gate voltage of power PMOS until it reaches zero, at which point the LDO regulator is unable to regulate. In this design, dependent on the aspect ratio and the maximum source-gate voltage of the power PMOS, the maximum driving capacity of the LDO regulator is larger than 150 mA.

To characterize the line transient response, a supply voltage pulsating between 1.8 and 3.8 V was applied to the input, and the effect at the output was measured. The results are shown in Fig. 15. Figure 16 demonstrates that the proposed LDO regulator largely reduces input ripple noise from 200 to 5 mV at 1 MHz, which corresponds to a 40-fold reduction.

Another important characteristic is the load transient response. When the load current is rapidly pulsed from 0 to 150 mA and from 150 mA to 0 under capacitor-less conditions, the maximum variations in transient output are 59 and 90 mV, respectively, as shown in Fig. 17. When the

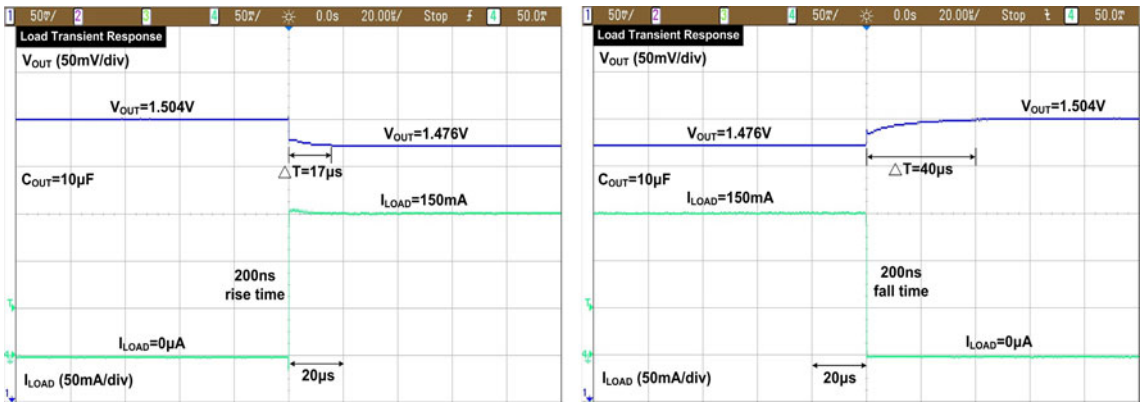

Fig. 19 Measured load transient response with $C_{out} = 10$ µF

Table 1 Summary of the LDO Performance

Supply voltage	1.73–5 V
Output voltage	1.5 V
Max. output current	150 mA
Quiescent current	40 µA
Dropout voltage	230 mV
$AV_{out\text{-}transient}$	59 mV, $C_{OP} = 100$ pF @ $\Delta I_L = 150$ mA
Line regulation	2.5 mV/V
Load regulation	0.187 mV/mA
PSRR	−71 dB @ 100 Hz
	−69.5 dB @ 1 kHz
	−63 dB @10 kHz
Output noise	$3.24\ \mu V/\sqrt{HZ}$ @ 100 Hz
C_{OUT}	100 pF (C_{OP})/1 µF/10 µF
Active area	0.14 mm^2

regulator output was connected to a 1 µF load capacitor, the maximum variations in transient output were 37 and 30 mV for a transient load current step between 0 and 150 mA, as shown in Fig. 18. When the regulator output was connected to a 10 µF load capacitor, the maximum output recovery times were 17 and 40 µs for a transient load current step between 0 and 150 mA, as shown in Fig. 19. The rise/fall time of the 0 to 150 mA load current pulse was 200 ns.

A summary of the proposed LDO regulator performance is shown in Table 1. The input voltage ranges from 1.73 to 5 V. The LDO regulator is capable of operating down to 1.73 V with a preset output voltage of 1.5 V. The quiescent current is only 40 µA. The dropout voltage for the worst case load current (150 mA) is 230 mV. The power supply rejection ratio (PSRR) is less than −71 dB for frequencies up to 100 Hz. The equivalent output noise at 100 Hz is approximately $3.24\ \mu V/\sqrt{HZ}$. Table 2 presents the specifications of the proposed LDO regulator and a comparison

Table 2 Comparison with previously published LDO regulators

Parameter	[8]	[9]	[10]	This work
Technology	90-nm CMOS	0.35-^m CMOS	0.35-fim CMOS	0.35-nm CMOS
Pass element	PMOS	PMOS	PMOS	PMOS
I_{Load} (mA)	100	100	50	150
Quiescent current (I_QLuA)	6,000	170	65	40
Dropout coltage (mV)	300	200	200	230
C_{OP} (pF)	600 pF	100 pF[a]	100 pF[a]	100 pF[a]
Response time T_R (ns)[b]	0.54	0.06	0.18	0.039
Load regulation (mV/mA)	1.8	0.02	−0.56	0.187
Line regulation (mV/mA)	N.A.	3.3	−23	2.5
FOM (ps)[b]	32.4	0.102	0.234	0.01

[a] The estimated maxmimum output capacitance $C_{OP} = 100$ pF from parasitics and test equipments

[b] Adopted from [8], $T_R = C_{OUT} \times V_{OUT}/I_{LOAD(Max.)}$ and FOM = $T_R \times I_Q/I_{LOAD(Max.)}$

with other published designs. The proposed regulator achieved performance in maximum load current (150 mA), quiescent current (40 µA), line regulation (2.5 mV/V), and Figure of Merit (FOM = 0.01 ps) superior to that afforded by other designs. A lower FOM implies better transient response.

5 Conclusion

This paper proposes a novel frequency compensation network design for a low dropout voltage regulator and measurement data are presented. Stability in the LDO

regulator using enhanced active feedback techniques and embedded RC blocks can be achieved with or without loading capacitors. The LDO regulator adopts both a feedforward path and a fast path to achieve fast load transient responses and small overshoots and undershoots. The design provides large loop gain to improve line and load regulation. Compared with previously published LDO regulators, the proposed approach provides low quiescent current and high speed transient response as shown in Table 2. The FOM of this regulator compares favorably to other published works.

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Chia-Min Chen received the M.S. degree in electrical engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2006. He is currently working toward the Ph.D. degree at the Department of Electrical Engineering, National Chiao Tung University, Hsinchu, Taiwan. His research interests include mixed-signal integrated circuit design, power management integrated circuits, and energy-efficient integrated circuits and systems.

Chung-Chih Hung received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1989, and the M.S. and Ph.D. degrees in electrical engineering from The Ohio State University, Columbus, Ohio, in 1993 and 1997, respectively. From 1997 to 2003, he worked for several IC design companies in San Jose, CA and San Diego, CA, where he held analog circuit design manager and director positions. Since 2003, he has been with National Chiao Tung University, Hsinchu, Taiwan, where he is currently a Full Professor in the Department of Electrical Engineering. His research interests include the design of analog and mixed-signal integrated circuits for communication and high-speed applications.