CARBON 54 (2013) 336–342

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Local anodic oxidation kinetics of chemical vapor deposition graphene supported on a thin oxide buffered silicon template

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ARTICLE INFO

Article history:
Received 25 September 2012
Accepted 21 November 2012
Available online 1 December 2012

ABSTRACT

Study of local anodic oxidation (LAO) of single layer graphene (SLG) supported on thin oxide buffered silicon template is reported. Centimeter scaled SLG sheet grown through chemical vapor deposition on Cu foil is transferred onto patterned silicon template covered with thin oxide steps. LAO are performed on the supported SLG through contact mode atomic force microscopy in ambient condition. LAO bumps with heights exceed physical carbon–oxygen stacking are formed on thin oxide buffered samples. Micro-Raman spectroscopy reveals the coexistence of surface graphene oxide formation and local strain near the LAO patterns. The writing speed dependence of LAO bump shows a multi-exponent behavior, indicating inhomogeneous chemical profiles involved in the LAO process. The observation points to a sequential kinetics of surface SLG oxidation prior to subsurface silicon oxide protrusion formation. Our work shows the necessity to consider oxidation of substrate through the subsurface buffer layer during nano-scaled field effect device fabrication with LAO method. The strain generation from the subsurface protrusion suggests possible tuning knob for local distortion of SLG structure.

1. Introduction

Since the realization of single layer graphene (SLG) by mechanical exfoliation of highly ordered pyrolytic graphite (HOPG) in 2004 [1], advancement in understanding on physical and material properties of graphene has been phenomenal [2–5]. This truly two-dimensional material provides a template for understanding low dimensional physics with lower technological barrier. In term of application, graphene is one of the most anticipated materials for future electronic devices. The high electron mobility and transparent properties make it an attractive candidate for variety of devices such as field effect transistor [6], light emitting diode [7], photovoltaic and even flexible electronics [8].

To date, SLG sheet can be acquired by variety of technique besides mechanically exfoliation of HOPG. Among all, SLG grown by thermal decomposition on the (0001) surface of 6H−SiC [9] and chemical vapor deposition (CVD) on transition metal [10] are the most sought-after methods due to their scalability for industrial application. Furthermore, the SLG can be easily transferred to other template from the metal substrate using chemical etchings [11]. It enables flexibility for studies on the interactions between SLG and various substrates, along with the potential for hybrid device fabrication.

Further realization of graphene application requires more manipulations techniques about it in order to fine-tune its properties. Pristine graphene is known to be a gap-less material around the Fermi level with linear dispersion relation [12].

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0008-6223/$ - see front matter
http://dx.doi.org/10.1016/j.carbon.2012.11.045

For electronics application, band gap opening of graphene can provide substantially more opportunities for further conductivity control by electronic means [13]. So far, band gap opening has been demonstrated with variety of methods including adatom/molecule absorption [14], substrate back-gating [15], and nano-ribbon formation through local anodic oxidation (LAO) [16–21].

LAO of silicon or metal substrate is a well developed technique that enables nanometer scale mask-less lithography [23–25]. In ambient, water bridges form between the tip of atomic force microscope (AFM) probe and substrate surface. When appropriately biased, water molecules decompose under strong vertical electrical field and interact with the surface atoms to form oxidation feature. LAO is a complex physical–chemical process that is co-determined by tip bias, humidity, substrate surface hydrophilicity, writing speed, and substrate/probe work function [23–25].

Realizations of LAO on graphene have been demonstrated recently [16–21]. So far, LAO of graphene has been successfully demonstrated on various graphene and substrates conditions including mechanically exfoliated graphene on 300 nm SiO_2 buffered silicon substrate [16–20] and epitaxial graphene on SiC(0001) [21]. In most cases, trenches are formed due to the generation of volatile oxide under high bias conditions. Ribbons are usually found around the trenches and it drastically increases the resistance of the graphene flake due to higher electron scattering [16,17]. On the other hand, bumps can be found in some other cases where oxygen is incorporated into graphene due to non-volatile oxidation [17,19]. Under low electric field, the oxidation may be non-volatile and lead to oxygen incorporation into the carbon network. Graphene oxide has been found luminescent under optical pumping. The photoluminescence (PL) comes from band gap opening by introducing SP^3 bonding into the SP^2 bonded network through bonds reconstruction processes [22]. It is therefore a very intriguing approach to generate localized PL spots by LAO of graphene. With appropriate oxidation, insulating graphene oxide (GO) can be formed. It has been demonstrated that when a graphene flake is enclosed by insulating GO, the lateral electrical conductance diminishes [19]. The above works showed the potential of using LAO for the fabrication of nanometer scale graphene based devices without masks or photo-resists. Nevertheless, as shown in many previous cases, due to the chemical inertness of graphene, LAO usually has to be started at the edge of graphene where unpaired carbon bonds are available [16–19]. Moreover, as in most of cases, the graphene samples are usually supported on 300 nm thick buffered oxide (BO) buffered silicon template. Additional metallic contacts are usually needed in order to apply voltage difference between the sample and AFM probe. The above issues make LAO process less convenient and limit its application in graphene study. Until very recently, there is report showing LAO of exfoliated graphene without additional metallic contact [20]. In above study, relatively high biases are employed due to the strong dielectric shielding effect of the 300 nm BO. If back gating is considered to be employed to control the conductance of the insulated graphene device through capacitive coupling across the BO, one must look for a way to substantially reduce the applied voltage. For this purpose, reduction of BO thickness could be considered.

In this work, we focus on controllable LAO on centimeter size CVD graphene with vertical electric field by simply tuning the back-gating conditions, at any location on the graphene sheet. We are especially interested in the case where the BO thickness is relatively thinner. In this case, due to weaker dielectric shielding, considerably lower threshold for back-gating voltage is expected for device application. Establishment of the above could give rise to fine-tuned electrical doping control for an insulated graphene flake by capacitive coupling. In another word, it is possible to perform *in situ* graphene based field effect devices fabrication, if we understand the LAO kinetics well.

2. Experimental

2.1. *Sample preparation*

The SLG is grown on 25 μm thick Cu foil in a quartz tube furnace system using a CVD method involving methane and hydrogen gases [10,11]. Under vacuum conditions of 10 mTorr, the furnace is heated with 2 sccm flow of H_2 inlet. The growth temperatures is 1000 °C. After 40 min of heating to anneal the Cu foil, a flow of 35 sccm of methane is subsequently introduced for a growth time ranging from 30 s to 15 min. A quick cooling process are then applied (300 °C/min) after growth, and the methane and hydrogen gas flows were continued throughout the cooling process. The typical grain size of SLG flakes on Cu foil was examined through field emission scanning electron microscopy (SEM). Fig. 1a shows the typical SEM micrograph. It was found that the typical grain size is about two to three micro-meter. The electrical conductivity was examined with Hall measurement to ensure good lateral electron mobility. After transferring the films to SiO_2/Si wafers through polymethyl methacrylate (PMMA) coating and iron (III) nitrate etching [26], the films is then further analyzed by Raman spectroscopy to ensure its monolayer characteristics.

The patterned silicon substrate is fabricated by conventional photolithography process. 100 nm Thick tetraethyl orthosilicate (TEOS) BO layer was deposited on a 6-in. n-type ⟨100⟩ (10–30 Ω-cm) Czochralski silicon wafer and subsequently developed by I-line stepper photolithography. A reactive ion etching (RIE) is followed to selectively etch the BO layer and result in well defined oxide steps. Prior to SLG sheet transferring process, the BO steps were etched by dilute HF to result in step height (h_{BO}) ranging from 3 to 40 nm. No crumpling of SLG sheet was found and the height differences between the BO steps and the exposed area show no significant difference from the initial condition before transferring. The above observations indicate conformal SLG attachment on the surface of supporting template. It is speculated that the capillary forces during the solution drying process and Van der Waals attraction between SLG and the supporting template are the major causes for the conformal attachment. Good electrical contact between the back side of silicon substrate and sample holder is ensured during the LAO processes. No additional metallic contact is needed since

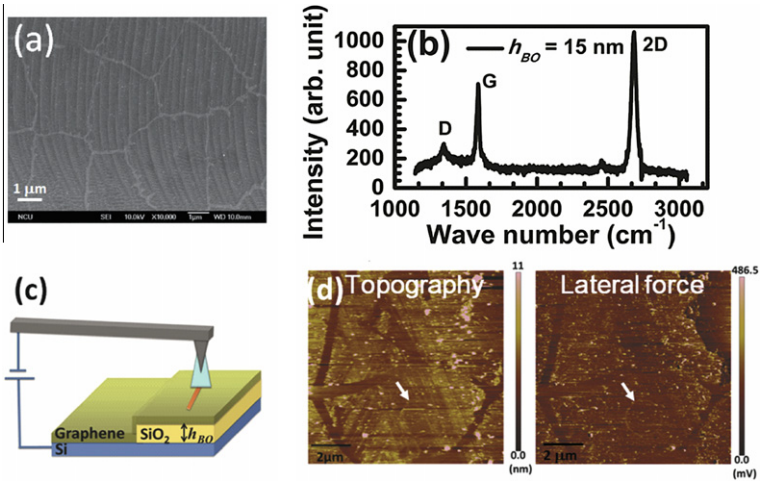

Fig. 1 – (a) Typical SEM image for completely as-grown CVD SLG on Cu foil. (b) Typical micro-Raman spectroscopy for SLG transferred on 15 nm thick BO buffered silicon substrate. The 2D, G, and D band are indicated. A typical $I_{2D}/I_G \sim 1.8$ is found for this case. (c) Stack scheme of the sample and schematic plot of the experiment setup, with h_{BO} the thickness of BO. (d) Typical AFM images for SLG transferred on SiO_2/Si template. The left and right images represent the topography and lateral force information, respectively. A circular pattern is drawn in the lower part of the AFM micrograph, as marked by the white arrow.

part of the SLG sheet is in electrical contact with the exposed silicon area under back-bias. The continuity of the SLG sheet ensures voltage difference is the same between tip and SLG at any location on the SLG.

2.2. *Characterization and fabrication methods*

Raman spectroscopy is employed to evaluate the quality of SLG on the SiO_2/Si substrate [27]. Signature 2D and G bands are detected at 2680 and 1580 cm^{-1} respectively. Notably, a low D band was detected, indicating low defect density for the CVD SLG. In this experiment, the I_{2D}/I_G ratio varies in between 1.8 and 2.0 due to interference effect from different BO thicknesses [28]. The intensity of each bands become significantly lower when the BO layer is thinner than 10 nm. Nevertheless, symmetry 2D band can always be detected for every case, which indicates SLG characteristics (Fig. 1b).

LAO is conducted with a Bruker Innova AFM equipped with a custom implemented external bias source that allow for bias application at range between ±50 V, with tunable step <0.01 V. Conductive AFM probe (Pt/Ir coated point-probe series, Nanosensor) is used for LAO in a chamber with controlled relative humidity (RH) ~ 50% throughout the experiment. Although tapping mode AFM is also found to be able to result in oxidation under certain conditions, contact mode AFM is used in this work for LAO due to better pattern continuity and reproducibility. Patterns or lines could be drawn by using the built-in software (Nanoplot, Bruker) with closed loop function to enable exact positioning down to nanometer scale precision. The schematic illustration of the experimental setup is presented in Fig. 1c. Topological and lateral force information are acquired during the same scanning. In Fig. 1d, we show typical AFM images acquired on SLG attached on SiO_2/Si template. Compared to the grain size distribution found on as grown SLG on Cu foil, the AFM images show similar size distribution for the SLG sheet attached on SiO_2/Si template. It further evidences no induced crumples and damages in the transferred SLG. A circular pattern was drawn with LAO in the lower part of the micrograph. For all investigated cases in this work, LAO processes are performed at locations within continuous grain. Clearly, the lateral force image exhibits higher sensitivity in detecting both the grain boundary and oxidation pattern. After the AFM operation, samples are further measured with micro-Raman spectroscopy to reveal the effect of LAO on SP^2 bonding and honeycomb structure modification.

3. Result and discussion

3.1. *AFM characterization*

Fig. 2a shows the bumps generated by LAO at tip bias −12 to −14 V, on 8 nm thick BO buffered silicon template. Notably, at tip bias −12 V, lateral force image is more significant than the topographical counterpart. Similar observation was pointed out by Byun et al. [19] that lateral force signal is more advantageous for the detection of graphene oxidation. The measured bump height vs. bias curve is presented in Fig. 2b. Height measurement of graphene oxidation pattern using contact mode AFM has been reported to cause artifacts due to strong tip–surface interactions [29]. Therefore, care is needed in measuring the bump height with contact mode AFM. Tapping mode AFM is best suited for height characterization and has been employed as reference for evaluating the issue of artifacts. We have found by minimizing the tip–surface interaction through setting set point value to 0 V for contact mode AFM, almost identical topographic information can be acquired for both contact and tapping mode AFM. Therefore, for convenience, we show the contact mode AFM topographic information since it is acquired simultaneously with the lateral force information. In above cases, a fixed LAO writing speed v ($v = 0.1$ μm/s) is employed. The G/SiO_2/

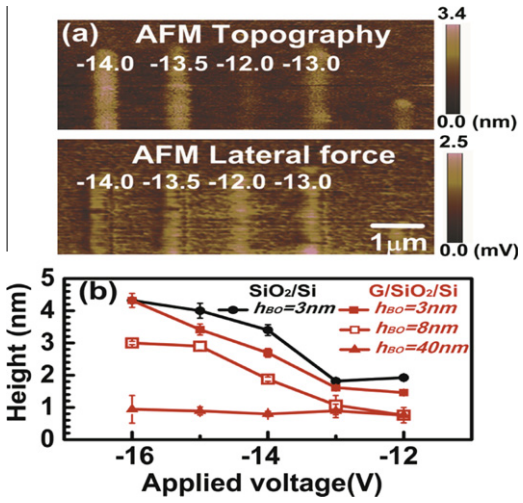

Fig. 2 – (a) Typical AFM topography (upper row) and lateral force (lower row) images of LAO strips on SLG supported on 8 nm BO buffered silicon template. (b) The measured bump height vs. tip bias for various BO thickness conditions. A fixed LAO writing speed v = 0.1 μm/s is employed. The silicon template buffered with 3 nm BO case is plotted for comparison purpose.

Si samples are the SLG transferred on BO buffered silicon while the SiO_2/Si sample is the BO buffered silicon template without SLG. With h_{BO} = 40 nm, a rather flat curve for bump height around 0.8 ± 0.1 nm is obtained. It is noteworthy to mention that there is no observable bump for the case of LAO on 40 nm thick BO buffered silicon template without surface SLG. From our previous studies, it is known that LAO of BO buffered silicon substrate is still possible with h_{BO} < 10 nm [30]. With strong enough bias, hydroxide ion can be accelerated into BO, and reach the underneath SiO_2/Si interface to form silicon oxide [31]. Therefore, the above observation indicates that the applied voltage difference is not strong enough to accelerate ion through the thick BO, and the observed bump on 40 nm thick BO buffered G/SiO_2/Si sample are the result of oxygen incorporation into graphene. On the other hand, for thinner BO case (h_{BO} = 3 nm), the measured bump height can be much higher than the physical thickness of carbon–oxygen stacking, especially under higher bias conditions. In fact, comparing the LAO result on areas not covered by SLG, it is found that the two curves resemble in term of the bias dependence, only differ in the measured bump heights. Slight increase in BO thickness (h_{BO} = 8 nm) leads to change in the curve shape, and significantly lower bump height. Our finding is similar to the observation of local oxidation on SiC(0001) by Alaboson et al. [21]. In their case, the oxidation of SiC substrate leads to bump as high as 3 nm because of volume expansion due to the oxidation of underneath SiC substrate. The above observation suggests that the observed bumps are partly formed by silicon oxide protrusion from the underneath substrate. Graphene is known to be impermeable for gases like oxygen or hydroxide ion under normal condition [32]. Furthermore, under our experimental setup, the electric field is screened by the surface metallic graphene due to contact with the grounded silicon substrate. What then is the pathway for the subsurface silicon oxide formation?

3.2. *Micro-Raman spectroscopy*

The micro-Raman spectroscopy for an oxidized strip is presented in Fig. 3. A scan line with step size of 1 μm across the oxidized strip (10 μm in length, 2 μm in width, lateral force image shown in the left inset) is being measured (Fig. 3a). Here, a LAO strip formed with tip bias at −12 V, with BO = 15 nm is shown as an example. The right inset of Fig. 3a shows the topographical cross-section of the LAO strip. The average measured height is about 1.5 nm. The center of the oxidized strip is located at position 5 in the figure. As shown in Fig. 3b, it is clear that the oxidation leads to deterioration of SP^2 bonding and honeycomb lattice structure, as indicated by the lower *G* and 2*D* band intensity, respectively. The I_{2D}/I_G ratio also drops at the oxidation location (Fig. 3c). Concurrently, significant increase in *D* band intensity, as well as additional *D′* band generation suggest introduction of defect levels into the original energy spectrum, most probably due to bonding with the introduced hydroxide ion by LAO process. A more subtle change in the Raman spectrum is the peak center position and width of *G* band (Fig. 3d). It can be found that *G* band blue shifted for 5 cm^{-1} at the oxidation site. The blue shift is similar to what is observed in epitaxial graphene growth on SiC(0001) [33], where lattice mismatch leads to strain in the graphene layer. In our case, there is only weak Van der Waals interaction between the SLG sheet and underneath transferred supporting template. In this case, the existence of strain suggests local distortion of the SLG sheet, probably due to silicon oxide protrusion from the underneath silicon substrate.

Both AFM and micro-Raman measurements suggest the observed oxidation heights could not be solely attributed to surface GO formation. Coexistence of surface GO and subsurface silicon oxide appears to be a plausible explanation. In thin BO condition, as the case studied here, the LAO process no longer only involves graphene. Rather, a sandwich stacking of graphene/SiO_2/Si (G/SiO_2/Si) must be considered due to the possibility of silicon oxide formation beneath the surface graphene. The metallic SLG is expected to effectively screen the electric field under it under back bias. However, once the SLG is locally oxidized, the oxidized part becomes insulated and acts as additional dielectrics. It effectively opens a pathway for further oxidation of underneath silicon substrate through BO. How then, would the LAO kinetics be affected by this sandwich stacking? More specifically, we are interested in the issue of whether the silicon oxide protrusion forms before or after the GO formation.

3.3. *LAO writing speed*

To understand the above issue, we perform LAO with varying writing speed. It is known for hydrogen passivated silicon and titanium cases [24,25], empirical power laws in LAO writing speed hold ($h_{bump} \propto v^{\gamma}$), where h_{bump} is the measured bump height, v the tip writing speed and γ the characteristic exponent. It was found that γ has value around −0.2 to −0.25 for hydrogen passivated silicon (001) and titanium, respectively. To date, physical explanation for the empirical power law remains elusive. It has been suggested as having to do with the charge accumulation during LAO [25]. In this model, change

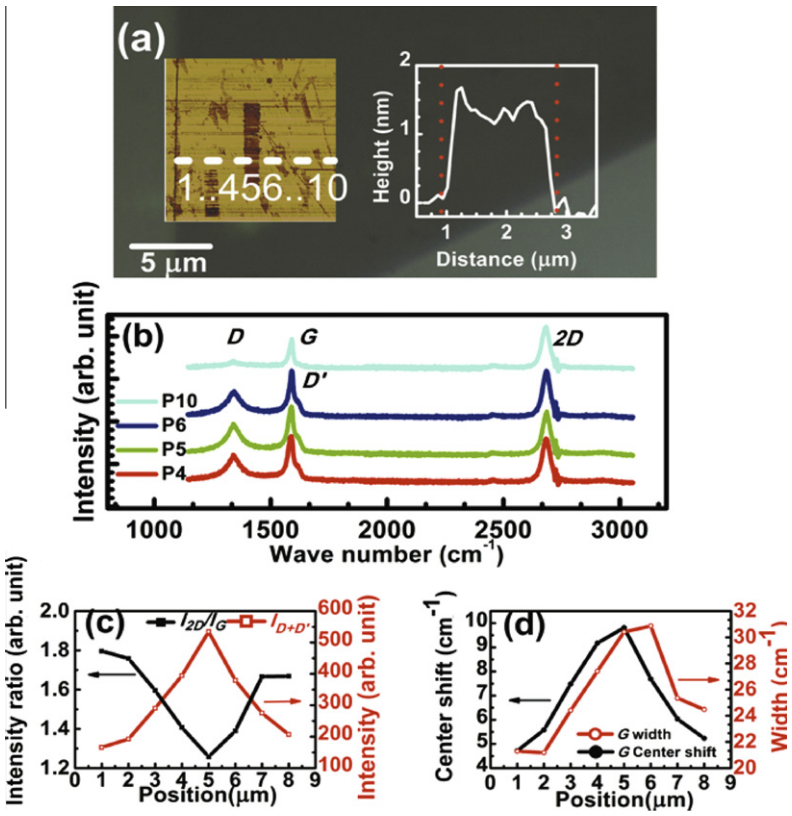

Fig. 3 – (a) The AFM lateral force images inset in the optical micrograph shows location of the scanning line across LAO strip (left). The numbers indicated in the scanning line mark the positions of the micro-Raman measurement. The darker area is the area covered by 15 nm BO. The AFM topography cross-section shows the height profile of the LAO strip formed with −11 V bias on the AFM tip, and v = 0.1 μm/s. across the scanning line in the right inset. (b) The micro-Raman spectra for part of the acquired position along the scanning line, showing significant increase in D and D' band near the LAO location. (c) The I_{2D}/I_G ratio and $I_{D+D'}$. (d) The peak center shift and full width at half maximum (FWHM) of G band for every measured position along the scanning line.

of exponent indicates changes in surface charging condition and hydrophilicity. Therefore, the exponent could serve as good indicator for specific substrate material properties. Observation of change in exponent would point to change of role in oxidation process for the sandwich stacking in our case. Fig. 4 shows the measured bump height vs. LAO writing speed for different conditions (−10 V for h_{BO} = 3 nm, −14 V for h_{BO} = 8 nm). The reason of choosing different biases for different h_{BO} is due to the sensitivity difference for thin or thick BO. Results obtained for SiO_2/Si system is presented alongside for comparison. It is found that for both 3 and 8 nm thick BO cases, the G/SiO_2/Si stacks render significantly steeper curves than the SiO_2/Si cases. Also it appears that at LAO writing speed > 0.7 μm/s, saturated bump heights at about 0.4 nm are found with BO = 8 nm, probably indicating partial GO formation. With thicker BO, the applied bias is only able to oxidize the surface SLG at slower writing speed condition. Also, it is noticeable that the LAO heights measured for the G/SiO_2/Si are always lower. The observation suggests that surface SLG plays the role of additional dielectric layer once it is being completely oxidized. The formed GO decreases the effective electric field between silicon substrate and AFM probe, and results in lower silicon oxide protrusion height.

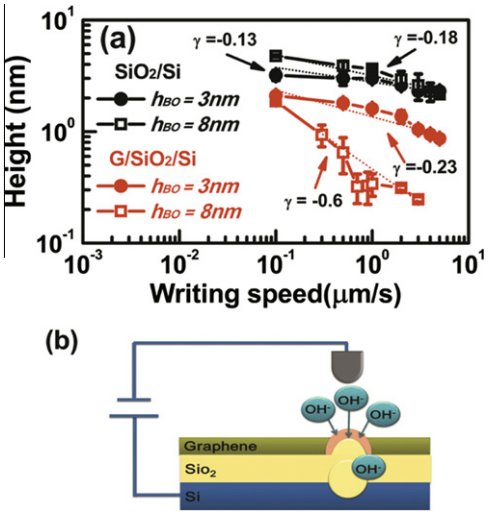

Fig. 4 – (a) The measured bump height vs. LAO writing speed for various conditions. The applied biases are −10 V and −14 V for h_{BO} = 3 nm and 8 nm, respectively. (b) The schematic plot illustrates the LAO mechanism.

The combined observation suggests that the oxidation of surface SLG is a prerequisite for oxidation of underneath silicon. For the G/SiO_2/Si case, before graphene oxidation is completed, the OH^- is not able to penetrate through the BO due to the compactness of graphene's honeycomb lattice [32] and shielding effect from the grounded metallic graphene. After the completion of graphene oxidation, the electric field could accelerate the OH^- through the BO, reaching at the SiO_2/Si interface, result in oxidation of the silicon substrate, and leads to volume expansion and silicon oxide protrusion. The effective electric field, however, becomes lower due to additional dielectric shielding from the surface GO. As a result, the LAO height decreases steeply as writing speed increases, resulting in more negative exponent in the power law fitting. While the overall LAO height becomes lower than in the SiO_2/Si case due to stronger electrical shielding from the formed GO. The figurative illustration of the above model is presented in Fig. 4b.

4. Summary

In conclusion, we report experimental study on local oxidation of CVD SLG supported on thin oxide buffered silicon template. LAO can be achieved at any location in the transferred SLG sheet with relatively low bias without needing additional metallic contacts. It is found that the LAO bumps generated by oxidation processes can be much higher than the physical height of carbon–oxygen stacking, and should not be solely attributed to surface GO formation. Micro-Raman spectroscopy confirmed the coexistence of introduced defect levels, probably by carbon–oxygen bonding and additional strain field due to lattice distortion near the LAO site. LAO writing speed experiments reveal an abrupt drop of LAO bump height as writing speed increases, indicating a threshold like kinetics for the formation of subsurface silicon oxide protrusion. Our experiment data suggests that complete formation of surface GO is prerequisite for the formation of subsurface silicon oxide protrusion.

The implications of the above findings are two folds. First, in fabricating graphene based field effect devices supported on thin BO buffered silicon template by LAO, a threshold voltage/writing speed may hold in which subsurface silicon oxide protrusion cease to grow. If local crumpling of graphene needs to be avoided to optimize surface conductance, knowledge of above would be helpful. Second, the strain generated by subsurface silicon oxide protrusion may be utilized to further fine tune the band gap of the supported graphene. In contrast to the global strain induced by epitaxial template, this kind of local strain could be localized and more specific. The above two implications need to be further explored, and is currently undergoing.

Acknowledgements

This work is supported by the National Science Council of the Republic of China under Contract NSC100-2112-M008-008-MY3. We gratefully acknowledge the facility support from NCU CNST.

Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.carbon.2012.11.045.

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