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Critical review

Growth, dielectric properties, and memory device applications of ZrO_2 thin films

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A B S T R A C T

In the advancement of complementary metal-oxide-semiconductor device technology, SiO_2 was used as an outstanding dielectric and has dominated the microelectronics industry for the last few decades. However, with the recent size downscaling, ultrathin SiO_2 is no longer suitable. ZrO_2 has been introduced as a high-*k* dielectric to replace SiO_2. This paper reviews recent progress of ZrO_2 thin films as dielectric layers for volatile dynamic random access memory (DRAM) applications and as a gate dielectric for CMOS devices. Materials and electrical properties of ZrO_2 films obtained by different deposition methods are compared. The effects of different top and bottom electrodes, and different doping elements, on ZrO_2 dielectric properties are described. Applications discussed include the use of ZrO_2 in Ge and SiGe nanocrystal-embedded nonvolatile flash memory devices. ZrO_2 films as charge trapping layers in SOZOS (poly-Si/SiO_2/ZrO_2/SiO_2/Si) and TAZOS (TaN/Al_2O_3/ZrO_2/SiO_2/Si) based nonvolatile flash memory stacks, and bipolar, unipolar, and nonpolar ZrO_2-based resistive switching memory devices are also briefly discussed. The impact of electrode materials, metal nanocrystals, metal implantation, metal doping, metal layers, and oxide ion conductor buffer layer on resistive switching properties and switching parameters of emerging ZrO_2-based resistive switching memory devices for high speed, low power, nanoscale, nonvolatile memory devices are briefly reviewed. A roadmap of the applications of ZrO_2 thin film in future low power, nanoscale microelectronic device applications is realized from this review.

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1. Introduction

The rapid progress of complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) technology, since the late 1980s, has enabled the silicon-based microelectronics industry to concurrently meet several technological requirements to fuel market expansion. These requirements include high performance (speed), high reliability, high package density, increased low voltage and low power applications, and multilevel capability (MLC) [1]. The incredible characteristic of transistors that drives the rapid growth of the semiconductor industry is that their speed increases and their cost decreases as their size is reduced. To meet these requirements for future CMOS technology nodes, device scaling has acted as the driving force. CMOS transistor scaling has been the primary factor driving improvements in microprocessor performance. Recently, however interest in nonvolatile memory technology research is increasing rapidly due to a vast number of applications in portable electronic devices which play an important part in our daily life [2,3]. Memory devices are classified into two broad categories based on CMOS technology: volatile and nonvolatile. Fig. 1 is a flow chart classifying semiconductor memory devices [2].

Downsizing of MOSFETs (metal-oxide semiconductor field effect transistors) places stringent demands on the properties of the gate oxide. SiO_2 has dominated the silicon microelectronics industry as the most practical choice for an FET (field effect transistor) gate dielectric material since 1957. SiO_2 offers several crucial advantages such as being highly compatible with silicon technology, a uniform and conformal oxide, high interface quality etc. Industry's acquired information regarding SiO_2 properties and processing techniques over the past several decades makes change difficult. However, further scaling of the FET is eventually going to be impeded by the inability to reduce the oxide thickness below 1.3 nm. For thin SiO_2, the leakage currents from electron tunneling through the dielectrics are a problem.

Amorphous HfO_2 and ZrO_2 with dielectric constants (k) ~20, have been considered for several years as SiO_2 replacement candidates essentially due to their good physical and electrical properties and the fact that they can survive transistor processing [4,5]. For future technology nodes, aggressive scaling to less than 1 nm equivalent oxide thickness (EOT) will require new gate oxides with k values of more than 30 [4]. High-k oxides ($k>50$) are also required for next generation dynamic random access memories (DRAM), where extremely low EOT (0.5 nm) is essential. Indeed, HfO_2 dielectrics are already in production for 45-nm CMOS technology by major IC manufacturers. Some leading companies are also using ZrO_2 as a dielectric material for CMOS applications. One of the most promising candidates for SiO_2 replacement, which is thermodynamically stable with respect to solid state reaction with silicon, is ZrO_2 [6–8]. In addition, it has a large band gap (~5.8 eV) and high dielectric constant (20) [9–14]. As a thin film, ZrO_2 normally condenses on a substrate in crystalline form, but amorphous ZrO_2 thin films are preferred for microelectronic device applications. Grain boundaries in crystalline ZrO_2 thin films can cause undesired increase in leakage current characteristics. Different anisotropic crystalline phases, such as monoclinic, tetragonal, and cubic [12–14], can lead to non-uniformities in k value as a function of film thickness.

A high k value is the first requirement in selecting a material for gate oxide applications. It must be higher than the k (3.9) value of SiO_2, preferably in the range 10–30 [12–30]. Several binary oxides such as Ta_2O_5, Y_2O_3, Al_2O_3, HfO_2, ZrO_2, and TiO_2 [12–30] and also perovskite materials such as $SrTiO_3$ and $(Ba,Sr)TiO_3$ [21–23], have been investigated as oxide dielectric materials for CMOS devices. If the k value of the material is too high, such as for TiO_2 (k~80), fringing

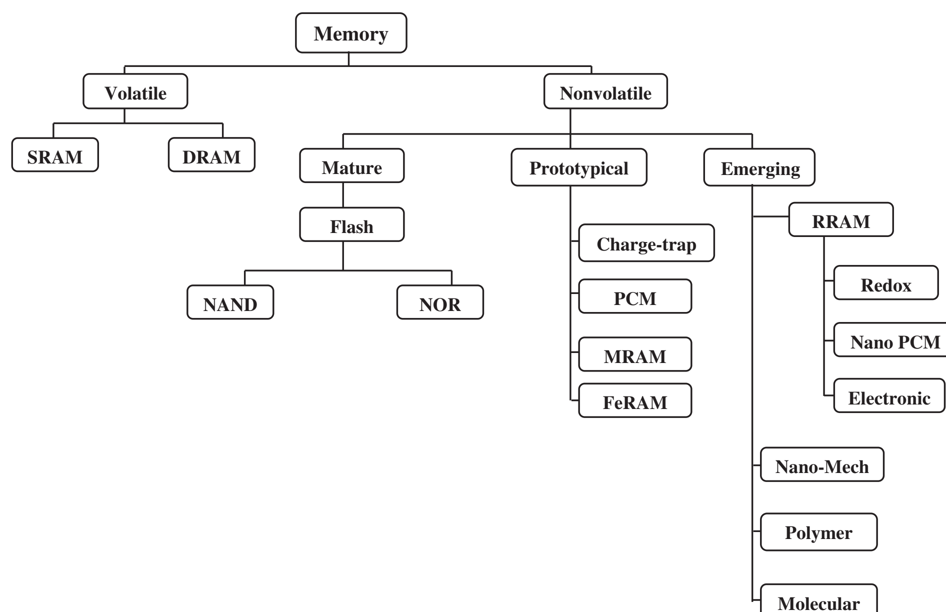
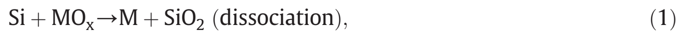


Fig. 1. Classifications of semiconductor memory [2]. SRAM: Static random access memory, DRAM: Dynamic random access memory, PCM: Phase change memory, MRAM: Magnetic random access memory, FeRAM: Ferroelectric random access memory, and RRAM: Resistive random access memory.

fields from the drain through the gate dielectric are observed. The fringing field may degrade the source-to-channel potential barrier yielding poor subthreshold device performance [30].

Among the materials listed above, ZrO_2 has received extensive attention as a candidate material for DRAM capacitor dielectrics due to its high dielectric constant, good thermal stability with Si, wide bandgap and band offsets, and the fact that it is currently used in DRAMs with a design rule below 70 nm [10]. The technological importance of ZrO_2 is enhanced due to its high melting point (2680 °C), good oxidation resistance, high refractive index (2.15–2.18), and low absorption ranging from the near UV (above 240 nm) to the mid IR (below 8 μm) [12–14].

Hubbard and Schlom [24] investigated the thermal stability of several dielectrics contacting Si based upon the Gibbs free energy for silicidation and for dissociation to metals using the equations:



$$Si + MO_x \rightarrow M + SiO_2 \text{ (dissociation)}, \quad (1)$$

$$Si + MO_x \rightarrow MSi_z + SiO_2 \text{ (silicide formation)}. \quad (2)$$

The results show that Ta_2O_5 can dissociate into metallic Ta, whereas TiO_2 forms a silicide at 1000 K. In contrast, these reactions are not favorable for oxides and silicates of Hf and Zr. Thus the primary candidate materials test for alternative gate dielectric applications has been narrowed to HfO_2, ZrO_2 and their silicates due to their excellent electrical properties and high thermal stability in direct contact with Si [25–27]. The interface stabilities and electronic properties of ZrO_2 on Si with a SiO_2 buffer layer were investigated by Fulton et al. [28] with X-ray ($h\upsilon = 1254$ eV) and ultraviolet ($h\upsilon = 21.2$ eV) photoemission spectroscopy. The buffer layers serve to lower the interface state density and to address the higher temperature stability of ZrO_2 in direct contact with Si. An approximately 2 eV ZrO_2/Si(001) band alignment shift was observed after annealing at 600 °C for 5 min in agreement with predictions and other experiments [28]. As-grown films contain excess oxygen resulting in charge transfer from the Si substrate to the internal (ZrO_2/SiO_2) interface, annealing at 600 °C is adequate to desorb the excess oxygen. Decomposition of the oxide to form $ZrSi_2$ was reported after further annealing to 900 °C for 5 min [28].

Efforts are also focused on alternating gate stacks, rather than just gate dielectrics [29]. Among the various high-k materials, ZrO_2 attracts much attention due to its process compatibility, minimization of EOT, moderately high k value (~20), wide band gap (~5.8 eV), barrier height with respect to Si (~1.5 eV), low achievable interface trap density, etc. However, it has three crystalline phases with different dielectric constants; monoclinic (m, k~20), tetragonal (t, k~47), and cubic (k~37), while k is ~22 for the amorphous phase (a-ZrO_2) [12–14]. ZrO_2 material properties have been reviewed by Wong and Cheong [30]. The valence electron state of amorphous ZrO_2 is more stable than those of other binary oxides making it of interest for resistive switching memory (RRAM) applications. Valence electrons play a crucial role in the formation and rupture of conducting filaments consisting of oxygen vacancies during resistive switching. Because of their exceptional properties compared to other dielectric oxides, except that ZrO_2 thin films have gate dielectric and volatile DRAM applications, they are also used in emerging memory device applications such as nonvolatile flash memory and resistive switching memory [31–48].

In this article, we review the primary synthesis techniques for ZrO_2 thin films and the properties of this material as a dielectric layer for volatile DRAM applications. The effect on the dielectric properties of the capacitor structure on different semiconductor substrates, strain compensation substrates, the use of different top and bottom electrodes, and different doping elements are also described together with applications of a-ZrO_2 in nonvolatile embedded nanocrystals and charge trapped flash memory devices. Finally, we briefly survey the prospective application of a-ZrO_2 thin films in resistive switching memory devices for high speed, low power, nanoscale, nonvolatile memory devices including the effect of different electrode materials, metal nanocrystals, metal doping, metal implantation, and buffer layer on the resistive switching properties.

2. ZrO_2 thin film deposition

Thin film deposition techniques for semiconductor device applications are classified into two wide categories, one is a physical route and the other is a chemical route. Simply, in physical vapor deposition, the atoms to be deposited are directly transported from a solid source onto the substrate through a gaseous phase. In chemical deposition processes, the atoms to be deposited are introduced in the form of chemical precursors (volatile liquid compounds) and deposited onto the substrate through the gas or liquid phase. ZrO_2 dielectric thin films are prepared by variety of techniques yielding different thin film properties. In this section, the fabrication, properties, and device applications of a-ZrO_2 thin films are compared for physical and chemical deposition methods.

2.1. Sputter deposition

The most popular ZrO_2 thin film deposition method is sputtering from ZrO_2 or Zr targets. Ramanathan et al. [49] reported the fabrication of 5-nm-thick Zr thin films by ultra high vacuum (UHV) sputtering from a Zr metal target on silicon nitride substrates. Oxidation of polycrystalline Zr metal was then performed in situ using ultraviolet (UV), from an Hg vapor lamp, annealing in oxygen ambient. A plot of oxide thickness with respect to oxidation time for high pressure (590 Torr) Zr oxidation is shown in Fig. 2. A significant amount of polycrystalline ZrO_2 (p-ZrO_2) (~3 nm) is formed almost immediately on exposure to oxygen in the presence of UV light. After 1 h of UV exposure, a 5 nm oxide film is formed at room temperature. The trend of oxidation follows a logarithmic law, consistent with Eley and Wilkinson theory [50]. It is well established that oxidation of Zr proceeds by oxygen migration to the ZrO_2/Zr interface [51]. Oxidation kinetics at low pressure, 80 mTorr, is shown in Fig. 2(b). 2-nm-thick ZrO_2 is formed at low pressure, comparable to the natural air oxidation of Zr. Thus, UV exposure is not very effective for enhancing oxidation rates at such low pressures. The rate of plasma oxidation is much faster than UV ozone oxidation and also follows a logarithmic relationship, as shown in Fig. 2(c). The higher

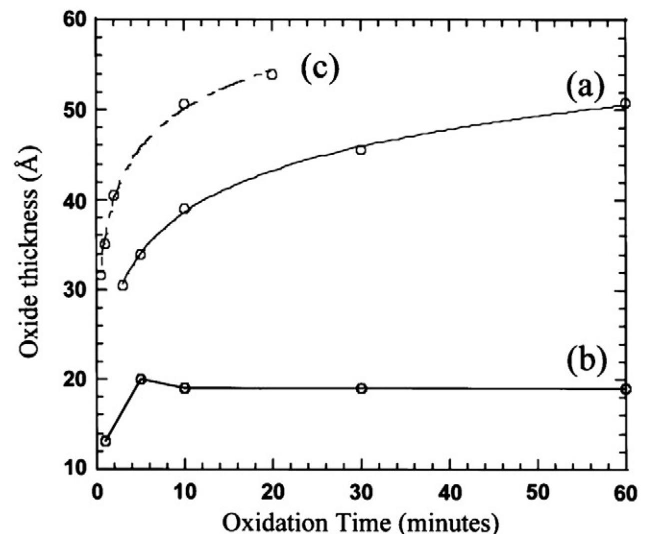


Fig. 2. Oxidation kinetics of Zr films; curve (a) is a logarithmic fit to high-pressure (590 Torr) UV ozone oxidation, (b) corresponds to low-pressure (80 mTorr) oxidation, and (c) is a logarithmic fit to plasma oxidation [49].

rate during plasma oxidation is due to O_2 dissociation in the plasma and O_2^+ collisional dissociation at the sample surface to provide reactive oxygen atoms [49].

ZrO_2 films were also formed by plasma oxidation at room temperature. ZrO_2 thin films with thicknesses ranging from 2.5 to 8 nm were deposited on Si(001) by reactive sputtering [52]. Reactive magnetron sputtering was performed in an Ar^+-O_2 ambient using 2 sccm O_2 flow rate, 40 mTorr total pressure, 300 °C substrate temperature, and 200–400 Watt sputtering power. Prior to Pt electrode deposition, the samples were annealed at 550 °C for 5 min in N_2 ambient. Nam et al. [53] reported the fabrication of a-ZrO_2 thin films by reactive dc magnetron sputtering from a Zr metal target at room temperature (RT) to 400 °C and 100–400 Watt power (ambient: $Ar+O_2$, and process pressure: 6 mTorr). Post deposition annealing (PDA) was performed in O_2 and N_2 mixed gas ambient over the temperature range 450–850 °C prior to Al top electrode deposition. The film crystallinity increased with the increase of deposition temperature. 20-nm-thick ZrO_2 films grown on Si(001) at room temperature were X-ray amorphous, while crystalline peaks of monoclinic and tetragonal ZrO_2 phases were observed in films deposited at 400 °C [53]. The refractive index of reactive dc magnetron sputtered ZrO_2 films grown on Si(001) increased with post deposition annealing (PDA), which also indicated that the films were densified during the PDA processes [53]. A sputtered ZrO_2 gate dielectric based *n*-channel MOSFET has been reported by Ho et al. [54]. We deposited ZrO_2 film by reactive rf magnetron sputtering at 200–300 °C using a ZrO_2 target [35,38,42,44].

Zhou et al. [55] fabricated epitaxial ZrO_2 films with different thicknesses on p-Si(001) by limited reaction dc-sputtering using a Zr metal target and 5 mTorr Ar gas pressure. Infrared lamps were used to heat the substrate during growth. At 400–500 °C growth temperature, polycrystalline ZrO_2 (p-ZrO_2) films were observed. However, at higher growth temperatures (700 °C), crystalline ZrO_2 phases were observed. Fig. 3 shows typical XRD patterns of ZrO_2 films having different thicknesses. At higher thickness (~51 nm), in addition to the tetragonal (002) crystalline phases of ZrO_2, weak tetragonal (200) peaks are also observed. The inset in Fig. 3 is a wider range XRD pattern from a ZrO_2 film with a thickness of 20.4 nm, which clearly shows the (001), (002) and (004) peaks of ZrO_2. As the film thickness is increased from 5 to 20 nm, the (002) peak shifts from 34.08° to 33.69°, as shown in Fig. 3, indicating a gradual increase in in-plane compression in the ZrO_2 film. For 26.3 nm thick layer, the (002) peak is shifted to a higher angle and weakened, and a weak (200) peak appears. Only the (200) peak is observed for films thicker than 51 nm. The phase transition begins at a film thickness between 20 and 26.3 nm [55].

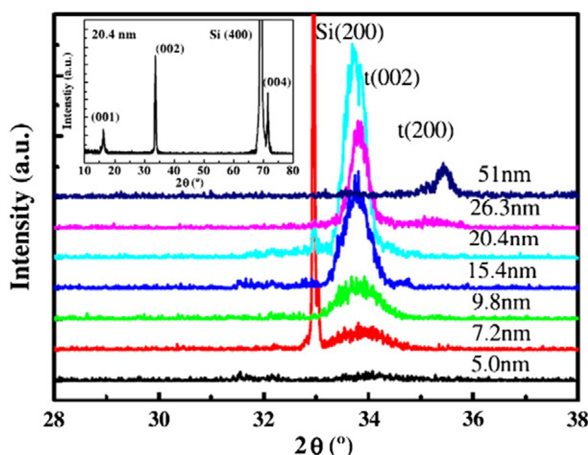


Fig. 3. X-ray diffraction patterns from ZrO_2 films, with different thicknesses, grown at 700 °C on Si(001). Inset shows an XRD scan from a 20.4-nm-thick ZrO_2 film [55].

2.2. Chemical vapor deposition

The advantages of rapid thermal chemical vapor deposition (RTCVD) over other deposition methods such as sputtering from metal and metal oxide targets, plasma-enhanced chemical vapor deposition (PECVD) with organometallic precursors, and molecular beam epitaxy (MBE), are reduced thermal budget and improved control of interfacial properties. The latter is due to rapid thermal ramping and more precise control of the substrate temperature at which precursor gas molecules interact with the surface and form the desired metal oxides. Several groups have used RTCVD [56–58] to deposit a-ZrO_2.

Chang et al. [59,60] reported the fabrication of stoichiometric, uniform, amorphous, and thermally stable (up to 750 °C) a-ZrO_2 dielectric films on Si(001) by RTCVD using a zirconium (IV) t-butoxide $Zr(OC_4H_9)_4$ precursor with oxygen. Capacitors showed low leakage current and excellent *C–V* response with negligible *C–V* hysteresis, which is ideal for charge storage in DRAM. Black et al. [61] deposited a-ZrO_2 thin films by liquid injection metal-organic chemical vapor deposition (MOCVD) using ansa-metallocene zirconium $(Cp_2CMe_2)ZrMe_2$ and $(Cp_2CMe_2)ZrMe(OMe)$ [C_p = cyclopentadienyl (C_2H_5)] precursors. Evaporated Al was used as a gate electrode. ZrO_2 was also deposited by MOCVD using the Cp-based Zr precursor $(MeCp)_2ZrMe(OMe)$ by the same group [62].

2.3. Atomic layer deposition

The atomic layer deposition (ALD) method is one of the sophisticated deposition techniques for well-controlled thin film deposition. ALD can be divided into two types: 1) atomic layer chemical vapor deposition (ALCVD) and 2) plasma-enhanced atomic layer deposition (PEALD). ALD has many advantages over other deposition methods including excellent thickness uniformity over large substrate area (conformality) and precise thickness control [63–66]. In ALD, film growth is dependent on surface saturation reactions, and the film thickness is controlled by the number of deposition cycles [66,67]. Each surface reaction cycle deposits a partial monolayer of the material on the substrate [66,68].

ALD grown polycrystalline ZrO_2 film with a high dielectric constant (~40), on sputter deposited polycrystalline TiN, using Tetrakis(ethylmethylamido)zirconium [$Zr(NEtMe)_4$] and O_3 has been investigated by Kim and Hwang [21]. The dielectric constant strongly depended on the crystallinity of the film [18]. ZrO_2 gate dielectric layers have been reported using PEALD with zirconium t-butoxide [$Zr(O\ t\text{-}C_4H_9)_4$] (abbreviated as ZTB) as the Zr precursor [66]. Evaporated 100-nm-thick Pt was used as the top electrode. Structural and electrical properties of ALCVD grown ZrO_2 dielectric gate stack structures have been reported by Perkins et al. [11]. The deposition was performed at 300 °C using $ZrCl_4$ and H_2O precursors. For electrical characterizations, an Al/TiN top electrode was deposited by CVD. The cyclopentadienyl-based Zr precursor $(MeCp)_2ZrMe(OBu^t)$ has also been used for the deposition of ZrO_2 thin films by the liquid injection ALD method [62].

ZrO_2 films grown by ALD at 325 °C using ZrI_4 and H_2O_2/H_2O are textured tetragonal and cubic ZrO_2 polymorphs [69]. The thinnest films (3–5 nm) grown at 272 °C were X-ray amorphous. Rechargeable oxide trap density and the unit cell volume decreased with increasing growth temperature from 272 to 325 °C. However, while an enhancement in material quality (i.e., less impurity, fewer traps, and better stoichiometry) was reported, the related permittivity and effective capacitance values in $Hg/ZrO_2/Si(001)$ capacitors decreased with increasing growth temperature. This is due to the formation of interfacial SiO_2 or silicate layer between ZrO_2 and Si(001) during film growth at elevated temperature. Interface layer thickness in ALD films grown at 325 °C exceeded that in films grown at 272 °C by approximately 0.7–1 nm. Lower effective capacitance values and noticeably increased hysteresis in the capacitance–voltage curves happened for growth

temperatures above 325 °C, without any change in crystallographic phases, tetragonal (111) and (202) [69].

2.4. Evaporation

ZrO_2 thin films were grown on p-type Si(001) using reactive molecular-beam epitaxy (MBE). Zirconium was evaporated by electron-beam heating in the presence of molecular oxygen at 300 °C substrate temperature. The samples were annealed at 1000 °C for 10 min in different oxygen partial pressures prior to Pt top electrode deposition [70]. ZrO_2 layers for nonvolatile flash memory devices were deposited by reactive electron-beam evaporation, followed by RTA at 500 °C in N_2 for 30 s [71]. Doped and undoped ZrO_2-based MIM capacitors with TaN/Ta as electrodes were deposited by evaporation [72]. Metal-organic molecular beam epitaxy (MOMBE) was used to grow ZrO_2 dielectric layers on p-type Si(001) substrates using ZTB as a Zr precursor [73,74].

2.5. Chemical solution deposition

Chemical solution deposition (CSD) is a cost effective and highly flexible method that allows for good film quality at moderate annealing temperatures. Generally, it has been used for the deposition of relatively thick (>180 nm) high-*k* layers [75]. However, it is necessary to fabricate ultrathin (<20 nm) films on SiO_x/Si(001) for process compatibility. The thickness of the film is controlled by varying the precursor solution concentration and the number of deposition cycles. Deposition of nanometer-thick ZrO_2 dielectric films by aqueous CSD has been reported [75]. Prior to annealing at 500 °C or higher, heat treatment was performed at 260–480 °C after each deposition cycle [75]. Photo-assisted growth of high quality ZrO_2 thin films on p-Si(001) at low temperatures by sol–gel method has been reported by Yu et al. [76]. Post deposition annealing (PDA) was performed using different exposure times of excimer UV light and oxygen pressure. Improvement in film stoichiometries after UV irradiation was confirmed from Fourier transform infrared spectroscopy (FTIR) analysis. ZrO_2 layers are highly stable against both silicide and silicate formation during UV exposure.

3. Important properties of ZrO_2

From the above discussion of the growth of ZrO_2 thin film by different methods, it can be concluded that ZrO_2 films have three crystalline polymorphs, monoclinic, cubic, and tetragonal along with the amorphous state. It is well known that the dielectric constant (*k*) of ZrO_2 is a function of its crystalline structure. Average static values are 20, 37, and 47 [12,21,77], respectively, for monoclinic, cubic, and tetragonal phases [18,78]. In general, the thermal stability of a-ZrO_2 films was up to 750 °C [59,60]. The *k* value and bandgap of a-ZrO_2 varied from 14 to 25 and 5 to 5.75 eV, respectively [61,79,80]. However, the thermal stability was strongly dependent on the growth process and other physical parameters. The tetragonal and monoclinic phases started to appear above ~500 and ~700 °C, respectively [16,81,82]. The crystalline structures of ALD grown ZrO_2 films on TiN was either tetragonal or cubic [21] with a dielectric constant ~40. The experimental bandgap energies of monoclinic, cubic and tetragonal ZrO_2 varied from 5.16 to 7.09 eV, 6.1 to 7.08 eV, and 5.78 to 6.62 eV, respectively [10,83]. Among all the crystalline structures, monoclinic ZrO_2 was the most stable phase at room temperature [21].

4. Application of ZrO_2 as a dielectric layer

With the increasing number density, and correspondingly small feature sizes, of dynamic random access memory (DRAM) devices, it is becoming increasingly difficult to obtain sufficient cell capacitance to satisfy device refresh requirements [21,84] Many of the materials initially investigated as prospective alternative dielectric layer candidates were inspired by memory capacitor applications and the resultant semiconductor manufacturing tool development infrastructure. The most commonly studied high-*k* gate dielectric candidates are Ta_2O_5, $SrTiO_3$, HfO_2, ZrO_2, and Al_2O_3, which have dielectric constants ranging from 10 to 80, and have been employed mainly due to their maturity in memory capacitor applications [85]. Thin dielectric amorphous films of ZrO_2 and HfO_2 have been intensively investigated as replacements for SiO_2 as the gate dielectric oxide in sub-45 nm CMOS technology [85]. This is due to their relatively high permittivities (k~14–25; for amorphous phase) compared with SiO_2 (k~3.9), large band offsets, large bandgaps and high thermodynamic stability on silicon. ZrO_2 and HfO_2 also have promising applications as capacitor layers in metal–insulator–semiconductor (MIS) and metal–insulator–metal (MIM) DRAM devices [61,79,80].

4.1. Dielectric properties of ZrO_2 film on Si(001)

Dielectric properties and conduction mechanisms of ultrathin RTCVD grown bilayer ZrO_2 films (top 1.9 nm amorphous and bottom 2.5 nm polycrystalline) have been reported by Chang and Lin [60]. Fig. 4(a) shows *C*–*V* characteristics of as-deposited 7.5-nm-thick a-ZrO_2 MOS capacitors on p-Si(001) [Al/ZrO_2/p-Si(001)] with a small hysteresis (<50 mV). The calculated average dielectric constant is ~16, and it varies between 15 and 18 depending upon the processing conditions. A plot of EOT versus physical thickness of the a-ZrO_2 films yields an intercept at essentially zero EOT (0.08 nm) indicating no interfacial SiO_2 formation, as shown in Fig. 4(b). However, due to mixing, interfacial $ZrSi_xO_y$ is formed, as shown in the high resolution transmission electron microscopic (HRTEM) image in Fig. 4(c). Taking into account the interfacial $ZrSi_xO_y$ layer and the physical thicknesses (7.5-nm-thick a-ZrO_2) of the dielectric layers, the dielectric constant of $ZrSi_xO_y$ is 11 and the dielectric constant of ZrO_2 is 21. The calculated flatband voltage is −0.7 eV.

n-MOS transistors using 15-nm-thick a-ZrO_2 and n^+-polysilicon gate electrode were also fabricated and good device turn-on characteristics are shown in Fig. 5. The reduced transconductance (g_m), of the order of 10^{-4} S, is most likely due to the high source and drain contact resistances (R_s and R_d) resulting from incomplete removal of the interfacial $ZrSi_xO_y$ layer with an HF etching process. An approximately 0.3-nm-thick interfacial zirconium silicate layer is responsible for the reduced mobility. This clearly indicates the necessity of more effective ZrO_2 and $ZrSiO_4$ patterning to minimize the device integration difficulties [60]. A sputter deposited ZrO_2-based MIS structure on *n*-Si(001) with an Al top electrode, having an equivalent-oxide thickness (EOT) of ~2.5 nm, has been also reported [86]. Optimized devices showed less than 2×10^{-5} A/cm^2 leakage current density at 1 V accumulation bias, which is lower than SiO_2-based gate dielectric devices with similar EOT. Formation of a 1.7-nm-thick zirconium silicate interfacial layer was confirmed by HRTEM analysis. The interfacial silicate layer was found to play a crucial role in determining the conduction mechanism in the high-*k* MIS structure [86].

Koo et al. [66] measured the leakage current characteristics of a Pt/p-ZrO_2/p-Si(001) MOS capacitor under negative bias as shown in Fig. 6(a). At −1.0 V gate voltage, the leakage currents of ALD-grown p-ZrO_2 films, using ZTB as a zirconium precursor, deposited in oxygen gas (film thickness: 6 nm) and in an oxygen plasma (film thickness: 6.5 nm) were approximately 3.7×10^{-7} and 2.7×10^{-8} A/cm^2, respectively. Sequential times of Zr-precursor, Ar-purge, O_2 gas, and Ar-purge were fixed to be 5 s each except for the O_2 plasma process time which was 10 s. 100 Watt rf power, 250 °C substrate temperature, and 1 Torr process pressure were used [66]. The corresponding extracted EOT at 1 MHz accumulation capacitance were about 2.85 and 3.31 nm for ZrO_2 films deposited with the oxygen gas phase and oxygen plasma ALD, respectively. The low leakage current compared to that of conventional SiO_2 gate

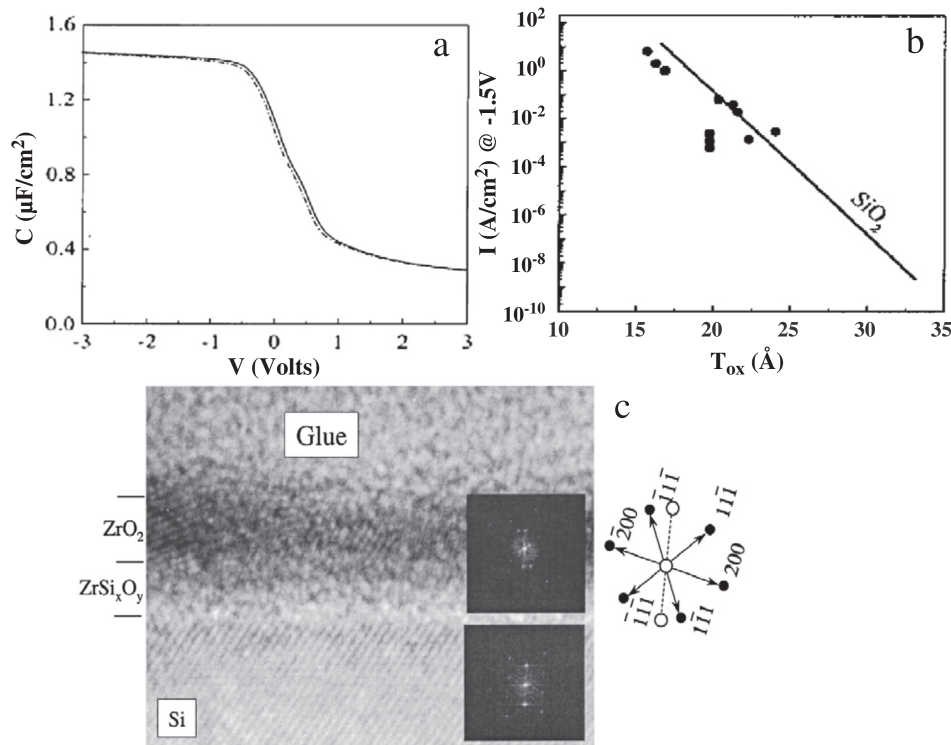


Fig. 4. (a) C–V characteristics of an Al/7.5-nm-ZrO_2/Si capacitor. (b) The leakage current I vs. oxide thickness t_{ox} measured at −1.5 V. The solid line represents the leakage current (I) measured for thermally grown SiO_2 at the same equivalent oxide thickness [60]. (c) HRXTEM image of a $ZrO_2/ZrSi_xO_y$ film stack on crystalline p-type Si(001). The upper selected area electron diffraction pattern is from the $ZrO_2/ZrSi_xO_y$ bilayer, while the lower one is from the Si(001) substrate. The lower part of the ZrO_2 layer is monoclinic polycrystalline while the upper part is amorphous [60].

dielectrics with the same EOT was attributed to the enhanced physical thickness of polycrystalline ZrO_2 (p-ZrO_2) with a higher dielectric constant (~25) and a larger bandgap (7.8 eV). The effective dielectric constants were calculated to be 10.94 for ZrO_2 grown from oxygen ALD and 11.2 for plasma ALD. The low effective dielectric constant, compared to the bulk dielectric constant (25) is due to the effect of the 2–3 nm interfacial Zr-silicate ($ZrSi_xO_y$) layer. Interface state densities were calculated to be 1.16×10^{11} and 5.52×10^{12} eV^{-1} cm^{-2} from the high frequency C–V curves, Fig. 6(b). Due to plasma-induced defects in the film and/or at the interface, the interface density was higher for the plasma ALD layer.

Qi et al. [52] obtained less than 1.1 nm equivalent oxide thickness with 1.93×10^{-3} A/cm² leakage current density at −1.5 V for a Pt/a-ZrO_2/p-Si(001) MOS capacitor. The deposition details are described in Section 2.1. Less than 10^{11} cm^{-2} eV^{-1} interface state density was calculated from the high frequency C–V_G curve shown in Fig. 7(a). No frequency dispersion was observed between 100 kHz and 1 MHz. However, the hump in the C–V curves at ~0 V is due to slow traps. No trap generation was observed during a stress-induced leakage current study. A stress-related 120 mV shift in gate voltage (ΔV_G) has been reported for a 2-nm-thick ALCVD-grown p-ZrO_2 film on p-epi/p$^+$ silicon with an Al/TiN top electrode after 10 successive ±2 V sweeps by Perkins et al. [11]. The process details have been described in Section 2.3. Gate stacks with EOT = 1.3 nm showed leakage values of 10^{-5} A/cm² at a bias of −1 V, which is significantly less than that seen with SiO_2 dielectrics at similar EOT [11]. MOS capacitors of RTCVD grown a-ZrO_2 on p-Si(001), using a ZTB metalorganic precursor [59], showed good inversion with a small but noticeable C–V_G hysteresis (50–100 mV), as shown in Fig. 7(b). The dielectric constant varied from 15 to 18 depending on the deposition conditions. A low leakage current density of 10^{-3} A/cm² at −1.5 V for EOT = 2 nm has been reported. This is a few orders of magnitude lower than that of thermally grown SiO_2 with comparable oxide thickness, as shown in Fig. 7(c) [59].

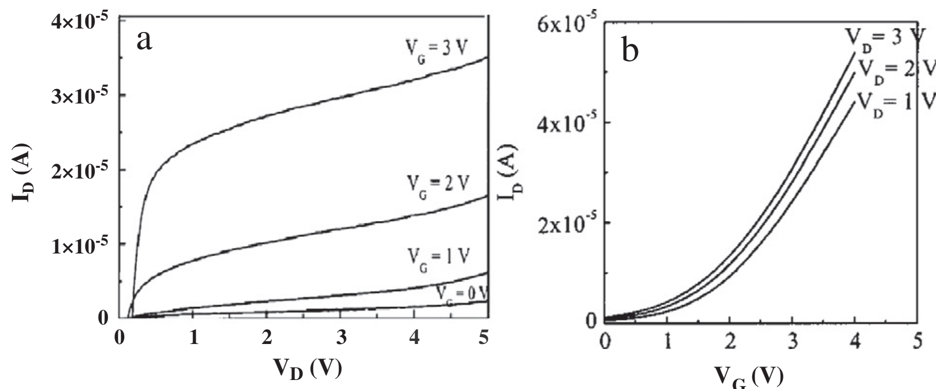


Fig. 5. (a) Drain current (I_D) vs. drain voltage (V_D) for a n^+-poly/15-nm-thick-ZrO_2/p-Si(001) transistor. (b) I_D vs. gate voltage (V_G) curve of the same device [60].

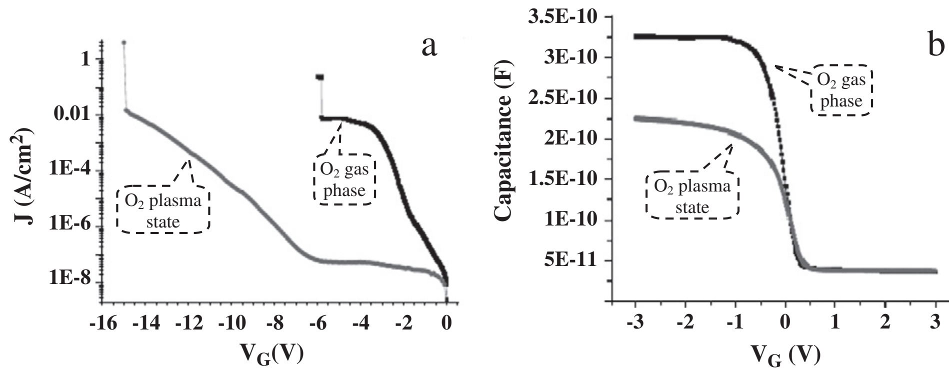


Fig. 6. (a) Leakage current density (J) vs. gate voltage (V_G), and (b) high-frequency capacitance (C) vs. V_G characteristics of a Pt/ZrO_2/p-Si(001) capacitor in which the ZrO_2 layer is deposited in oxygen gas and oxygen plasma [66].

Ramanathan and McIntyre [87] reported severe distortion of C–V curves in both depletion and accumulation regions due to defects in a ultra high vacuum (UHV) sputter deposited p-ZrO_2 based MOS capacitor on an HF treated p-Si(001) substrate (details of the growth process described in Section 2.1 [49]). A detailed study of the interface reactions between sputtered polycrystalline Zr film and Si(001) has been performed by Sun et al. [88]. Generally there is a tendency to form silicate or silicate oxides at the Zr/Si or ZrO_2/Si interface. This can significantly affect the electrical properties of the dielectric layer. The distorted C–V curves noted above were attributed to under-oxidized dielectric layers and interfacial-polarization phenomena [87–89]. Only a small frequency dispersion in accumulation has been reported in 2-nm-thick ZrO_2 film grown on ultrathin (1.1 nm) SiO_2, due to the effects of series resistance arising from a resistive substrate [87,90].

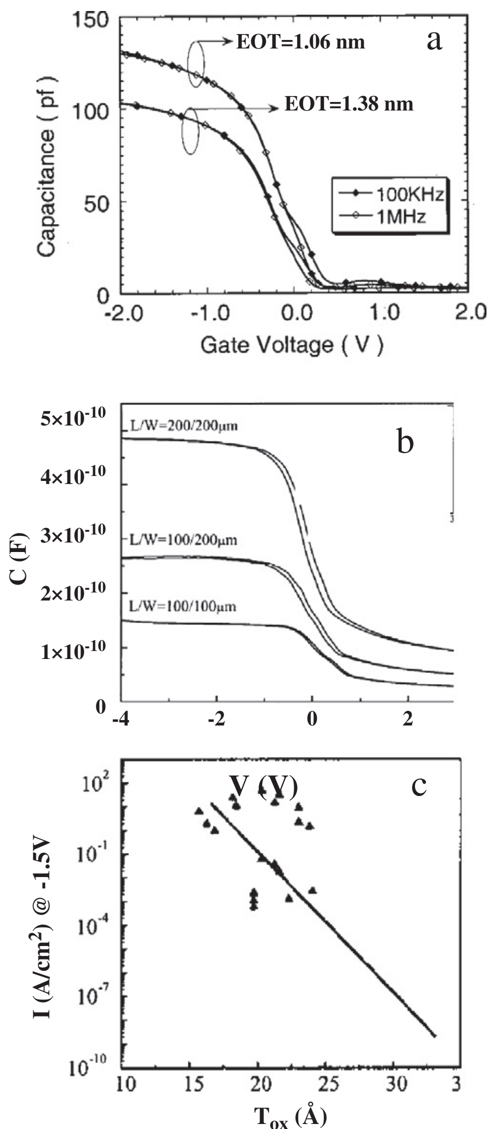


Fig. 7. (a) High frequency C–V characteristics of $Pt/ZrO_2/Si$ structures [50]. (b) C–V responses, and (c) the leakage current I vs. oxide thickness t_{ox} measured at -1.5 V of planar 7.5-nm-thick ZrO_2 based MOS capacitors on Si with Al top electrode [59].

A 1.5 nm equivalent oxide thickness was estimated from the C–V curve. A high dielectric constant (k) of 18–19 with low leakage current density were obtained in MOMBE grown ZrO_2 on p-Si with an Ag top electrode [74]. Dielectric properties of a 4-nm-thick ALD-grown ZrO_2 layer on native oxide (1.2 nm) coated Si(001) have also been reported [91]. After PDA at 700 °C for 5 min in O_2 at atmospheric pressure, multiphase (~with over 90% by volume predominantly tetragonal-ZrO_2 (t-ZrO_2) and monoclinic-ZrO_2 (m-ZrO_2) nanocrystals) and heterogeneous structure evolved. The effective dielectric constant of a $Pt/ZrO_2/SiO_2$/Si(001) MOS capacitor was significantly reduced due to its nanochemistry, although the effective k of the interfacial layer was increased [91].

Of the several advantages of ZrO_2 in gate dielectric applications, such as wide bandgap, suitable dielectric constant, low interface trap density, process compatibility etc., one issue is C–V hysteresis [92–96]. This hysteresis induces a flatband voltage shift, leading to threshold voltage instability, when ZrO_2 is used as a gate dielectric. Such hysteresis phenomenon may be due to chemical contamination from ALD precursors, stress-induced defect formation, or mobile ions [96,97]. Wang et al. was studied this phenomenon and explained it using an inner-interface trapping model for ultrathin (EOT~1.5 nm) ALD grown 5-nm-thick ZrO_2 films using $ZrCl_4$ and H_2O precursors at 300 °C and 1 Torr pressure [96]. A serious charge trapping phenomenon (flatband voltage shift: ~45 mV) has been reported due to the influence of light on charge trapping at the ZrO_2/Zr-silicate interface.

It was proposed that UV irradiation can improve electrical properties leading to a low leakage current density of 8.3×10^{-8} A/cm^2 at 1 MV/cm and a breakdown field larger than 4 MV/cm [76] for chemically grown metastable ZrO_2 (t-ZrO_2 and m-ZrO_2) films on p-Si(001) with an Al gate (growth process is described in Section 2.5). UV (172 nm) irradiation at ~300 °C in 0.75 Torr oxygen pressure for 5 min dramatically reduced the density of positive fixed-oxide charges near the ZrO_2/Si interface, resulting in a low positive charge density of 3.2×10^{10} cm^{-2}. Harasek et al. [98] reported a PDA effect (650 °C to 800 °C for 5 min in forming gas and diluted O_2) on the electrical properties of MOCVD grown ZrO_2 MOS capacitor on p-Si(001) at 450 °C, using $Zr(tfacac)_4$ precursor, with an Al top electrode and an EOT of 2 nm. Interface trap densities (D_{IT}) of

approximately 53×10^{11} cm^{-2} eV^{-1} and a small oxide charge density in combination with a leakage current density of 43×10^{-6} A/cm^2 have been reported for ZrO_2 films having an EOT of 3 nm. An oxidizing atmosphere during the annealing process leads to inferior electrical characteristics with regard to interface trap density, oxide charge, and insulator leakage due to the formation of an increased trap density [98].

4.2. ZrO_2-based MIS structures on strained Si and SiGeC

Strained-Si based MOSFETs are promising candidates for next generation complementary MOS technology [99–101]. In tensile-strained Si layers grown on relaxed-SiGe substrates, mobility enhancements over bulk Si of roughly 60% for holes and 80% for electrons were achievable [99–104]. This corresponds to a considerable performance enhancement over current Si MOS devices; however, strained-Si technology must be compatible with the standard CMOS process. Maiti et al. [99,100] studied the quality of thin low-temperature (150 °C) microwave plasma (700 W, 2.45 GHz) CVD grown high-*k* ZrO_2 films on tensile-strained p-Si(001) on relaxed $Si_{0.91}Ge_{0.09}$ layers at a pressure of 500 mTorr and reported a very low leakage current density of 10^{-7} A/cm^2 at −1 V. The calculated interface state density was comparable with those reported for ZrO_2 films deposited directly on Si(001) using other techniques. The conduction mechanism was found to be dominated by Schottky emission. Bandgap and strain engineered $Si_{1-x-y}Ge_xC_y$ alloys are also attractive for high performance silicon heterostructure devices [101–107]. Chatterjee et al. [101] deposited SiO_2/ZrO_2 film stacks on strained-$Si_{0.91}Ge_{0.09}$/Si(001) layers at low temperature (150 °C, 30 s) by microwave plasma (700 W, 500 mTorr) deposition. An effective dielectric constant of ~13.3 was calculated from the analysis of high frequency *C–V* characteristics of the stacked-gate MIS capacitors. By calculating interface trap charge density from the *C–V* characteristics of as-deposited and 500 °C annealed in pure nitrogen ambient for 30 min samples, ZrO_2 and stacked SiO_2/ZrO_2 samples indicate that the interface quality was improved by introducing an ultrathin SiO_2 layer. However, further improvement was also observed after annealing the samples at 500 °C for 30 min. Mahapatra et al. [103] investigated the interfacial structure and electrical properties of sputtered ZrO_2 films, using a ZrO_2 target, on strain-compensated $Si_{0.69}Ge_{0.3}C_{0.01}$/Si(001) layers with an Al top electrode. A 350 °C substrate temperature, 50 Watt rf power, and a process pressure of 0.2 Torr have been used during 20 minute sputtering. Formation of an ultrathin Zr–Ge-silicate interfacial layer was realized from an HRTEM study. The ZrO_2 layers consist of a top p-ZrO_2 film with a thickness of ~8.5 nm and an a-ZrO_2 interfacial layer with a thickness of ~3.6 nm. A low leakage current of ~9×10^{-8} A/cm^2 at −1.0 V gate voltage, a high breakdown field of 7 MV/cm, and a moderate interface state density of 6×10^{11} cm^{-2} eV^{-1} were observed in the stacked dielectric films with an EOT of ~1.9 nm for this mixed ZrO_2 with a 2 nm interfacial silicate layer. High dielectric constants of ~17.5 for ZrO_2 and ~7.0 for the interfacial silicate layer were calculated from the *C–V* analysis.

4.3. ZrO_2-based MIS structure on III–V semiconductors

The understanding of III–V MOSFETs requires gate dielectrics that allow for low gate leakage currents and a low density of interface states. A primary challenge in the growth of high-quality III–V/dielectric interfaces is that even sub-monolayer coverages of oxygen pin the Fermi level of the III–V semiconductor [108,109]. Moreover, native III–V oxides cause interface instability, which must be minimized before and during dielectric deposition [108,109]. Engel-Herbert et al. [109] reported the properties of CBD grown ZrO_2 MOS capacitors, using a zirconium tert-butoxide [$Zr(OC(CH_3)_3)_4$] metalorganic precursor at 225 and 470 °C (15 to 60 min) without using any carrier gas or additional oxidant, on in situ arsenic (As) capped $In_{0.53}$ $Ga_{0.47}As$(001) substrate. Pt, Mo, or Ta metal gates are evaporated with areas from 7.8×10^{-5} to 4.9×10^{-4} cm^2 through a shadow mask for MOS capacitive structures. Low frequency dispersion (<2%), an accumulation capacitance and horizontal position of the *CV* curve with temperature independent, shifted flatband voltages with metal gate work function, and surface potential responded with the applied gate voltage were observed in the optimized 30-nm-thick ZrO_2 based III–V MOSFETs with a Pt gate electrode. Strongly temperature dependent inversion capacitance was also noticed [109].

4.4. MIM capacitor based on ZrO_2

In terms of the bottom electrode, highly doped poly-Si is typically used in DRAM capacitors. However, it easily reacted with high-*k* dielectric materials and generated thick interfacial oxides having low dielectric constants [110,111]. Thus, MIM capacitors using different metals, such as Pt, Ru, Ta, and W as bottom electrodes, have been considered for future capacitor structures [111,112]. MIM capacitors of ALD grown t-ZrO_2 on W/TiN/SiO_2/Si(001) with a Pt top electrode have been reported by Lee et al. [111]. 50-nm-thick W was also grown by ALD. 11–11.5 nm t-ZrO_2 was deposited at 300 °C using $ZrCl_4$ and H_2O precursors. Both the precursors were pulsed for 2 s and N_2 purging followed for 30 or 60 s after H_2O or $ZrCl_4$ pulsing, respectively. A thin interfacial amorphous layer of thickness of 1.3 to 1.4 nm was detected between the t-ZrO_2 and W layers. EOT of 2–2.1 nm and the effective dielectric constant (22–25) of the dielectric capacitor, including the contribution of interfacial WO_x layer have been reported [111].

Dielectric constants of around 26 and 24 for PLD (KrF excimer laser, 248 nm wavelength) grown a-ZrO_2 films deposited in N_2 and O_2 ambient, respectively, with Pt top and bottom electrode have been reported [113]. Laser repetition rate of 5 Hz, 30 ns pulse width, energy density of 1.8 J/cm^2, 300 to 700 °C substrate temperatures, and 0.15 Torr process pressure were used during a-ZrO_2 film deposition. The film deposited in N_2 ambient had better frequency stability, smaller dielectric loss, and a smoother surface than the film deposited in O_2 ambient. Lower EOT of 1.38 nm and leakage current density of 94.6×10^{-3} A/cm^2 were observed for the films deposited in N_2 ambient. This indicated that the dielectric property of the a-ZrO_2 films was improved by nitrogen incorporation [113].

A high dielectric constant of ~40 was observed for ALD grown ZrO_2 on TiN at 250 °C growth temperature using $Zr(NEtMe)_4$ and O_3 sources [21]. The crystalline structures of this ALD grown ZrO_2 films was either tetragonal or cubic. Kim et al. [114] also reported that the leakage current and capacitance were decreased with increasing ZrO_2 thickness grown by ALD with TiN top and bottom electrodes (TZT). $Zr[N(CH_3)C_2H_5]_4$ and O_3 precursors were used during growth process of ZrO_2 film at 225 °C, 250 °C, and 275 °C. ZrO_2 films deposited at 225 °C and 250 °C were amorphous, while the films deposited at 275 °C were partially crystalline and at 300 °C the films were completely crystalline. The as-deposited a-ZrO_2 layer became crystalline during PDA (400 °C, 1 min in N_2) and/or top electrode formation at >400 °C temperature. Low leakage current density (<10^{-8} A/cm^2) with high dielectric constant (~43) were calculated for 8-nm-thick crystalline ZrO_2 film deposited at 275 °C [114].

The influence of electrode roughness on the leakage current in TiN/ZrO_2/TiN capacitors having t-ZrO_2 thicknesses of 10 and 7 nm, corresponding to EOTs between 1.0 and 0.7 nm (assuming a permittivity of 40 for t-ZrO_2), has been studied by Jegert et al. [115] using a microscopic transport model. Tunneling transport in the dielectric bandgap was treated which incorporating defect-assisted transport mechanisms. Small electrode roughness does not influence the leakage current significantly; however, thickness fluctuations have an important impact on the dielectric properties. For thinner films, the transport mechanism transformed from Poole–Frenkel (P–F) conduction to trap-assisted tunneling. As a result, the sensitivity of the leakage current on electrode roughness dramatically increased upon downscaling [115].

Jegert et al. [116] also studied leakage currents using kinetic Monte Carlo (kMC) simulation of TZT capacitors with a t-ZrO_2 dielectric. The transport model of a typical TZT capacitor with a *k* value of 38 is shown in Fig. 8. Defect density was assumed to be $N_D = 3 \times 10^{18}$ cm^{-3}. For a TZT capacitor having an oxide thickness of 9 nm, the leakage current was dominated by P–F emission of electrons from positively charged defects at a donor level depth $E_D = 1.15$ eV with respect to the ZrO_2 conduction band, at less than 2.5 V. Electrons are injected from the TiN cathode into the defects through multi-phonon assisted and elastic tunneling. In the next step, de-trapping occurred via P–F emission into the t-ZrO_2 conduction band, where the electrons rapidly flowed to the anode [116]. Thermally-activated de-trapping of electrons was the transport limiting step in this multistep process. During injection steps for kMC simulations, a conduction band offset (E_B) between TiN and t-ZrO_2 of 1.74 eV was extracted. Therefore, the defect level laid well above the electrode Fermi level. For applied voltage > 2.5 V, at lower temperatures ($T \leq 50$ °C), an increase of the slope of current–voltage curves was observed together with a reduced temperature scaling. Here, trap-assisted tunneling (TAT) was dominant. At high voltages when the shape of this barrier changes from trapezoidal to triangular (see Fig. 8), the de-trapping rate increases with the applied voltage, so that it finally exceeds the rate for P–F emission [116]. The increased slope was explained by the stronger voltage dependence of the weak temperature dependence of TAT. The P–F emission rate is higher than that for TAT over the entire voltage range so that PF emission dominates the leakage current for $T \geq 90$ °C.

4.5. Stacked ZrO_2–Al_2O_3-based MIM capacitors

As the minimum feature size of DRAM shrinks, high-*k* dielectric materials have been investigated to find an alternative for Al_2O_3 as a dielectric in MIM capacitors with TiN electrodes. EOT lower than 0.9 nm will be required to obtain 25 fF/cell with a 1.3 μm high cylindrical capacitor structure. It was discussed above that quite different phases of ZrO_2 have different dielectric constants. However, the high dielectric constant phases of ZrO_2 are unstable [117]. ZrO_2 MIM capacitors with TiN electrodes cannot be easily used due to high leakage current, particularly, in negative bias. To solve these issues in DRAM, a different capacitive structure was introduced. A dielectric film stack of ZrO_2–Al_2O_3–ZrO_2 (ZAZ) with TiN top and bottom electrodes was one of the most attractive ZrO_2–Al_2O_3 laminate structures [117]. The ZrO_2 and Al_2O_3 dielectric films were deposited by ALD using $Zr(N(CH_3)C_2H_5)_4$-ozone and $Al(CH_3)_3$-ozone precursors, respectively, at 300 °C. Both ZAZ and AZA (Al_2O_3–t-ZrO_2–Al_2O_3) structures decrease capacitance from 42.8 fF/cell to 29.4, and 30.6 fF/cell by 30% and effectively suppressed leakage current from 1.6 fA/cell to 0.18, and 0.10 fA/cell, respectively, as shown in Fig. 9.

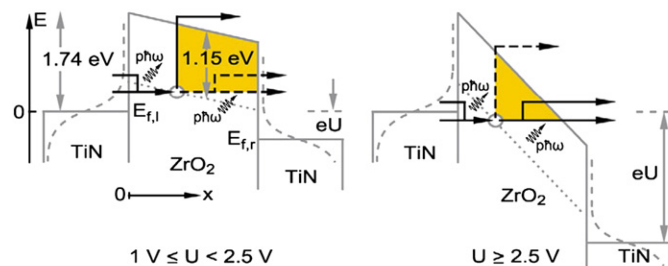


Fig. 8. Schematic band structure of a TiN/ZrO_2/TiN (TZT) capacitor for low (left side) and high (right side) voltages. Arrows illustrate electron flow, while a dashed arrow indicates a slower electron emission path. Barriers for tunnel emission are highlighted with color. U is the applied voltage [116].

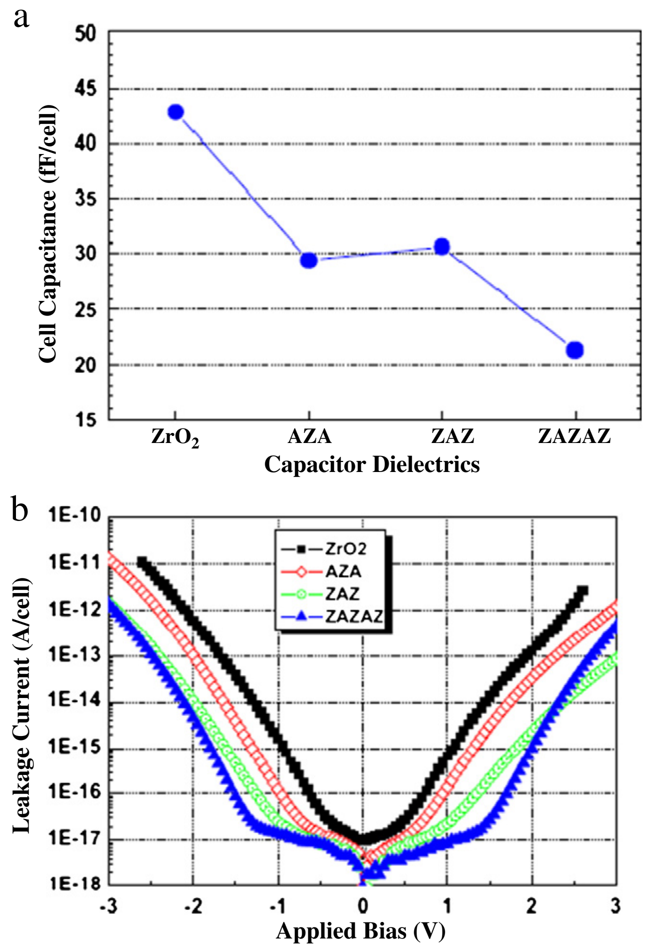


Fig. 9. Variation of (a) cell capacitance, and (b) leakage current with different ZrO_2-Al_2O_3 film stacks. AZA = Al_2O_3/ZrO_2/Al_2O_3; ZAZ = ZrO_2/Al_2O_3/ZrO_2; and ZAZAZ = ZrO_2/Al_2O_3/ZrO_2/Al_2O_3/ZrO_2 [117].

The lowest leakage current density of 0.05 fA/cell is observed in ZAZAZ (a-ZrO_2–Al_2O_3–a-ZrO_2–Al_2O_3–t-ZrO_2) film stacks, as shown in Fig. 9(b). But ZAZAZ film stacks showed 30% lower cell capacitance than AZA or ZAZ due to a lower dielectric constant. With respect to capacitance and leakage current, the ZAZ stack acts as a best capacitor dielectric [117].

Electrical properties of ALD grown Al_2O_3-doped ZrO_2 dielectric thin films in three-dimensional MIM capacitors with TiN top and bottom electrodes have been reported by Zhou et al. [118] by means of *I–V* and constant voltage stress measurements. ZrO_2 and Al_2O_3 were deposited by ALD at 275 °C using the precursors described above in this section. Three different film stacks have been studied. The first one is a 6-nm-thick amorphous $ZrAl_xO_y$ layer ($k = \sim 24$), in which 30-at.% Al_2O_3 contained. The second one is crystalline ZAZ ($k = 40$), in which crystalline-ZrO_2 was symmetrically inserted of a monolayer of Al_2O_3 to form a 5.2-nm-ZrO_2/0.35-nm-Al_2O_3/5.2-nm-ZrO_2 sandwich structure. In the third sample, asymmetric ZAZ ($k = 35$), a ~0.35-nm-thick Al_2O_3 layer was inserted between the ~5.5 nm lower crystalline ZrO_2 layer and the ~2.2-nm-thick upper crystalline ZrO_2 layer, forming a crystalline-ZrO_2/amorphous-Al_2O_3/amorphous-ZrO_2 laminate structure. Higher leakage current at positive gate bias and pronounced barrier lowering at negative polarity were observed in the amorphous $ZrAl_xO_y$. These phenomena are due to the creation of more oxygen vacancies at the bottom interface by incorporating nitrogen into the a-ZrO_2 layer. Higher leakage current at negative bias for the crystalline films is due to the formation of a TiO_2 layer at the bottom interface with TiN yielding a band-offset asymmetry.

A power-law model is appropriate for lifetime extrapolation of amorphous $ZrAl_xO_y$ over a voltage stress time of 10^{-1} and 10^6 s. Both symmetric and asymmetric ZrO_2–Al_2O_3–ZrO_2 stacks follow a thermo-chemical bond-breakage model and demonstrate more field acceleration of lifetime for positive bias on top electrode [118]. Reliability of the ZAZ sandwich stack is dominated by the crystalline ZrO_2 layer. Clear differences between their *I*–*V* asymmetry and breakdown behavior were correlated with the differences in compositional variation of the bottom interface, defect density, and conduction mechanism of the film stacks. All three film stacks achieve the leakage criteria of 1 fA/cell (at ±1.0 V) and a reliability specification of ten years for DRAM storage capacitor applications.

4.6. Carrier mobility of ZrO_2 gate dielectrics

The effective mobility of ZrO_2-gate-dielectric based MOSFETs (μ_{eff}) can be written as [54,119]

$$\mu_{eff} = \frac{LI_D(V_G)}{WV_{DS}Q_{INV}(V_G)}, \quad (3)$$

where L is the channel length, W is the channel width, I_D is the drain current, V_G is gate voltage, V_{DS} is drain to source voltage, and Q_{INV} is the inversion charge density which was extracted by measuring the gate-channel capacitance C_{GC} as a function of gate voltage V_g [54,120]. Q_{INV} is given by

$$Q_{INV} = \int_{-\infty}^{V_G} C_{GC}(V_G)dV_G. \quad (4)$$

The effective normal field E_{eff} can be written in terms of the depletion charge density (Q_d) and the inversion charge density [54,119,121,122] as

$$E_{eff} = (|Q_d| + |Q_{INV}|)/\varepsilon_{Si}, \quad (5)$$

where $|Q_d|+|Q_{INV}|$ is the total charge inside a Gaussian surface through the middle of the Si inversion layer. The effective electron mobility of a ZrO_2-gated *n*-MOSFET as a function of effective electric field at different temperatures is shown in Fig. 10. The electron mobility of ZrO_2 gated transistors does not increase linearly with decreasing temperature from 300 to 11 K.

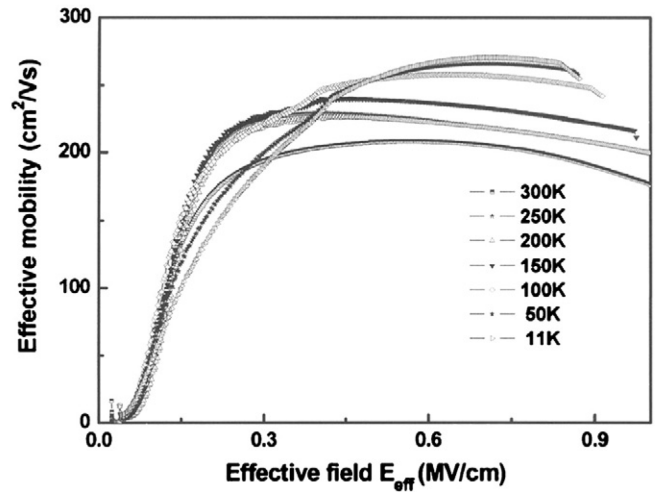


Fig. 10. A plot of effective electron mobility for ZrO_2 gated nMOSFETs as a function of effective electrical field (E_{eff}) in the temperature range from 11 to 300 K [54].

4.7. Impact of doping on dielectric properties

Recently, tetragonal and cubic phases of HfO_2 and ZrO_2 have drawn intense interest because their *k* values are much higher than those is the corresponding amorphous phases. However, tetragonal and cubic phases of ZrO_2 are only stable above 1170 and 2297 °C, respectively, which is not suitable in ultra large scale integration (ULSI) technology [12,72,123]. Doping with Si, Ce, or Ge [72,124] can lower these stabilization temperatures. Wu et al. [72] reported that a Ge-stabilized t-ZrO_2 dielectric with a permittivity of 36.5 was obtained by rapid thermal annealing of a ZrO_2/Ge/ZrO_2 (ZGZ) laminate structure at 500 °C for 30 s. A 5.5/0.6/5.5-nm-thick ZGZ laminate structure was grown by PVD on TaN/Ta/SiO_2/p-Si(001) as an insulator followed by 400 °C O_2 furnace annealing for 10 min. MIM capacitors with t-ZrO_2 layers have a high capacitance density of 27.8 fF/μm^2 and unacceptably high leakage current [72]. By capping an amorphous La-doped ZrO_2 layer, with a *k* value of 26.3, high-performance MIM capacitors have been reported with a capacitance density of 19.8 fF/μm^2, a leakage current of 6.5×10^{-8} A/cm^2 at −1 V, and a satisfactory capacitance shift of 1.21% after ten years [72]. Ozone-based ALD grown monoclinic La-doped ZrO_2 thin films deposited on Ge(001), using $(iPrCp)_3La$ and $[(MeCp)_2(ZrMe)OMe]$ precursors, showed a dielectric constant of 29 [125]. After annealing at 400 °C in N_2, a high *k* value more than 40 was observed due to a Ge-induced formation and stabilization of cubic or tetragonal-ZrO_2 phases [125]. Ge-doped ZrO_2 thin films were prepared at low growth temperatures (225–360 °C) on SiON/Si(001) substrates by atomic oxygen beam deposition of Zr and Ge [126]. Pure tetragonal zirconia phase films were prepared which were stable after N_2 annealing at 1050 °C. The dielectric constant and EOT show pronounced correlation with the Ge concentration in the oxide film, as shown in Fig. 11. The dielectric constant was increased with increased Ge doping to a maximum value of 37.7, for a 6.2-at.% Ge sample grown at 225 °C. The enhancement in dielectric permittivity upon doping was attributed to an increase in the ZrO_2 tetragonal distortion [125]. The EOT decreases with increased Ge content up to 6.2-at.% and then increases as shown in Fig. 11.

Early-stage doping effects on high-temperature stabilization and dielectric properties were systematically compared by Lee et al. [127], after a low-temperature annealing process (400 °C), for sol–gel derived ZrO_2 films, doped with ~13-at.% Y, Gd, Dy, or Ce on p-Si(001) with an Al top electrode. The doped-ZrO_2 films were deposited using acetic acid (CH_3CO_2H) and 2-methoxyethanol ($CH_3OCH_2CH_2OH$) solvents, and the following metal-based nitrate hydrates were used as metallic components: zirconyl nitrate hydrate [$ZrO(NO_3)_2.xH_2O$], yttrium nitrate hexahydrate [$Y(NO_3)_3.6H_2O$], gadolinium nitrate hexahydrate [$Gd(NO_3)_3.6H_2O$], dysprosium nitrate hydrate [$Dy(NO_3)_3.xH_2O$], and cerium nitrate hexahydrate [$Ce(NO_3)_3.6H_2O$]. The doped ZrO_2 films consist of mixed monoclinic and tetragonal/cubic phases. *C*–*V* curves measured at a frequency of 100 kHz as a function of the dopant species are shown in Fig. 12(a) and the extracted dielectric constant together with amount of hysteresis are shown in Fig. 12(b). The dielectric constant for sol–gel deposited pure ZrO_2 films was ~20. The dielectric constant was slightly lower, 16–18, when Y, Gd, and Dy atoms were added to the ZrO_2 film due to the retardation of the tetragonal/cubic phase formation and/or decreased crystallinity. However, the dielectric constant is significantly increased up to ~26 upon Ce doping, which was explained by Ce–O bond formation, densification, and tetragonal/cubic phase formation. The dielectric constant of Ce-doped ZrO_2 films increased without hindering the stabilization of the high temperature phase and degrading the hysteresis characteristics [127]. Ozone-based ALD La-doped ZrO_2 thin films grown on Ge(001) have a dielectric constant of 29. After annealing at 400 °C in N_2, a high *k* value of more than 40 was observed due to Ge-induced stabilization [125].

5. Application in nonvolatile flash memory

Amorphous ZrO_2 dielectric material is also used as a charge trapping layer in flash memory devices. On a Si(001) substrate, Ge-based nonvolatile memory devices with evaporated 10.1-nm-thick ZrO_2 as a charge trapping layer and 3 nm thermally grown GeO_2 as a tunnel dielectric

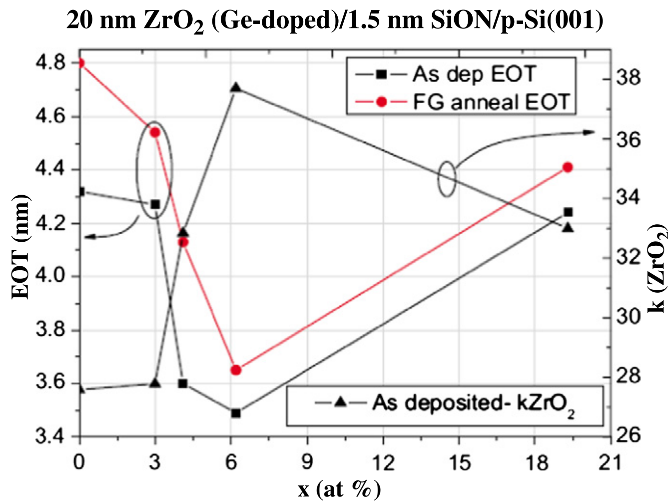


Fig. 11. EOT and k values determined for ZrO_2 as a function of Ge doping concentration x. Results are shown for as-deposited and forming gas (FG) annealed samples [126].

followed by a rapid N_2 annealing at 500–550 °C for 60 s have been reported [72]. Evaporated 14.5-nm-thick a-Al_2O_3 and Al were used as a blocking layer and gate electrode, respectively. A 1.8 V memory window at ±5 V program/erase (P/E) for 1 ms was achieved due to the crystalline ZrO_2 trapping layer which provides a high permittivity of 36.8 with a large amount of trapping sites. Negligible memory window degradation was reported after 10^5 P/E cycles of ±5 V gate pulses for 1 ms. Good retention characteristics, with 30% charge loss after a 10 years operation at 85 °C, also confirmed the eligibility of GeO_2 as a tunnel dielectric and ZrO_2 as a trapping layer [72].

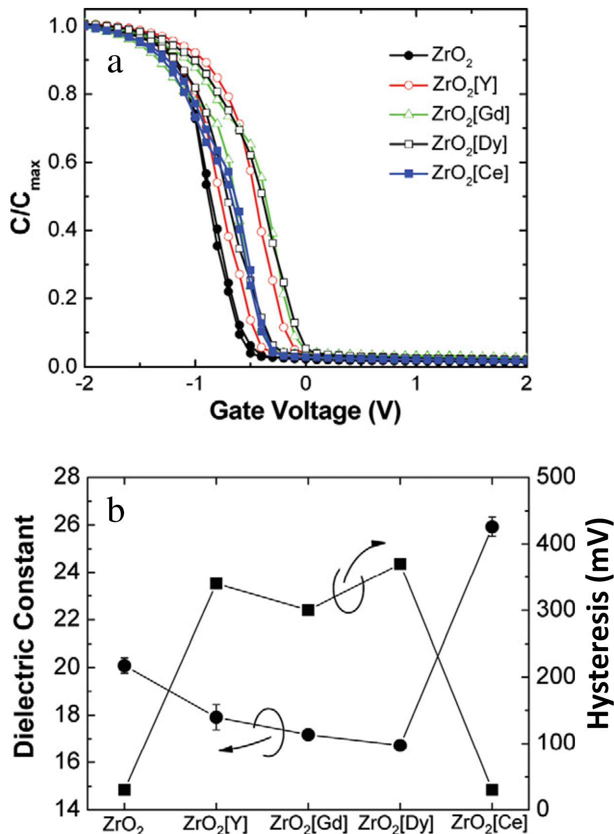


Fig. 12. (a) C–V curves for sol–gel deposited ZrO_2 films, as a function of the doping species, measured at a frequency of 100 kHz. The dopant concentration was 13-at.%. (b) The extracted dielectric constant and the amount of hysteresis in the ZrO_2 films as a function of doping species [127].

Lee et al. [32] reported the fabrication of flash memory structures consisting of Ge nanocrystals (NCs), prepared by ion implantation, embedded in ALD grown 20-nm-thick a-ZrO_2 on p-Si(001), using Tetrakis Ethyl Methyl Amino Zirconium and O_3 precursors at 340 °C. The Ge-ion-implanted a-ZrO_2 gate material in the MOS capacitors was annealed in N_2 gas ambient for 10 min at 800 °C, and evaporated Ti/Au was used as the top electrode. C–V curves of an MOS capacitor embedded with Ge NCs (size: 5 nm) exhibited a 3 V memory window at ±9 V bias, whereas a negligible memory window was observed at the same voltage range for MOS capacitors without Ge NCs. This indicated the presence of charge storage in the Ge NCs which was confirmed by the observed counter-clockwise hysteresis in the C–V curves. White light illumination significantly influenced the flat band voltage shifts. Under forward bias, from 0 to 5 V, with illumination, the current was larger than that obtained in the dark at the same bias voltage [32]. Such positive photoconductivity indicates that the photoionized electrons participate actively in the conduction mechanism rather than forming positively charged NCs. The memory window under illumination is larger and the CV curve, as well as the flat band voltage (V_{FB}), shifts more than that obtained in the dark. A significant positive shift in V_{FB} can be explained by the trapping of photoionized electrons in the Ge NCs. The ZrO_2-based MOS capacitors with embedded Ge NCs showed a capacitance decay of only 4.63% after 10^5 s [32]. Kim et al. [128] investigated charge retention characteristics of SiGe NCs (size: ~6 nm) embedded in an RTCVD grown a-ZrO_2 (using zirconium tertiary-butoxide precursor) MIS memory capacitor. With a thin ZrO_2 tunneling oxide (EOT~6 nm), and self-assembled SiGe NCs, a low write voltage was achieved. Discharge from the SiGe NCs was due to the direct tunneling of electrons through the ZrO_2. A lower charge loss rate was observed for ZrO_2-based SiGe NC embedded devices compared to SiO_2-based devices.

Hsu et al. [47] fabricated poly-Si/SiO_2/ZrO_2/SiO_2/p-Si(001) (SOZOS) memory structures using spin-coated a-ZrO_2 as a charge trapping layer. The starting solution was prepared by dissolving $ZrCl_4$ in isopropanol (IPA) under vigorous stirring in an ice bath. A 2.7 V threshold voltage shift from the drain current vs. gate voltage (I_d–V_g) curve was observed due to charge trapping in the a-ZrO_2 layer of the SOZOS memory device. Fast program/erase speed of 0.1 ms, good data retention up to 10^4 s, only a 5% charge loss due to deep trapping in the a-ZrO_2 layer, and good endurance for more than 10^5 P/E cycles have been reported. Replacing the Si_3N_4 charge trapping layer in a TANOS (TaN/Al_2O_3/Si_3N_4/SiO_2/Si) structure by an ALD grown polycrystalline (cubic/tetragonal) ZrO_2 layer, TAZOS (TaN/Al_2O_3/ZrO_2/SiO_2/Si) based nonvolatile flash memory stacks have been demonstrated by Congedo et al. [129]. $MeCp_2ZrMe(OMe)$ and tri-methyl aluminum (TMA) were used as Zr and Al precursors with O_3 as oxygen source at 300 °C to deposit ZrO_2/Al_2O_3 layers on 4.5-nm-thick tunnel-SiO_2/p-Si(001). The high dielectric value of ZrO_2 (~30), acceptable thermal stability suitable for high processing temperatures, and efficient program/erase performance compared to Si_3N_4 for the same EOT and PDA conditions support studying ZrO_2 for replacing Si_3N_4 in low voltage charge trapping flash memory applications. Annealing temperature is a key factor in this structure controlling device performance. PDA of 900 °C in N_2 ambient ensures superior thermal stability of the structure, but is not sufficient to provide acceptable performance, in particular in terms of erase. PDA at 1030 °C is essential for optimizing the program/erase efficiency of the stack, due to enhanced blocking oxide quality and/or modification in trap distribution, but degrades retention [129].

6. ZrO_2 based resistive switching memory

ZrO_2 has attracted extensive attention for its application in resistance random access memory (RRAM) devices which have prospective advantages such as simplicity, high integration density, low operating power, and nondestructive readout [31–45,130–162]. In this section we briefly review the effect of electrode material, metal doping, metal

implantations, embedded metal layers, metal nanocrystals, and buffer layer on the resistive switching properties of ZrO_2 film.

6.1. Effect of electrode material

Use of ZrO_2 for resistive switching (RS) device applications was first proposed by Lee et al. in 2005 [33]. Most of the reports on ZrO_2-based devices were fabricated from sputter deposited ZrO_2 thin films. Different electrodes such as p^+-Si [33], n^+-Si [39,40,43], Al [34], Pt [35,41,42,44,142], Ag [37], Au [37], Ti [38,42,146,147], TiN [36], etc. have been studied for ZrO_2-based MIM RRAM structures. In this section, we discuss resistive switching and related properties of ZrO_2-based RRAM structures.

Unipolar resistance switching (URS) mechanisms and properties of non-stoichiometric reactive rf magnetron sputter deposited Pt/ZrO_x/p^+-Si (MIS) sandwich structures using a Zr metal target at 400 °C has been reported by Lee et al. [33]. A highly doped *n*-Si(001) substrate was used as the bottom electrode with a 100-nm-thick Pt top electrode. The RRAM was implemented with an *n*-MOSFET using a Pt/ZrO/n^+-Si structure (MISFET) at the source side of the nMOSFET as a 1T1R structure (one transistor and one RRAM). By applying proper bias, two distinct resistance states, high resistance state (HRS) and low resistance state (LRS), were observed in both MIS and MISFET structures. Phase identifications of the mixed monoclinic and tetragonal zirconium oxide layer were studied using XRD, TEM and X-ray photo-electron spectroscopy (XPS). The ZrO_x layers consisted of three sub-layers: a stoichiometric upper zirconium oxide layer with high resistance, a transition region with medium resistance, and a conducting zirconium oxide bulk layer, based upon XPS and SEM analyses. The resistive switching mechanism and negative differential resistance (NDR) behavior were explained by electron trapping and detrapping by excess Zr^+ ions in the transition layer which controlled the electric field distribution and current flow inside the oxide [33].

Wu et al. [34] demonstrated unipolar resistive switching behavior for stoichiometric reactive rf magnetron sputter deposited 60-nm-thick ZrO_2 films using aluminum as a bottom electrode. A typical Al/ZrO_2/Al/SiO_2/p-Si(001) device cell exhibited stable and reproducible switching behavior [34]. Fig. 13 shows typical *I–V* switching characteristics of a RRAM device cell with a 60-nm-thick ZrO_2 layer. Initially 8 V was used for the forming process, by which the pristine device was turned on. Reset is performed after the forming process, by sweeping the applied positive voltage to 0.4 V with 0.1 A compliance current. For continuous sweeping, more than 2.5 V with 0.01 A compliance current was used for the set process. Successive reset was performed by applying higher compliance current. Good retention behavior was observed for the Al/ZrO_2/Al device at both high and low resistance states. The resistance of the HRS is about 90 kΩ while the resistance of the LRS is approximately 40 Ω. The average on/off ratio between the two states is larger than 2×10^3. A Schottky conduction mechanism has been established by fitting the *I–V* characteristics at high voltage region. Based on Joule heating, a mechanism for the formation and rupture of conducting filament has been reported [34].

The effect of top electrode material (Ti, Pt, or Al) on the resistive switching properties of rf magnetron sputter deposited 70-nm-thick a-ZrO_2 films at 250 °C on a Pt (Pt/Ti/SiO_2/Si) bottom electrode was systematically studied [35]. All films were deposited at 10 mTorr process pressure with a 6:12 oxygen to argon ratio. Improved bipolar resistive switching (BRS) was demonstrated for Ti top electrodes with a Ti/ZrO_2/Pt structure, as shown in Fig. 14(a). A forming voltage of ~8.8 V with a 5 mA compliance current was used for initial forming of the Ti/ZrO_2/Pt device. A similar forming process was applied for devices with Pt and Al top electrodes. After forming the Ti/ZrO_2/Pt device reaches LRS, the ON state. To switch the device from LRS to HRS (OFF state), a negative voltage is applied. For successive set/reset process, positive voltages were used for set process and negative voltage for reset without any current compliance for the typical Ti/ZrO_2/Pt device. A typical *I–V* switching curves for Pt/ZrO_2/Pt and Al/ZrO_2/Pt devices are unipolar [as shown in Fig. 14(b)], where only positive voltage was applied to switch from HRS to LRS and LRS to HRS with an appropriate current compliance [35]. The oxygen content and oxygen related defects at the active oxide layer had a large influence on the resistive switching characteristics [35,145–151]. This phenomenon was proposed based upon the evolution of series resistance at the Ti/a-ZrO_2 interface, composed of TiO_x and ZrO_y, and this contact resistance imposed current compliance on the device [35,42]. Bipolar and unipolar switching behaviors with a variation in switching parameters were observed in the a-ZrO_2/Pt sample connected using a W probe [42].

The different *I–V* curves for the top electrode materials were explained by differences in work function and oxygen diffusion. The Ti electrode, which has a low work function (4.3 eV), serves as an oxygen getter and induces oxygen vacancies at the Ti/a-ZrO_2 interface which would modify the oxygen vacancy distribution within the a-ZrO_2 active layer. This leads to better resistive switching characteristics, first proposed by us [35,38,42]. As for Ti/ZrO_2/Pt devices, the conducting filaments are formed in series with the Ti-induced interface layer after the forming process. The interface layer serves as an oxygen reservoir and acts as a series resistance. While applying the bipolar voltage sweeps, interfacial oxygen migration causes a redox reaction leading to the formation/rupture of conducting filaments near the Ti/ZrO_2 interface. There is no distortion and 'set fail' phenomenon observed during successive dc switching cycle (up to 10^3 cycles) for the Ti/ZrO_2/Pt device. R_{ON}, R_{OFF}, V_{ON}, and V_{OFF} of the Ti/ZrO_2/Pt device have sharp distributions in comparison to the Pt/ZrO_2/Pt and Al/ZrO_2/Pt devices as shown in Fig. 15. More than 10^4 cycles of write–read–erase–read operations with more than 10^5 s data retention has been reported for Ti/ZrO_2/Pt devices without degradation and data loss.

Wang et al. [38] proposed that the forming voltage increases with increased thickness of sputtered-deposited a-ZrO_2 layer. The a-ZrO_2 films were deposited by rf magnetron reactive sputtering at 200 °C substrate temperature, 10 mTorr, and 1:2 oxygen to argon gas ratio. Since the forming process is equivalent to dielectric breakdown, after the forming process, conducting filaments exist within the RS films [38,152]. As the a-ZrO_2 thickness increases, it can withstand higher breakdown voltage, and thus, a higher forming voltage has been observed.

Influence of current compliance during forming process on resistive switching properties of the Ti/ZrO_2/Pt device has also been reported [38]. ON state current increases with increased current compliance during the forming process, indicating the formation of more, or stronger, conducting filaments in the ZrO_2 layer. Thus, the formation of

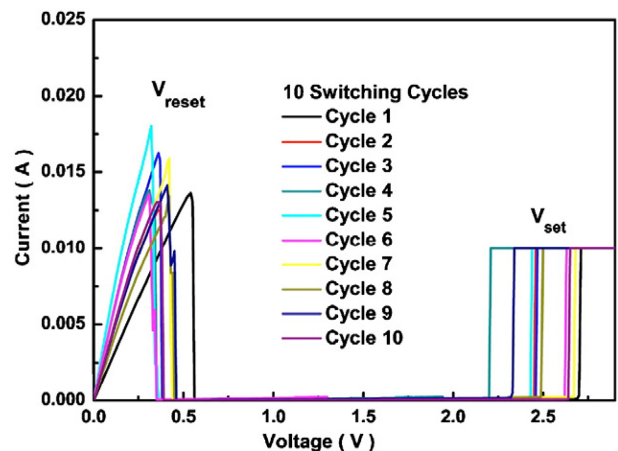


Fig. 13. *I–V* characteristics of ZrO_2-based RRAM device cells with an Al top and bottom electrode [34].

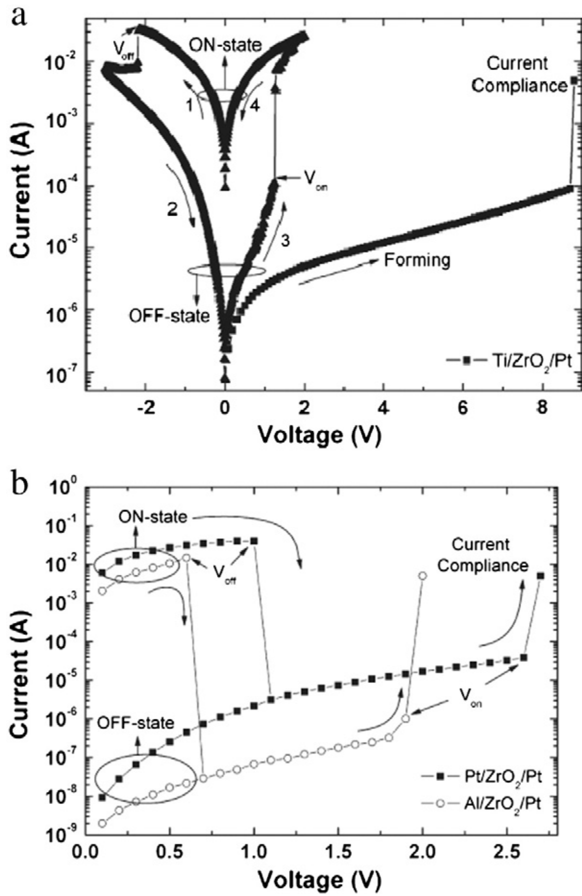


Fig. 14. Typical *I–V* resistive switching characteristics of Ti/ZrO_2/Pt, Pt/ZrO_2/Pt, and Al/ZrO_2/Pt devices [35].

percolating filaments is influenced by the current compliance [38,40,153]. Larger reset voltage is required for higher current compliance. However, the resistance ratio between two memory states is almost independent with the compliance current. Operational errors have been observed during continuous write–read–erase–read cycles, measured at less than 50 ns pulse width. More than 10^3 ac switching cycles have been observed in Ti/ZrO_2/Pt devices without degradation.

A bipolar resistive switching memory device consisting of 20-nm-thick a-ZrO_2 layer grown on Pt by sol–gel methods has also been reported [36]. Zirconium nitrate ($Zr(NO_3)_4 \cdot 5H_2O$) and ethylene glycol monomethylether ($C_3H_8O_2$) were used as precursor and solvent, with acetylacetone ($C_5H_8O_2$) as a stabilizer reagent. The films were deposited by spin-coating at 2500 rpm for 30 s followed by heating at 180 °C for 5 min to remove organic ingredients. Furnace annealing was performed at 600 °C in O_2/N_2 mixed gas ambient for 15 min. Sputter-deposited TiN was used as the top electrode to fabricate a TiN/ZrO_2/Pt sandwich structure. Excellent bipolar resistive switching characteristics (shown in Fig. 16), including highly uniform and stable switching parameters, presentable endurance (up to 600 ac cycles), and long retention time (up to 10^4 s) has been reported. Improvement in switching properties has been ascribed to the effect of TiN electrode, which acts as an oxygen reservoir during formation and rupture of the filamentary conducting paths, thus modifying the concentration distributions of the oxygen ions and vacancies in the ZrO_2 layer [35].

Li et al. [37] reported the bipolar resistive switching characteristics of Au/ZrO_2/Ag devices. The structure was achieved by evaporating a 40-nm-thick ZrO_2 layer on Ag using ZrO_2 powder in a vacuum of 2.6×10^{-6} Torr to yield a deposition rate of 1 Å/s. A negative set voltage of −0.5 V and reset voltage of 0.6 V with a 1 mA compliance current were required for the switching process, without any forming

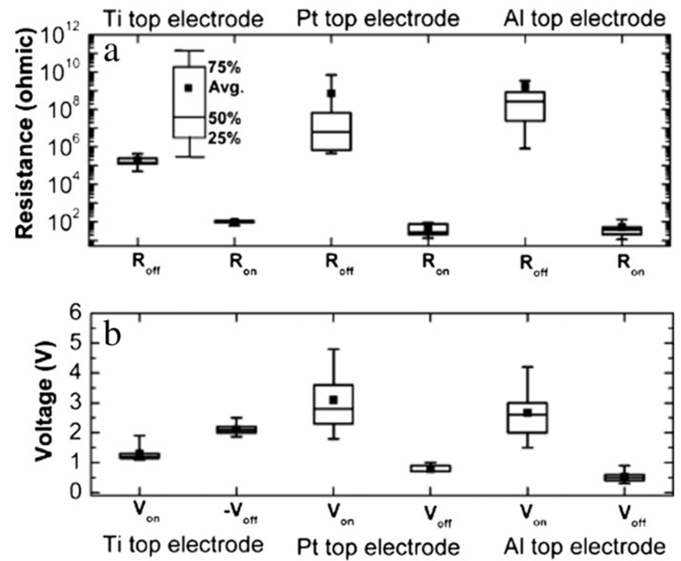


Fig. 15. Variations in the resistive switching parameters of Ti/ZrO_2/Pt, Pt/ZrO_2/Pt, and Al/ZrO_2/Pt devices. On and off resistances (R_{ON} and R_{OFF}) are measured at 0.3 V [35].

process. High device yield, low switching voltages (<1 V), high resistance ratio (~10^4), fast switching speed (50 ns), nondestructive readout, and good retention at 85 °C (10^4 s) were reported [37].

To improve the RRAM device properties, an internal transistor has been used to control the overshoot current, parasitic capacitance, and filament size. A Pt/Ti/ZrO_2/Pt RRAM structure combined with a transistor (1T1R device) was proposed by us [154,155]. The ZrO_2 layer was deposited by rf sputtering using the same deposition parameters reported by Lin et al. [35]. A 4 V forming voltage with an appropriate compliance current was required to activate the reversible resistive switching behavior of pristine memory devices to reach the LRS (ON state). In the set process, a positive voltage was applied to the top electrode sweeping from zero to the set voltage (V_{set})~0.8 V; a set current of 20 μA was obtained with the source grounded. This process causes the current suddenly increase to reach LRS, where the set current value was controlled by modulating the gate voltage of the transistor. In the reset process a positive voltage was applied to the source pad, sweeping from zero to 2.5 V, with the top electrode grounded. Meanwhile, a gate voltage up to 2 V is employed in order to supply an adequate I_{reset}; a current of 20 μA was reached at 1 V, leading to a decrease in reset current as the memory state is switched back to HRS. Small set and reset current, as low as 20 μA, with an operation voltage is less than 1.5 V was reported [154,155]. A multilevel LRS can be achieved in this 1T1R RRAM structure by modulating the gate voltage of the transistor. Four LRS levels were achieved by changing the amplitudes of set current from 20 to 40 to 115 to 280 μA. A resistance ratio HRS/LRS of 6×, after switching for more than 2000 times, was observed. A nondestructive readout for up to 10^4 s at 100 °C was observed for multilevel data storage under a stress voltage of 0.1 V. The devices have high switching speed (250 ns), low operation voltage (V_{set} = 2.5 V; V_{reset} = −2 V), and acceptable HRS/LRS resistance ratio (>10) suitable for next generation nonvolatile memory device applications [154,155].

6.2. Effect of metal nanocrystals and implantations

Several research groups have demonstrated, since 2002, improved resistive switching behavior for organic bistable devices with an organic/nanocrystal/organic structure sandwiched between two metal electrodes [156–158]. However, the organic material is not thermally stable or compatible with current CMOS technology. In 2007, Guan et al. [39] first proposed the improved resistive switching properties of

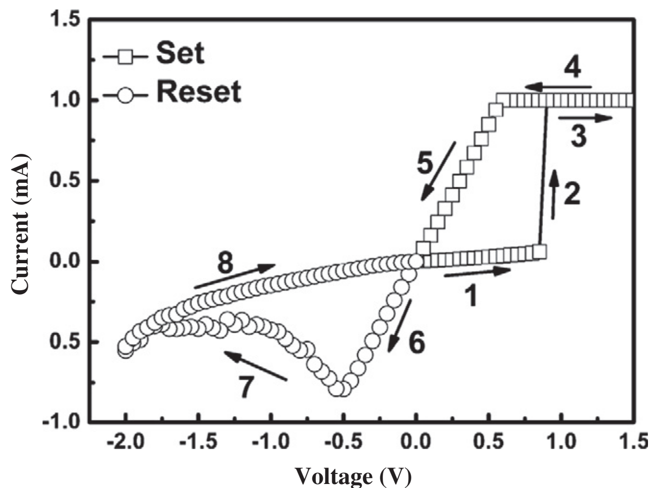


Fig. 16. A typical bipolar *I–V* curve for a sol–gel derived ZrO_2-based TiN/ZrO_2/Pt structure [36].

Au nanocrystals (NCs) embedded in ZrO_2 layers. Several groups have demonstrated improved resistive switching properties by incorporating metal nanocrystals, implanting metals, or embedding metal layers into the active binary oxide layer [39,131,159–161]. An example of the latter is evaporated Au to form ZrO_2/Au/ZrO_2 (with thickness of 25/2/25 nm) on an n^+-Si substrate [39]. Prior to the 50-nm-thick Au top electrode evaporation, high temperature post-depositions annealing (700, 800, or 900 °C, for 2 min in N_2 ambient) were performed to form Au nanocrystals. Fig. 17(a) shows a cross section transmission electron microscopy (XTEM) image of the microstructure following an 800 °C annealing. The gold nanocrystals are clearly observed embedded in the polycrystalline ZrO_2 (p-ZrO_2) matrix. The resistive switching of this sample annealed at 800 °C is shown in Fig. 17(b). A resistance ratio of nearly 10^2 at 0.5 V was reported. To set and reset the device, ~−2.4 V and 3.2 V were used. The influence of Au NCs on resistive switching properties of ZrO_2 was investigated and compared with control samples (without Au NCs). The control sample exhibited poor, or nearly no, bipolar resistive switching [39]. Au NCs embedded with and without annealing, show reproducible bipolar resistive switching behavior. Several groups have studied the resistive switching properties of heterogeneous ZrO_2 layers [20,39,162,163]. Au NCs in p-ZrO_2 act as electron traps and improve the device yield by reducing the effective thickness of ZrO_2. The devices displayed reversible and reproducible resistance switching, nondestructive readout, good cycling performance, and nonvolatile properties [39].

An interesting effect has been reported by Liu et al. [40] who implanted Au into 70-nm-thick ZrO_2 layers on n^+-Si. The ZrO_2 films were deposited by evaporation at a rate of 1 Å/s, under a base pressure of 2.6×10^{-6} Torr, and annealed at 800 °C for 120 s in N_2 ambient. Prior to Cr/Au (50 nm/10 nm) top electrode deposition, the samples were annealed at 400 °C for 5 s to activate the implanted Au atoms. Unlike most of the undoped transition-metal-oxide based resistive switching memory devices, [40,163–168], the Au-implanted crystalline-ZrO_2-based sample did not require an electroforming process to initiate resistance switching. By sweeping the applied positive voltage (0 to 10 V) with 10 mA current compliance, an abrupt increase in current appeared at a set voltage (V_{set}) of 8 V, and the device switched from the HRS to LRS, as shown in Fig. 18. The reset process was performed by applying more than 2.2 V with compliance current greater than 10 mA. 100% device yield was reported for the implanted samples. For the control samples, about 10% of the test cells showed unipolar switching after the electroforming process (forming voltage > 10 V). More than 40% of the test cells showed bipolar switching phenomenon under ±4 V switching voltage. The reset of the test cells were unstable with noisy switching. The dominant conduction mechanisms in the ON and OFF states were hopping and trap-controlled space-charge-limited conduction (SCLC), respectively. Au/Cr/Au-implanted-ZrO_2/n^+-Si device exhibit high device yield, good endurance, fast switching speed, and long retention [40].

ZrO_2-based nonpolar resistive switching memory devices exhibit puzzling polarity-dependent characteristics. Guan et al. [41] investigated the reproducible nonpolar resistive switching performance of Cu-doped ZrO_2 (ZrO_2:Cu) memory devices with a Cu/ZrO_2:Cu/Pt structure. Three sequential resistive ZrO_2/Cu/ZrO_2 switching layers with thickness of 20/3/20 nm, were deposited by electron beam evaporation on Pt/Si(001). A Cu top electrode (70 nm) and a protective Au layer (30 nm) were then deposited to form complete RRAM structure. Fig. 19 shows typical nonpolar *I–V* switching characteristics of Cu/ZrO_2:Cu/Pt memory devices. A current limited set voltage (V_{set}) was applied to turn the device on (curves a or c), while a reset voltage (V_{reset}) was required for switching the device back to the OFF state (curves b or d). The switching characteristic of the devices shows a uniquely nonpolar behavior: both switching from ON to OFF and from OFF to ON can be accomplished without changing the voltage polarity (unipolar, e.g., curves a and b). However, they can also be achieved by changing the polarity (bipolar, e.g., curves a and d). No forming process was required for this structure [41]. Typical resistances of the ON and OFF states are on the order of 10^2 Ω (R_{on}) and 10^8 Ω (R_{off}) at 300 mV, respectively with a resistance ratio of more than 10^6. The set and reset operation speeds were as fast as 50 and 100 ns, respectively.

The same group [43] also investigated the reversible bipolar resistive switching properties of Zr^+-implanted in ZrO_2 layers on n^+-Si. The

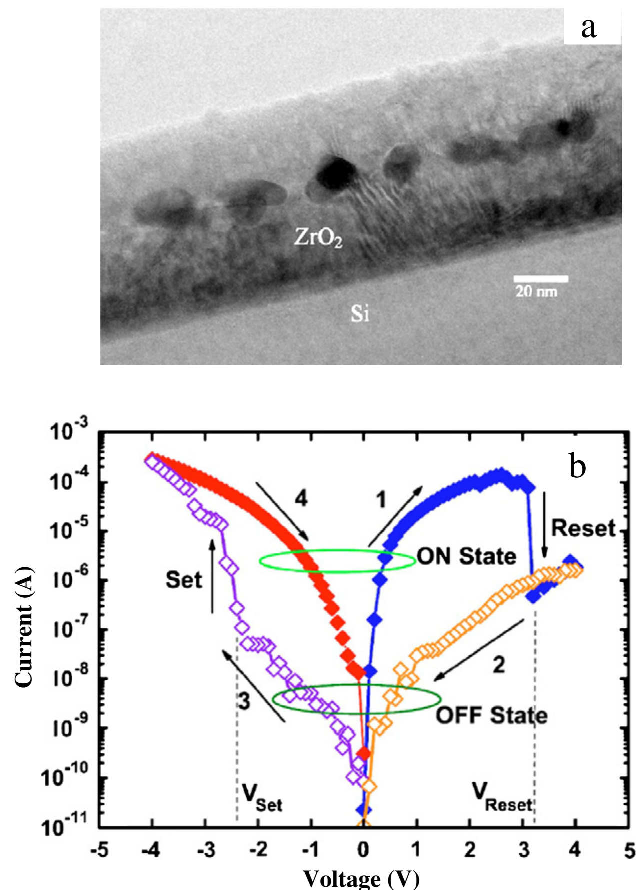


Fig. 17. (a) XTEM image and (b) typical bipolar *I–V* switching characteristics of an 800 °C annealed Au NC embedded ZrO_2-based RRAM device. Arrows indicate sweep directions [39].

Zr^+-implanted ZrO_2 films are annealed at 800 °C for 30 s in N_2 ambient. Evaporated Cr/Au (10 nm/50 nm) was used as a top electrode. The resistance ratio and device yield were significantly improved by the Zr^+-implantation step compared to un-implanted samples, though the set and reset voltages were almost same. The resistive switching mechanism of the fabricated structures was explained by trap-controlled SCLC conduction theory [43].

We reported [159] robust unipolar and bipolar resistive switching properties of a-ZrO_2 film embedded with Co NCs. Sputtering was used to deposit two-layer a-ZrO_2 films, each layer 10 nm thick, with an intermediate Co layer (5 nm) deposited by e-beam evaporation. The samples were annealed at 600 °C for 60 s in N_2 to form Co nanocrystals. The Ti/Pt top electrode was deposited by thermal evaporation. A negative forming voltage of −1.5 to −2.8 V was required for pristine Co NC embedded ZrO_2-based devices in order to activate switching. Samples with and without Co NCs exhibit bipolar switching phenomena with positive set and negative reset process, as shown in Fig. 20(a). Unipolar switching (negative set and reset) was also observed for the Co NC embedded devices [159]. Both types of switching properties improved significantly after annealing at 600 °C for 60 s in N_2 due to the formation of nanocrystals, as shown in Fig. 20(b). Co NC formation does not introduce more oxygen vacancies within the ZrO_2 layer after post annealing. The formation equations for CoO and ZrO_2 are as follows [159,169]:

$$Co + \frac{1}{2}O_2 \rightarrow CoO; \Delta G_1^0 = -214 \text{ kJ/mol}, \quad (6)$$

$$Zr + O_2 \rightarrow ZrO_2; \Delta G_2^0 = -1042.8 \text{ kJ/mol}. \quad (7)$$

Thus, the Gibbs free energy, for the reaction $CoO + Zr \rightarrow ZrO_2 + 2Co$ is negative, indicating that Co is stable to oxidation in ZrO_2 [159]. This thermodynamic prediction is corroborated with HRTEM and XPS results.

An improved unipolar and bipolar resistive switching properties of Co NC-embedded ZrO_2-based RRAMs with 1T1R architecture have also been investigated by us [170]. The device showed stable and reproducible URS and BRS characteristics including low operation current (20 μA), low switching voltage, multi-bit storage characteristics, and reliable data retention for LRS with 20 μA set current at 85 °C. Fig. 21 shows typical *I–V* switching characteristics of 1T1R-architecture devices, in which the transistor acts as a perfect current limiter. Small set and reset currents, as low as 20 μA are obtained, as shown with the operation voltage less than 1.3 V. The devices can also be operated in URS mode with negative bias set and reset process,

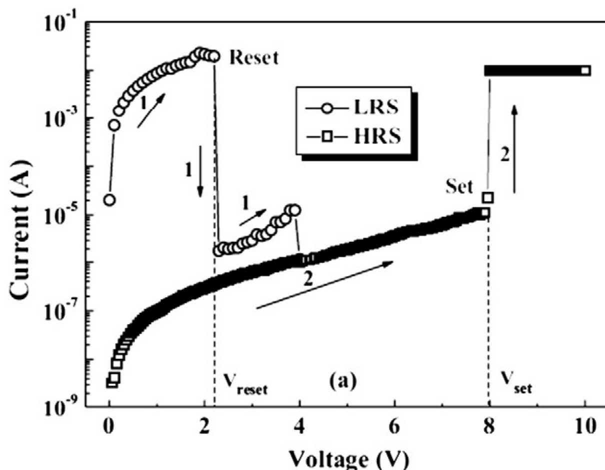


Fig. 18. Typical *I–V* switching characteristics of the Au-implanted ZrO_2-based RRAM device, arrows indicate sweep directions [40].

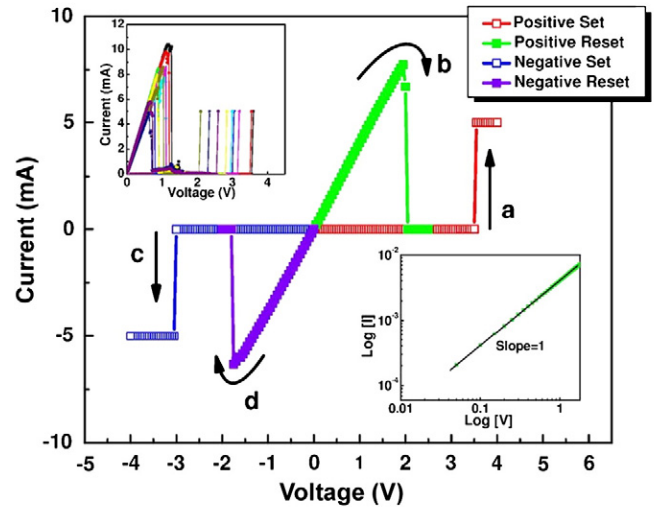


Fig. 19. Typical nonpolar *I–V* switching characteristics of Cu/ZrO_2:Cu/Pt memory devices. The upper inset shows the reproducibility of resistive switching in dc sweep mode (10 cycles) and the bottom inset shows *I–V* fitting result in log–log scale, demonstrating a linear correlation [41].

where V_{set} is ~−1.6 V. Multilevel LRS is achieved by modulating the gate voltage of the transistor as also shown in Fig. 21. Three distinct LRS levels are achieved using set current compliances of 20, 40 and

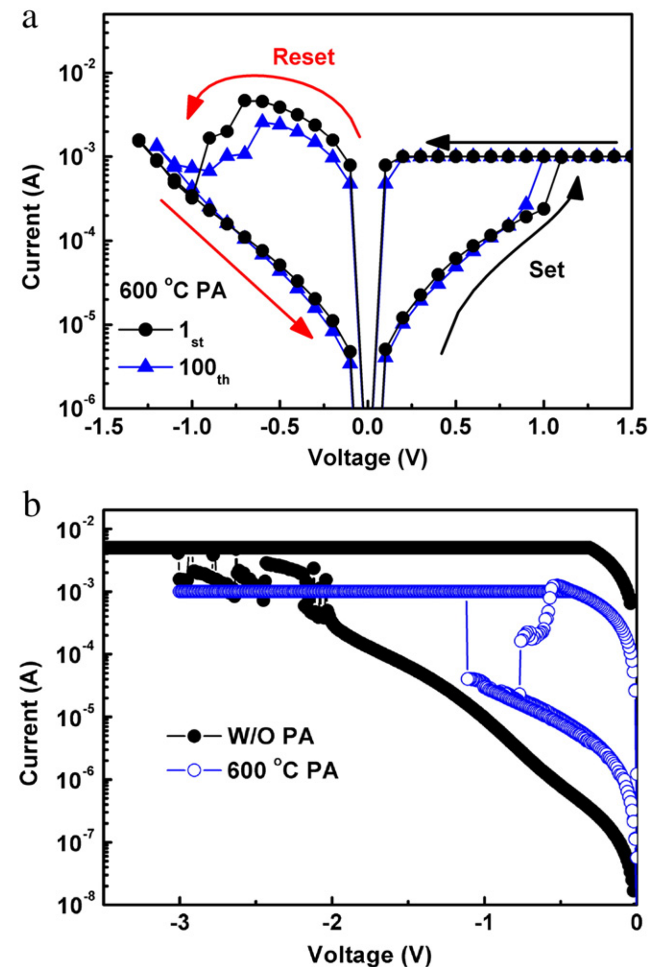


Fig. 20. (a) Bipolar resistive switching characteristics of Ti/ZrO_2/Co NC/ZrO_2/Pt devices, and (b) negative bias set process for the Co NC-embedded devices with and without post annealing. The annealed device shows unipolar switching [159].

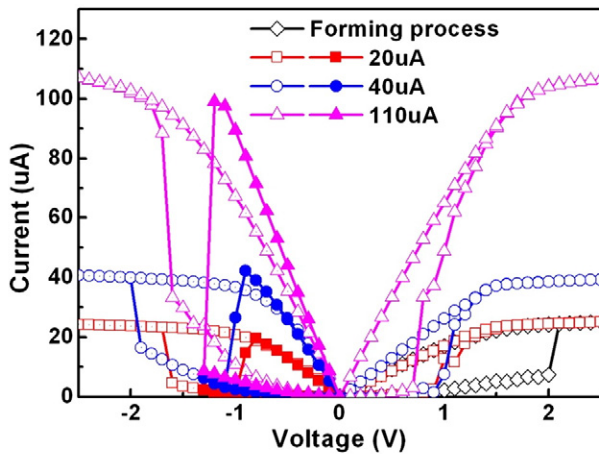


Fig. 21. Typical unipolar and bipolar *I–V* switching characteristics of the set and reset process at 20, 40 and 100 μA operation current for a Ti/ZrO_2/Co NC/ZrO_2/Pt RRAM device with 1T1R architecture.

100 μA, respectively. It is observed that the high I_{set} leads to slightly higher V_{reset}.

Fig. 22 shows schematic RS mechanism of Ti/ZrO_2/Co NC/ZrO_2/Pt devices. After the forming process, a conduction filament consisting of oxygen vacancies is formed and the device is switched to LRS. The conduction filament is expected to connect with Co NC, due to the reduced effective ZrO_2 thickness and the local electric field enhancement, to provide an easy and localized path to form and rupture the conducting filament [Fig. 22(a)] [159,171]. When applying negative bias to the top electrode, O^{2-} ions drift from the interfacial layer between Ti and ZrO_2 to the bulk film and reoxidize the region beneath the interfacial layer by local Joule heating to switch the device into HRS [Fig. 22(b)]. The conduction filaments below metallic Co NCs are not expected to rupture since O^{2-} cannot pass through the nanocrystals and drift to the bottom region [159]. Therefore, a smaller negative set voltage (−1.1 to −1.6 V) can be achieved without fluctuating set voltage issue. Defects are created due to local electric field enhancement and align to form the conducting filament during the negative bias set process (Fig. 22(c)). Furthermore, when the negative bias (−0.6 to −0.9 V) is applied to the top electrode again, O^{2-} are expected to drift to the bulk film and reoxidize the conducting filament beneath the interfacial layer, then the device switches to HRS again [Fig. 22(d) and (e)]. In contrast, the Co-NC-embedded devices without PDA need higher negative set voltage (−2 to −3 V) and have a fluctuating set voltage issue. A Ti/ZrO_2/Pt device [146,147,159] was broken down by applying a high negative bias along with fluctuating set voltage. The filaments were driven to percolate toward the top electrode under high electric field which resulted in too many external defects to degrade the device. However, the NC-embedded device only requires half of the negative bias set voltage applied to the without NC-embedded device due to the reduced effective thickness of the ZrO_2 layer.

Recently, a phenomenological model for the reset mechanism of metal-oxide RRAM devices was proposed that indicates the reset process is dominated by O^{2-} drift due to the electric field and O^{2-} diffusion due to a concentration gradient [159,172]. For the ZrO_2-based RRAM with a Ti top electrode, a TiO_x interfacial layer formed at the Ti/ZrO_2 interface may act as a diffusion barrier for O^{2-} migration [147,159]. Thus, when positive bias is applied to the top electrode, thermal O^{2-} diffusion cannot overcome the electric field drift. Thus, too few O^{2-} ions reach the bulk to reoxidize the conducting filaments, leading to a positive bias reset failure. Therefore, in the Ti top electrode system, the reset process can only be achieved using a negative bias. The Co NCs lead to local electric field enhancement. Hence, the set process is achieved by the formation of a suitable amount of electric-field-induced external defects such as oxygen vacancies that form the conducting filament under negative bias [159].

Resistive switching characteristics of sol–gel derived Gd, Dy, or Ce doped ZrO_2 films with Pt bottom and TaN top electrodes have been reported by Lee et al. [142]. To prepared doped ZrO_2 film, zirconyl nitrate hydrate was slowly dissolved in a mixture of 2-methoxyethanol and acetic acid to reach a solute concentration of 0.3 M. Gadolinium nitrate hexahydrate, dysprosium nitrate hydrate, and cerium nitrate hexahydrate, were added as dopants. Forming-free bipolar switching behavior has been observed in pure ZrO_2 films with large HRS fluctuation during the dc sweep cycle. This fluctuation is attributed to the large number of film defects (including oxygen vacancies) that are formed during the deposition process. Trivalent Gd and Dy doping of ZrO_2 films increases the HRS current level due to the generation of excessive oxygen vacancies. On the other hand, tetravalent Ce doping enhances ZrO_2 crystallization and reduces film defects, without increasing oxygen vacancies. For this reason, forming is required for Ce doped ZrO_2 [142]. However, stable endurance (5000 cycles) with a relatively large resistance ratio has been reported. Zhang et al. [45] reported that trivalent Al and La doping improve the distribution of resistive switching parameters. Resistive switching properties are also improved by embedding an evaporated Mo layer within rf magnetron sputter deposited a-ZrO_2 films (ZrO_2/Mo/ZrO_2; layer thickness = 20/2/20 nm) as we have reported [44]. Prior to Ti top electrode evaporation, the samples were annealed at 800 °C in N_2 ambient for 60 s to diffuse the Mo atoms into the ZrO_2 matrix. The embedded Mo layer acts as an oxygen getter, causing formation of more controllable oxygen vacancies within the ZrO_2 layer. These oxygen vacancies can enhance the formation and rupture of conducting filaments and further improve the switching characteristics of ZrO_2-based devices. A

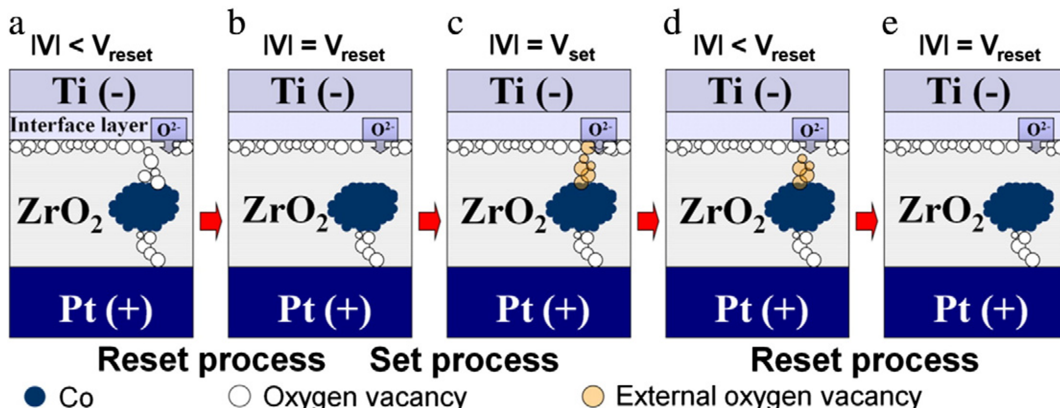


Fig. 22. Schematic representation of conducting filament formation and rupture by applying negative bias to set and reset Ti/ZrO_2/Co NC/ZrO_2/Pt devices after the forming process [159].

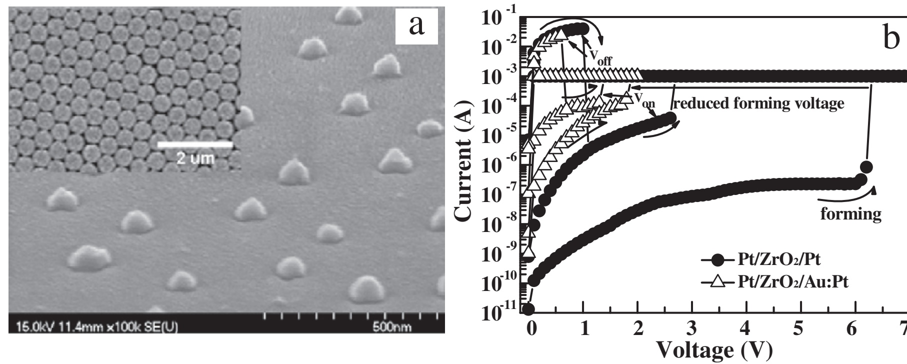


Fig. 23. (a) SEM image of Au nanospheres prepared by a lithography process. The inset shows the arrangement of the NSs on Pt/Ti/SiO_2/Si substrate. (b) Typical *I–V* switching curves for Pt/ZrO_2/Pt and Pt/ZrO_2/Au:Pt devices [173].

narrower dispersion in the ON and OFF state resistance and voltage was observed in the Mo-layer-embedded devices compared to devices without embedded Mo layer. Forming-free Ti/Mo:ZrO_2/Pt RRAM devices have lower operation voltage (<1.5 V), good endurance (>10^3 cycles), nondestructive readout (>10^4 s), high-speed operation (10 ns), and long data retention (>10^7 s) [44].

We observed that the resistive switching properties could be improved by modifying the bottom electrode using metal nanospheres (NSs) [173]. A Pt bottom electrode modified with Au NSs was used to suppress the variation in switching parameters. The Au NSs were prepared by lithography, as shown in Fig. 23(a). The 30-nm-thick ZrO_2 active layer was deposited by reactive rf magnetron sputtering at 200 °C substrate temperature. The forming process causes the formation of conducting filaments in the memory film at 6.2 V with 1 mA compliance current for the control sample without Au NSs, as shown in Fig. 23(b) [173]. The forming voltage of the Pt/ZrO_2/Au:Pt device is reduced to about 1.9 V (close to V_{on}), compared to the control device. It is observed that the Pt/ZrO_2/Au:Pt device can be operated with lower voltages (V_{on} and V_{off}) than the Pt/ZrO_2/Pt device. A high electric field was created above the Au nanospheres within the Pt/ZrO_2/Au:Pt device. So that, the formation and rupture of conducting filaments was enhanced near the top of Au NSs after the forming process. Thus, the conducting filaments were confined, which decreased the variations in operating parameters [173]. Stable retention and nondestructive readout properties of the Pt/ZrO_2/Au:Pt device were observed at both room temperature and 150 °C.

6.3. Switching effect of ZrO_2 using buffer layer

As oxygen vacancies are the main player in ZrO_2 RRAMs, we investigated the possibility of using an oxygen ion conductor buffer layer for enhancing resistive switching properties. We replaced the native ZrO_y layer of a ZrO_2-based memory device with an CaO:ZrO_2 oxygen ion conductor buffer layer [174]. A 30-nm-thick sputter deposited ZrO_2 film on Pt followed by 5-nm-thick sputter deposited CaO:ZrO_2 buffer layers having different CaO concentrations were used for this study. A 150-nm-thick evaporated Ti top electrode was used to produce a Ti/CaO:ZrO_2/ZrO_2/Pt structure. Unipolar resistive switching was observed for the ZrO_2-based RRAM devices having CaO buffer layers. The 2 mol% CaO doping concentration created more oxygen vacancies within the CaO:ZrO_2 buffer layer, thus enhancing oxygen ion conductivity. For the same operation time, more oxygen ions migrated from the TiO_2 layer laterally and vertically across the 2-mol% CaO:ZrO_2 buffer layer to form and rupture conducting filament. Ti/2-mol% CaO:ZrO_2/ZrO_2/Pt devices exhibited more endurance cycles with no soft errors [174]. Stable nondestructive readout and good retention were observed in both the ON and OFF states at RT and 150 °C.

We studied the bipolar resistive switching mechanism of ALD grown 3-nm-thick HfO_2 films with a Pt/HfO_2/TiN device structure, specifically the formation and rupture of conducting filaments near the HfO_2/TiN interface. However, by introducing a 5-nm-thick ZrO_2 layer (by sputter deposition) in the Pt/HfO_2/TiN device to yield a Pt/ZrO_2/HfO_2/TiN structure, unipolar RS behavior was observed, which reveals that the conducting filament form/rupture within the ZrO_2 layer [175]. A forming voltage of 2.2 V with 10 mA compliance current was used for the forming process. The device was switched on at ~2 V and switched off at ~0.7 V. A 1D1R structure using the Pt/ZrO_2/HfO_2/TiN RRAM device exhibited unipolar switching with higher operation voltages (V_{set} = ~3 V, V_{reset} = ~2 V) with continuous and stable RS behavior, as shown in Fig. 24. Stable retention (>10^5 s), good endurance (>100 cycles) and nondestructive readout properties were observed at both ON and OFF states at RT and 85 °C.

Table 1 shows a comparison of resistive switching device structures and their switching parameters for different ZrO_2-based RRAM devices. The devices with lowest operational voltage for bipolar ZrO_2-based RRAM devices were those with the TiN/ZrO_2/Pt structure [36]. Our Ti/ZrO_2/Pt bipolar device shows the highest switching speed, high endurance and very good device yield [42]. A high resistance ratio of 10^5 was observed for nonpolar Cu/ZrO_2:Cu/Pt devices [41].

7. Conclusions

In conclusion, ZrO_2 is an attractive candidate with enormous potential to substitute for conventional SiO_2 in gate dielectric applications in downsized ULSI technology due to high dielectric constant, large band offset, good thermal stability in contact with Si, and process

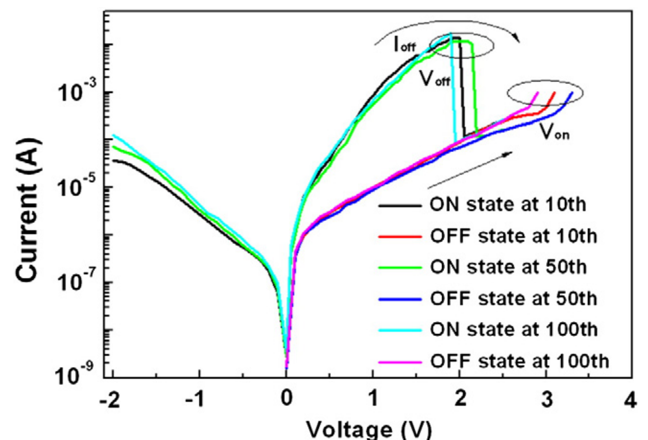


Fig. 24. Unipolar resistive switching characteristics for a Pt/ZrO_2/HfO_2/TiN device in a 1D1R architecture. ON and OFF states are shown after 10, 50, and 100 cycles [175].

Table 1
Comparison of resistive switching parameters of ZrO_2-based RRAM devices; V_F = forming voltage, I_C = compliance current for forming, $R_{off/on}$ = off and on state resistance ratio, ND = no data available.

Device structure	V_F and I_C (V, mA)	Switching type	V_{reset} (V)	V_{set} (V)	$R_{off/on}$	Set speed	Reset speed	Endurance cycles	Retention (S)	Device yield	Ref.
Au/ZrO_2/Ag	No	Bipolar	0.2 to 1	−0.2 to −0.079	10^4	50 ns	50 ns	500	85 °C, 10^4	NA	[37]
Pt/ZrO_x/p^+-Si	5–7	Unipolar	~1.2	~1.6	~3	100 ns	100 ns	80	RT, 10^3	43	[33]
Ti/ZrO_2/Pt	8.8, 5	Bipolar	−1.8 to −2.6	1 to 2	10	10 ns	10 ns	10,000	85 °C, 10^5	~100	[42]
Pt/ZrO_2/Pt	~8.8, 5	Unipolar	~1.1	~2.3	10^4	ND	ND	ND	ND	40	[35]
Al/ZrO_2/Al	8	Unipolar	0.4	2.5	2×10^3	ND	ND	ND	ND	ND	[34]
Al/ZrO_2/Pt	~8.8, 5	Unipolar	~0.7	~1.9	10^5	ND	ND	Good	RT, 10^4	38	[35]
TiN/ZrO_2/Pt	No	Bipolar	−0.5	0.8	10	NA	NA	600	RT, 10^4	NA	[36]
W-probe ZrO_2/Pt	8	Unipolar	±1.0	±3.6	Small	ND	ND	ND	ND	17	[146]
TaN/ZrO_2/Pt	No	Bipolar	~−0.7	1.2 to 0.7	<100	ND	ND	5000	ND	ND	[142]
Au/NC-Au ZrO_2/n^+-Si	No	Bipolar	1 to 3	2.6 to 3.5	~10^3	NA	NA	100	RT, >10^3	73%	[39]
Cr/Au-imp-ZrO_2/n^+-Si	~12, 10	Unipolar	2.2	8	~10^4	50 ns	100 ns	200	85 °C, 10^5	100%	[40]
Cr/Zr^+-imp. ZrO_2/n^+-Si	No	Bipolar	−3.1	3.2	~10^3	ND	ND	ND	RT, >2500	Higher than un-imp.	[43]
Ti/Co-NC-E ZrO_2/Pt	−1.5 to −2.8 (2–3), 1	Unipolar/ bipolar	−0.6 to −0.9 (0.6 to −1)	−1.1 to −1.6 (0.8 to 1.2)	10	ND	ND	>3500	220 °C, 10^4	ND	[159]
Cu/ZrO_2:Cu/Pt	No	Nonpolar	0.8 to 1.5	2.1 to 3.6	10^6	50 ns	100 ns	NA	RT, 10^4	NA	[41]
Pt/ZrO_2/Au:Pt	6	Unipolar	~1	~2	10^2	ND	ND	NA	150 °C, 10^2	ND	[173]
Ti/Mo:ZrO_2/Pt	No	Bipolar	−1.2 to −1.5	0.6–1	10^2	10 ns	10 ns	1000	RT, 10^7	ND	[44]
TaN/Gd:ZrO_2/Pt	No	Bipolar	−0.7 to −1.4	~1.1	10	ND	ND	5000	ND	ND	[142]
TaN/Dy:ZrO_2/Pt	No	Bipolar	−0.9	~1.1	5	ND	ND	5000	ND	ND	[142]
TaN/Ce:ZrO_2/Pt	2.3, 0.1	Bipolar	~−0.6	1.2 to 0.9	100	ND	ND	5000	ND	ND	[142]
Ti/CaO:ZrO_2/Pt	−8, 5	Unipolar	−1.3	−3	10	ND	ND	400	150 °C, 10^6	ND	[174]
Pt/ZrO_2/HfO_2/TiN	2	Unipolar	0.7	2	<10	ND	ND	200	85 °C, 10^2	ND	[175]

compatibility. Numerous deposition methods including evaporation, sputtering, PLD, ALD, MOCVD, and chemical sol–gel are commonly used to deposit ZrO_2 thin films on Si, metalized Si, strained-Si-based substrates, and III–V substrates. The recent progress of ZrO_2 dielectric layers for volatile DRAM applications, in terms of material and electrical properties produced by various deposition methods and different structures such as MIS and MIM has been briefly reviewed. The influence of different electrodes including highly-doped Si, and the effects of different metal and semiconductor doping on the dielectric properties has been investigated. Dielectric properties of stacked ZrO_2 and Al_2O_3 MIM capacitors were briefly reviewed. ZrO_2-based device structures embedded with Ge and SiGe nanocrystals are applicable for nonvolatile flash memory application. Sputter deposition of ZrO_2 is primarily used for nonvolatile memory applications due to several advantages. ZrO_2 films can be used as a charge trapping layer in SOZOS (poly-Si/SiO_2/ZrO_2/SiO_2/Si) and TAZOS (TaN/Al_2O_3/ZrO_2/SiO_2/Si) based nonvolatile flash memory stacks. Bipolar, unipolar, and nonpolar resistive switching properties are also observed in ZrO_2-based RRAM devices, depending on the device structure. Choice of electrodes plays a significant role in determining the nature of resistive switching properties by controlling the oxygen vacancy concentration in ZrO_2-based RRAMs. Metal nanocrystals, metal implantation, metal doping, and embedded metal layers in ZrO_2 films improve resistive switching behaviors. Oxygen ion conducting buffer layer can also be used to modify the oxygen vacancy concentration in the active layer. This review provides a roadmap of ZrO_2 thin films in future low power, nanoscale microelectronic device applications.

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