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Enhanced lateral heat dissipation packaging structure for GaN HEMTs on Si substrate

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HIGHLIGHTS

- An enhanced packaging structure designed for AlGaN/GaN HEMTs on an Si substrate.
- The V-groove copper base is designed on the device periphery surface heat conduction for enhancing Si substrate thermal dissipation.
- The proposed device shows a lower thermal resistance and upgrade in thermal conductivity capability.
- This work provides useful thermal IR imagery information to aid in designing high efficiency package for GaN HEMTs on Si.

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ABSTRACT

This work presents a technology for packaging AlGaN/GaN high electron mobility transistors (HEMTs) on a Si substrate. The GaN HEMTs are attached to a V-groove copper base and mounted on a TO-3P leadframe. The various thermal paths from the GaN gate junction to the case are carried out for heat dissipation by spreading to protective coating; transferring through the bond wires; spreading in the lateral device structure through the adhesive layer, and vertical heat spreading of silicon chip bottom. Thermal characterization showed a thermal resistance of 13.72 °C/W from the device to the TO-3P package. Experimental tests of a 30 mm gate-periphery single chip packaged in a 5 × 3 mm V-groove Cu base with a 100 V drain bias showed power dissipation of 22 W.

1. Introduction

The ability of Gallium Nitride (GaN) and Silicon Carbide (SiC) to operate at high voltages, high power densities, high temperatures and high frequencies make them highly interesting for use in power electronics applications. Because of its superior electron mobility compared to SiC, GaN should have superior performance in high frequency and high power operation [1]. However, SiC devices should theoretically perform better at relatively higher power densities because of their superior thermal conductivity. Wide bandgap and high critical field combined with high thermal conductivity are key desirable device features for high power operation. The relatively poor thermal conductivity of GaN makes heat management for GaN power devices a challenge for packaging designers to contend with.

This study describes an enhanced packaging structure designed for AlGaN/GaN High Electron Mobility Transistors (HEMTs) on an Si substrate. Instead of the flip chip or copper–molybdenum–copper (CMC) based packaging technology currently used in GaN HEMTs, the proposed device integrates GaN HEMTs, V-groove Cu base and TO-3P leadframe. The packaging structure is designed on the device periphery surface heat conduction for enhancing Si substrate thermal dissipation. Structural designs and fabrication processes were evaluated in terms of effects on device performance measures such as thermal resistance. For a fabricated device with the same drive condition, the proposed device shows a lower thermal resistance, and upgrade in thermal conductivity capability. The proposed fabrication process may also be applicable in other leadframe packaging or power modules.

2. Device structure and fabrication

Recent improvements in AlGaN/GaN HEMTs make them viable candidates for use in high-power and high-temperature electronic applications. The HEMTs fabrication and its electrical characteristics have been performed on different substrates (*e.g.* Sapphire, SiC and Si). The use of Si substrates for growth of GaN has the poor thermal conductive properties of Si. Therefore, thermal

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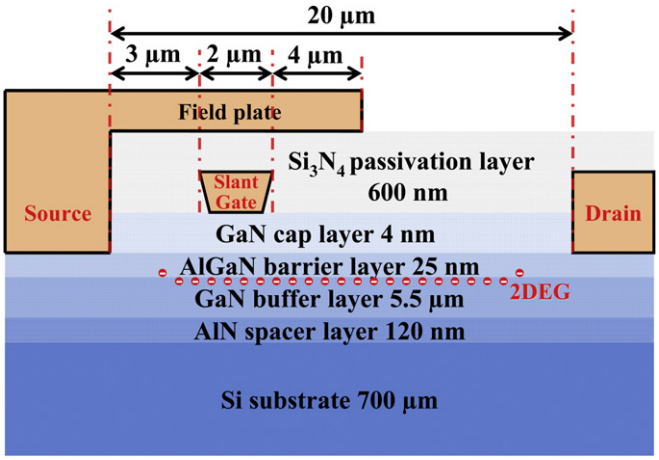

Fig. 1. Cross-section of AlGaN/GaN HEMT with slant gate and source field plate structure.

management is a critical factor in the design of Si-based GaN HEMTs and their corresponding packages [2].

The AlGaN/GaN heterostructure pattern is made using metal organic chemical vapor deposition (MOCVD) techniques on a 1000-μm-thick silicon substrate [3–5]. As shown in Fig. 1, the epitaxial structure consisted of a 120-nm-thick AlN spacer layer, followed by 5.5 μm thick GaN buffer layer, 25 nm thick AlGaN barrier layer and finish with 4 nm thick GaN cap layer. In the transistor fabrication process proposed in this study, ohmic contact formation in multi-layer Ti/Al/Ni/Au-based (20 nm/120 nm/25 nm/5100 nm) and Ni/Au-based (20 nm/150 nm) Schottky contacts achieve low contact resistance and smooth surface morphology. After ohmic contact formation, the device is passivated with a 600 nm thick Si_3N_4 layer. Device breakdown voltage and power performance are improved by electrically connecting the field plate electrode formed on the Si_3N_4 passivation layer to the source electrode. Finally, a 6 μm thick Au plated air-bridge process is employed for connecting multi-finger devices. Bonding pad connections are formed by electro-chemical plating with a gold layer 30 μm thick. Fig. 2 illustrates the AlGaN/GaN HEMT structure in this work. Each of the 60 gate fingers in the proposed layout has a gate width of 2 μm and a gate length of 500 μm, which yields a total gate periphery of 30 mm. The active device area is 0.25 mm^2, and adjacent gate fingers are separated by a 50-μm pitch, which includes source and drain contact regions.

The difficulty of achieving thermal performance improvements in electronic components increases as power densities increase and as device sizes decrease [6]. Effective thermal management is essential for high power packaging at operating junction temperatures above 240 °C. Self heating and its effects on transport properties determine the thermal dissipation properties of device packaging and the device junction temperature ranges that enable reliable and long-term operation. Most attempts to dissipate heat have used a gold–silicon eutectic bonded to a package substrate or leadframe. The thermal management solution proposed in this work minimizes thermal resistance and maximizes power dissipation. Fig. 3 shows how a GaN HEMT with a gate width of 30 mm is mounted on a V-shape grooved copper base and attached to a TO-3P package for high power operation. An adhesive is used to attach the device to a V-groove in the copper surface. The Cu base is then mounted to the TO-3P leadframe, and the device is connected to the external circuit by gold-wire bonding. Finally, efficient thermal management is achieved by using silicone-based protective

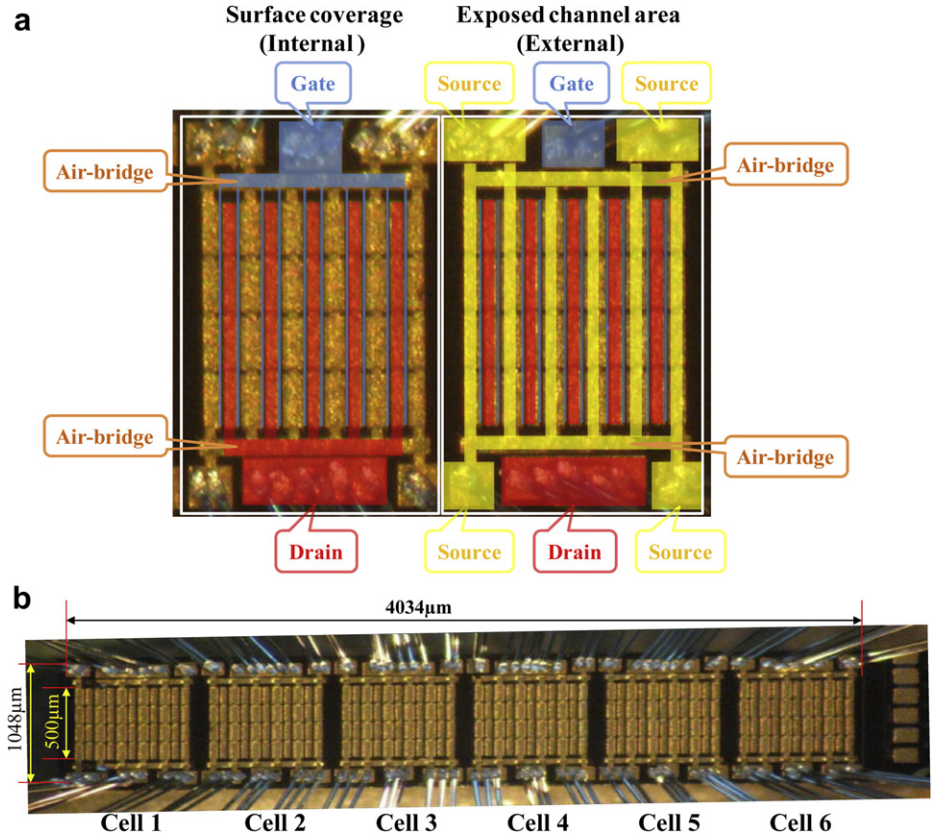

Fig. 2. Photograph and schematic of the HEMTs Dimensions. (a) The photograph of 10-finger HEMTs with air-bridge interconnection. (b) Overall die size 4034 × 1048 μm (6-cell), die thickness 1 mm.

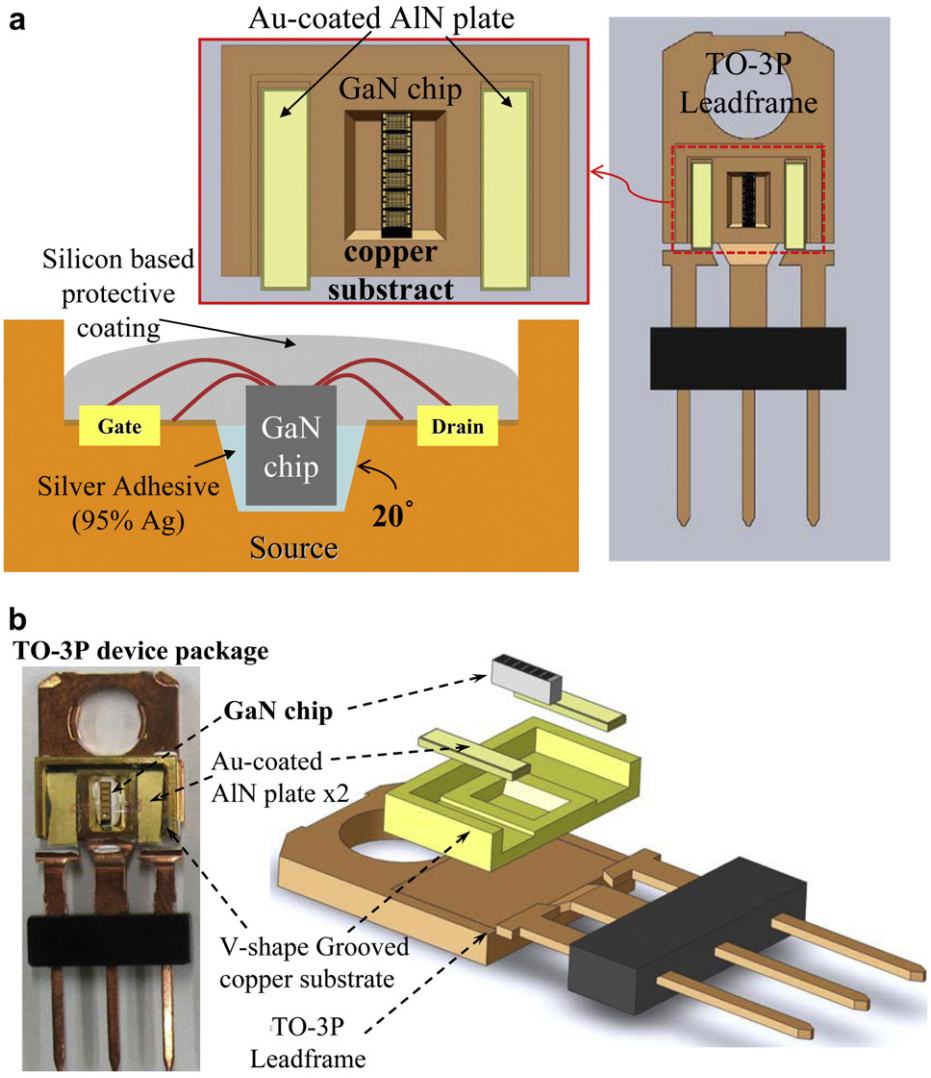

Fig. 3. Packaging processes of GaN HEMTs power device. (a) Die attachment on Cu base with thermoset paste; bonding with wires on to pads; covered with protective coating. (b) Mounted the V-groove Cu base on TO-3P leadframe.

coatings on GaN HEMT surfaces exposed to elevated temperatures in atmospheric environments. Selecting the appropriate adhesive for attaching the die is crucial for efficient operation of the device and should consider degradation and other failure mechanisms in the thermal treatment. For thermal conductivity exceeding 65 W/m K, a viable substitute for conventional thermal conductive silver adhesive is a V-shape grooved substrate. In comparison with conventional packages, V-shape grooved substrates not only provide an additional thermal path for lateral thermal conductivity, they also enable precise positioning. The microstructure is extended surface cooling for thermal requirements and obtained lower package thermal resistance in a similar package size, which exceeds those of ordinary metals.

3. Performance evaluation of packaged device

Total thermal resistance was measured in die thicknesses of 1 mm and 0.5 mm in a core is shown in Fig. 4. The thermal resistance measured in the TO-3P package was 13.72 °C/W, which included a junction-to-chip thermal resistance of 11.28 °C/W, a die attachment of 1.92 °C/W, and a package thermal spreading 0.52 °C/W [7]. The high power application-specific thermal resistance targets were also met through die thinning. In the single package HEMT device, reducing the silicon wafer thickness from 1 mm to 500 μm also achieved a ~16.8% reduction in thermal resistance. Assuming total power dissipation lower than 15 W, the temperature remains below 200 °C during switching operations. The thermal performance of the device plays a critical role in the electrical performance of the device. The V-groove Cu base used for the 30 mm GaN HEMTs has a lower thermal conductivity compared to the DIP package. The thermal impedance of the parts was compared by measuring the peak junction temperature over a range of dissipated powers at a drain voltage of 100 V. Fig. 5 demonstrates the thermal paths and infrared (IR) thermography of a packaged device at the peak temperature and at a dissipated power of 22 W. The peak junction temperature is 87 °C [8].

The measurement of temperature is essential to the thermal management of a device because localized self-heating during operation under high-voltage switching increases the channel temperature. Non-intrusive infrared spectroscopy is performed to measure the surface temperature profiles in the source-drain active region. Fig. 6 is an IR image of GaN chip bonded on a flat plate dual-in-line package (DIP) driven by a 100 V drain voltage. The line scan profile of IR thermography indicates that the temperature of the center finger is 120 °C, which confirms that the V-groove packaging design provides sufficient thermal conductive ability to spread and

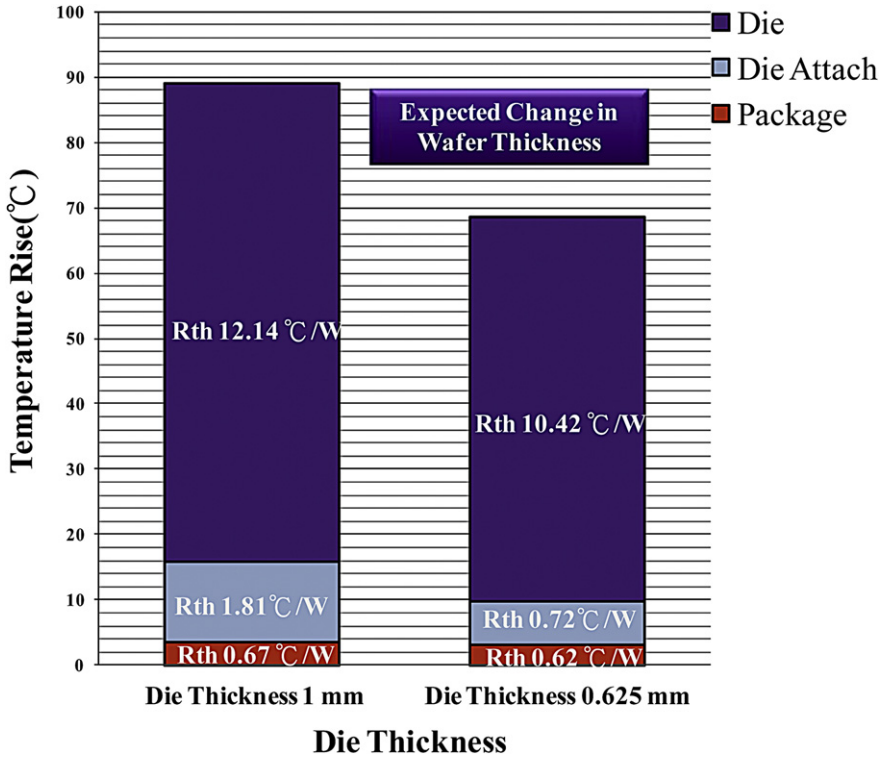

Fig. 4. Thermal resistance impacts due to thickness alterations.

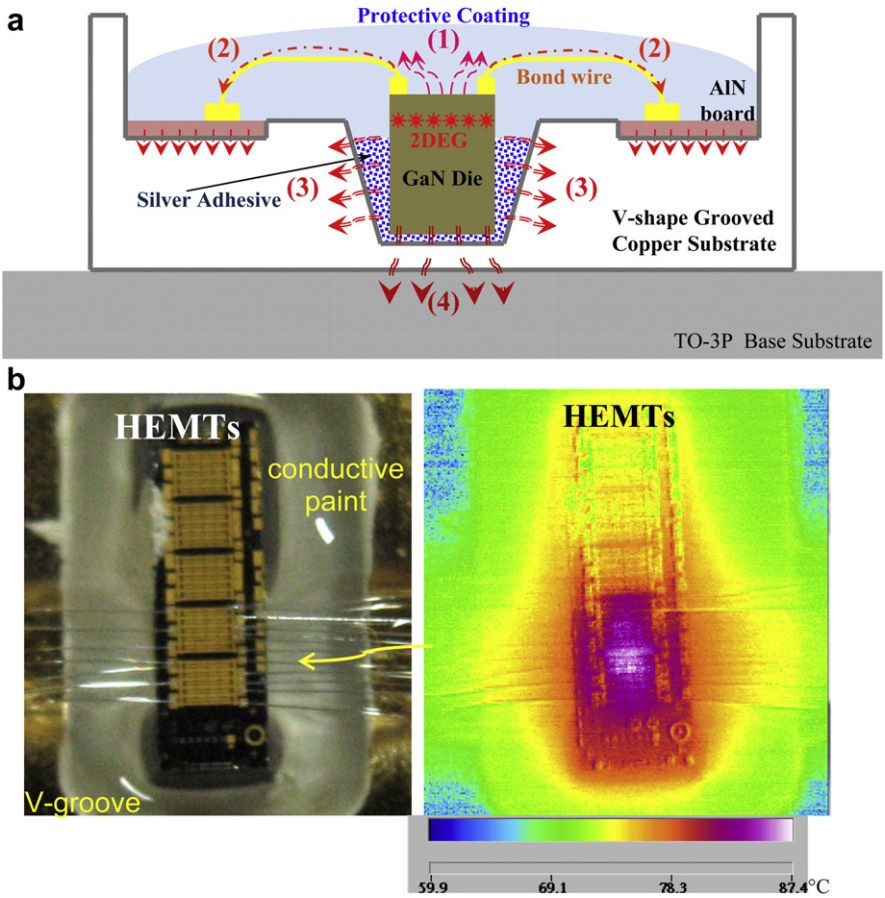

Fig. 5. Thermal paths and IR image of packaged HEMTs device. (a) The various thermal paths from the junction to case are depicted as follows: (1) Spreading to protective coating. (2) Transferring through the bond wires. (3) Spreading in the lateral device structure through the adhesive layer. (4) Vertical heat spreading of silicon chip bottom. (b) Thermal images of the GaN HEMTs at the V-grooved Cu base at a dissipated power of 22 W (100 Vd/0.22 A/10 min). The peak junction temperature is 87 °C.

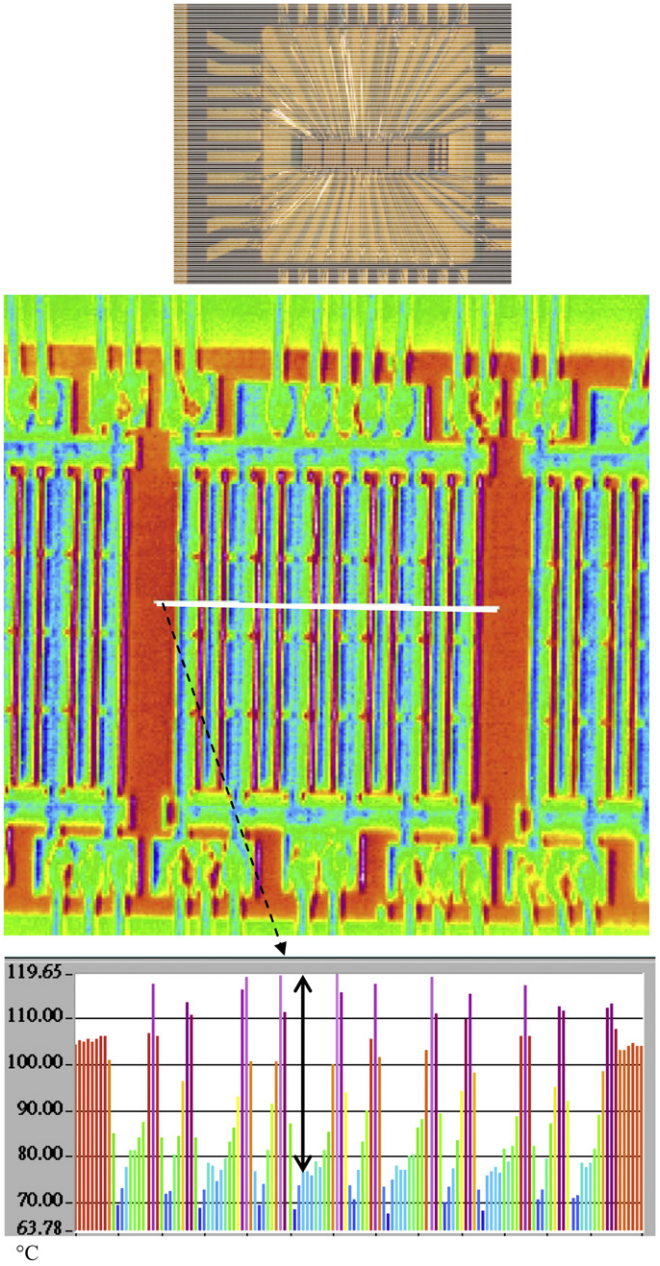

Fig. 6. Thermal infrared temperature map and line scan profile of GaN HEMTs on Si substrate bonded on flat plate package.

remove heat from the chip. The heat in the transistor is generated in the GaN two-dimensional electron gas (2DEG) channel by self-heating effect and localized hot spots arise in a region with a diameter of 0.5 μm near the gate contact.

4. Conclusion

The GaN HEMTs on the Si substrate packaged with a V-groove Cu base and mounted on a TO-3P leadframe showed improved thermal conductivity. Analysis of IR thermal images showed improved thermal spreading on the transistor side when thermal resistance from the chip through the conductive paint to the Cu base is reduced. In a device fabricated with the same drive condition, the proposed approach obtains a 19.6% lower thermal resistance compared to DIP package. The V-groove packaging technique supports effective thermal management and minimizes self-heating effects. The IR-measured peak temperature of V-groove packaged device is lower than the maximum operating junction temperature of DIP, and does not cause degradation issues. These IR thermal analyses reveal that the peak channel temperature occurs closed to the drain side of the gate contact owing to Joule heating. This work provides useful information to aid in designing high efficiency package for GaN HEMTs on Si.

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References

[1] D.C. Dumka, P. Saunier, GaN on Si HEMT with 65% power added efficiency at 10 GHz, Electron. Lett. 46 (13) (2010) 946–947.
[2] Ryan J. McGlen, Roshan Jachuck, Song Lin, Integrated thermal management techniques for high power electronic devices, Appl. Therm. Eng. 24 (2004) 1143–1156.
[3] C.-T. Chang, H.T. Hsu, E.Y. Chang, Y.-C. Chen, H.-D. Trinh, K.J. Chen, Normally-off operation AlGaN/GaN MOS-HEMT with high threshold voltage, Electron. Lett. 46 (18) (2010) 1280–1281.
[4] C.-Ta. Chang, H.T. Hsu, E.Y. Chang, C.I. Kuo, J.C. Huang, C.Y. Lu, Y. Miyamoto, 30-GHz low-noise performance of 100-nm-gate-recessed n-GaN/AlGaN/GaN HEMTs, IEEE Elec. Device Lett. 31 (2) (2010) 105–107.
[5] W. Chen, C. Zhou, K.J. Chen, High-current-density high-voltage normally-off AlGaN/GaN hybrid-gate HEMT with low on-resistance, Electron. Lett. 46 (24) (2010) 1626–1627.
[6] Aram Mkhitarian, Vincent Ngo, Florian Baltac, and Huoping Xin. 200 W discrete GaN HEMT power device in a 7 × 7 mm CMC package, Proceedings of the 4th European Microwave Integrated Circuits Conference, 2009, pp. 97–100.
[7] H.Y. Zhang, Y.C. Mui, M. Tarin, Analysis of thermoelectric cooler performance for high power electronic packages, Appl. Therm. Eng. 30 (2010) 561–568.
[8] Marco Lorenzini, Giampietro Fabbri, Sandro Salvigni, Performance evaluation of a wavy-fin heat sink for power electronics, Appl. Therm. Eng. 27 (2007) 969–975.