A Novel Charge-Trapping-Type Memory With Gate-All-Around Poly-Si Nanowire and HfAlO Trapping Layer

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***Abstract*—Hf-based charge-trapping (CT) layers, including HfO_2 and HfAlO, were employed in the fabrication of a CT-type memory with gate-all-around (GAA) poly-Si nanowire channels. It is shown that the GAA configuration can greatly enhance the programming/erasing efficiency as compared with the conventional planar scheme. It is also shown that the incorporation of Al into the dielectric can further improve the retention and endurance characteristics over the counterparts with a HfO_2 trapping layer. Retardation of the recrystallization of the dielectric film with Al incorporation is postulated to be responsible for these observations.**

***Index Terms*—Charge-trap memory, endurance, gate-all-around (GAA), HfAlO, nanowire (NW), retention.**

I. Introduction

CHARGE-trapping (CT)-type memory is regarded as one of the most promising candidates to replace floating-gate memory due to its superior scaling capability [1]. Recently, high-κ dielectrics such as HfO_2 and Al_2O_3 have been explored to replace nitride in silicon–oxide–nitride–oxide–silicon (SONOS) as the CT layer [2]. Implementation of a high-κ trapping layer tends to improve the programming/erasing (P/E) efficiency due to the reduced equivalent oxide thickness and may improve data retention because of the favorable band structure. According to previous studies [2], [3], the density of trapping sites in HfO_2 is large, while the Al_2O_3 trapping layer provides good retention capability due to its deeper trap states. It has also been reported that the HfAlO trapping layer can preserve the advantages specifically pertaining to both HfO_2 and Al_2O_3 [4].

Despite the merits stated earlier, the devices characterized in the aforementioned works on exploring high-κ trapping layers were of conventional planar type. Concurrently, the nonplanar scheme like the gate-all-around (GAA) configuration is known to enhance the gate controllability and the tunneling probability through the tunnel oxide because of the increase in the surface curvature of the wrapped nanowire (NW) channel [5], [6]. In this work, to evaluate the impacts of both structure and trapping medium, GAA CT devices with poly-Si NW channels and various CT layers were fabricated and characterized. The poly-Si-based device technology is suitable for the construction of 3-D electronics.

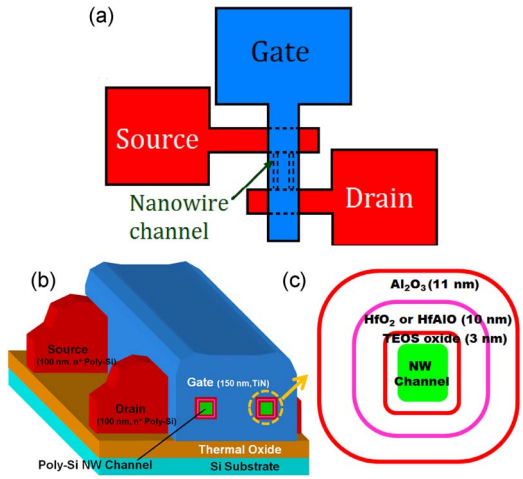

Fig. 1. (a) Top and (b) stereo views and (c) channel cross section of the CT-type memory with HfO_2 or HfAlO as the CT layer.

II. Device Fabrication

The top and stereo views of the CT-type memory devices are shown in Fig. 1(a) and (b), respectively. The fabrication process is basically the same as that described in our previous work on SONOS NW memory [7] except that the CT and blocking layers are substituted with HfAlO (or HfO_2) and Al_2O_3 dielectrics, respectively, as shown in Fig. 1(c). The high-κ layers were prepared by an atomic layer deposition system. The thicknesses of the tunnel oxide, CT layer, and blocking oxide of the devices are 3, 10, and 11 nm, respectively. The thicknesses of the n^+ poly-Si source/drain are 100 nm, and the gate electrode is 150-nm-thick TiN. The total width of the NW channel is around 85 nm. After the deposition of the gate dielectrics and electrodes, all devices were treated by a postmetallization annealing (PMA) at 600 °C for 30 s. For comparison, planar devices with the same dielectric stacks were also fabricated.

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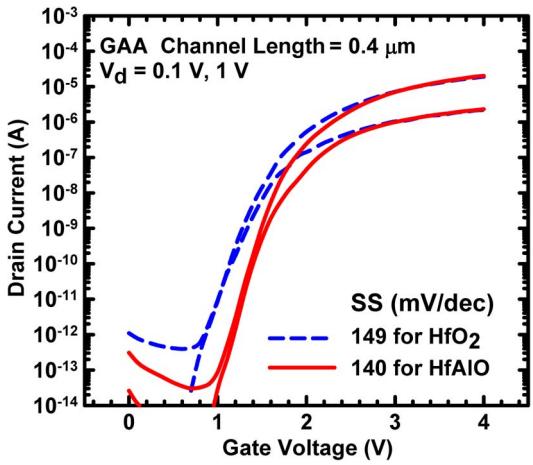

Fig. 2. Transfer characteristics of HfAlO and HfO_2 CT-type GAA NW devices.

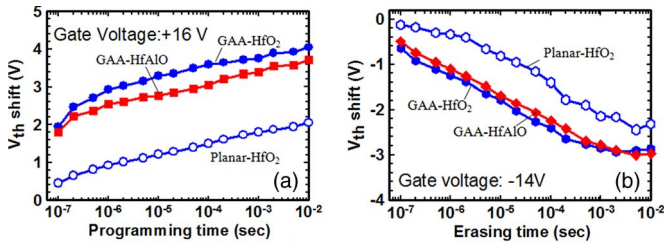

Fig. 3. Threshold voltage shift as a function of (a) programming and (b) erasing times for the fabricated GAA and planar devices.

III. Results and Discussion

For simplicity, the threshold voltage $(V_{\rm th})$ is obtained from the transfer curves with the drain current equal to 10^{-9} A at a V_d of 0.1 V. Fig. 2 shows the fresh transfer characteristics of HfAlO and HfO_2 memories at V_d's of 0.1 and 1 V. Both devices show a steep subthreshold swing (SS) of less than 150 mV/dec. The small SS and the negligible DIBL are attributed to the tiny NW channel and the GAA configuration.

For the P/E operation, a high voltage is applied to the gate while both source and drain are grounded. The typical P/E characteristics of the two kinds of GAA devices are shown in Fig. 3. To illustrate the merits of the GAA configuration, the characteristics of a planar device with HfO_2 storage medium are also included in the figures, and obviously, its performance lags far behind those of the GAA ones. The corresponding $V_{\rm th}$ shifts of programming (erasing) at 1 (100) μs are 3 (2.4) and 2.6 (2.3) V for the GAA HfO_2 and HfAlO devices, respectively.

Fig. 4 shows the retention characteristics of the fabricated GAA devices. As can be seen from the figure, the extrapolated window after ten years for the HfAlO device is about 2.2 V, which is much larger than that of the HfO_2 one ($\sim$1.2 V). One plausible reason for this observation is the difference in the crystallinity of the trapping layers. Zhu *et al.* have shown that the crystallization phenomenon of the HfO_2 dielectric starts at 300 °C [8]. It is thus expected that the HfO_2 trapping layer in the device is polycrystalline in nature. This nature renders the CT inside the material nonuniform since the defect density is larger at or near the grain boundaries (GBs). The excessive

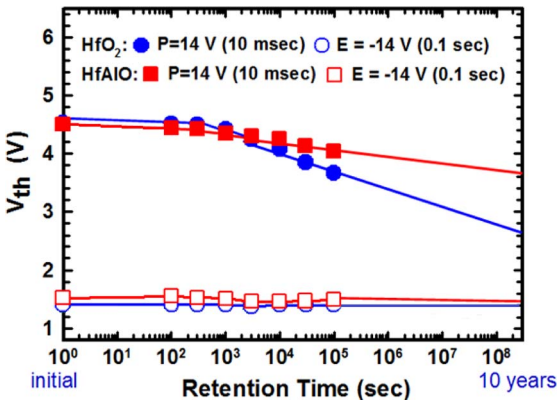

Fig. 4. Retention characteristics of the fabricated devices at room temperature. The solid and open symbols stand for programmed and erased devices, respectively. The HfAlO split shows superior retention characteristics.

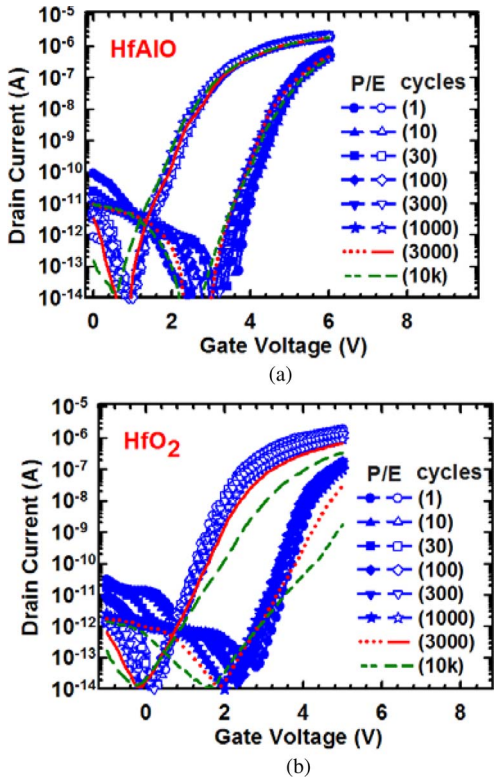

Fig. 5. Transfer characteristics of (a) HfAlO and (b) HfO_2 CT-type GAA NW devices.

trapped charges located close to the GBs would leak out faster due to the rise in electric potential locally. As Al is incorporated into the dielectric, the thermal stability is greatly promoted, and the recrystallization temperature is dramatically increased. Thus, the dielectric would remain in the amorphous state even after the 600 °C PMA treatment [2]. As a result, the nonuniform CT situation in the poly-HfO_2 could be eliminated, resulting in much improved retention. For each split, at least five samples were tested to confirm the observed trends.

The endurance of the GAA devices is also evaluated, and typical results are shown in Fig. 5(a) and (b) in which the transfer characteristics of the GAA HfAlO and HfO_2 devices, respectively, recorded at various P/E cycles (1–10 000) are presented. Obviously, the endurance performance of the HfAlO

memory outperforms that of the HfO_2 memory. The increase in SS leads to a positive shift in $V_{\rm th}$. Again, this is attributed to the polycrystalline phase of the HfO_2. Excessive charge trapping/detrapping events occurring near the GBs would degrade the nearby tunneling oxide, resulting in distorted I–V curves as the P/E cycle number increases. In contrast, the HfAlO device exhibits only minor changes in the transfer characteristics even after 10 000 P/E cycles.

IV. Conclusion

GAA NW CT-type memory devices with Hf-based trapping layers were fabricated and characterized. Equipped with the GAA configuration, the devices show much faster P/E speeds as compared with the planar counterparts. However, the GAA devices with the HfO_2 CT layer display worse retention and endurance performances as compared with the GAA HfAlO ones. Nonuniform CT due to the existence of the polycrystalline phase in the HfO_2 is postulated to be responsible for the reliability issues. In contrast, the GAA HfAlO memory shows an excellent extrapolated window of 2.2 V after ten years and only minor shift in the transfer curves even after 10^4 P/E cycles. This is attributed to the retardation of recrystallization with the incorporation of Al into the Hf-based dielectric. Based on the results, the GAA CT scheme with a HfAlO trapping layer is promising for the construction of 3-D high-density Flash memory in the future.

Acknowledgment

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