# Backside-Process-Induced Junction Leakage and Process Improvement of Cu TSV Based on Cu/Sn and BCB Hybrid Bonding

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*Abstract*—Wafer-level 3-D integration using Cu through-silicon vias (TSVs) and fine-pitch Cu/Sn–BCB hybrid bonding is investigated with electrical leakage current. With the well-fabricated Cu TSVs and Cu/Sn bond structures, the leakage current path in this scheme due to backside process was found, and the corresponding mechanism is discussed. The leakage current can be solved by the modified backside process. The improved 3-D integration scheme shows extremely low leakage current and no visible defects inside Cu TSV.

*Index Terms*—Hybrid bonding, leakage current, through-silicon via (TSV), 3-D integration.

## I. INTRODUCTION

THREE-dimensional integrated circuits have received widespread recognition as the most promising solution for the next semiconductor generation since this technology has the potential to break through the limitation of traditional 2-D scaling and provides a lot of merits, such as smaller form factor, lower power dissipation, lower transmission delay, and the great capability of heterogeneous integration [1], [2]. Several wafer-level 3-D integration schemes have been developed by using Cu through-silicon vias (TSVs) and bonding technologies for establishing the baseline of 3-D platforms vertically linked with several different functional blocks [3]–[9].

One wafer-level 3-D integration scheme with Cu TSVs and fine-pitch Cu/Sn-microbump-to-BCB hybrid bonding was proposed [9]. One advantage of the hybrid bonding integration scheme is low bonding temperature ($< 250$ °C) without any cracks and issue of underfilling. The simplified carrierless process can reduce cost, remove the risk of handling wafers, and increase yield and throughput. Exceptional results of reliability tests [10] indicate an excellent bonding strength against oxidation and corrosion through the BCB reinforcement. However,

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TABLE I
TSV PARAMETERS, INCLUDING VIA DIAMETER, PITCH, AND VIA DEPTH, AND CORRESPONDING RESULTS OF $A^*$ AND $R_S$

| TSV Design | | | | Results | |
|---|---|---|---|---|---|
| Type | Diameter | Depth | Pitch | $A^*$($\mu m^2$) | $R_S$( M$\Omega$) |
| A | 5μm | | 20μm | 3.03 | 1.45 |
| B | 10μm | 40μm | 40μm | 3.11 | 1.31 |
| C | 5μm | | 40μm | 1.57 | 1.87 |
| D | 10μm | | 80μm | 1.37 | 1.82 |

other than the quality of the bonding structure and TSV in this 3-D integration scheme, the integration of RDL and TSV using polymer as isolation may be challenging and needs extra attention.

In this letter, we investigate the backside-process-induced TSV leakage current, which might be ignored and not addressed in the fabrication of 3-D integration platforms. The procedure to verify the failure location and possible transport mechanism is described. The electrical characteristics and OBIRCH results simultaneously indicate that the leakage current comes from the Ti overlaying on Si. Finally, the improved backside process is developed and shows an extremely low leakage current in this 3-D integration platform.

## II. EXPERIMENT

The fabrication of this 3-D integration scheme employs the following key technologies: Cu TSVs, fine-pitch Cu/Sn microbumps, patterned BCB, hybrid bonding, wafer thinning, and backside RDL process. First, 200-mm silicon wafers were cleaned and lithographed for fabricating 5- and 10-$\mu$m Cu TSVs by using the sequence of 40-$\mu$m-deep DRIE for via opening, ~400-nm PE-TEOS oxide liner deposition, TiN/Cu deposition as barrier/seed layer, ECD Cu, and overburden CMP. To optimize the hybrid bonding quality, both silicon wafers were electroplated with 3-$\mu$m-thick Cu and then 2-$\mu$m-thick Sn for fabricating bumps with surrounding 4-$\mu$m-thick BCB. After the two wafers were face-to-face Cu/Sn-BCB hybrid bonded at 250 °C for 30 min under a contact force of 5000 mbar and a vacuum pressure of $10^{-3}$ torr, the top wafer was thinned down to 40 $\mu$m, followed by CMP to expose Cu TSVs. Finally, the wafer backside was covered with passivation polyimide (PI), Ti adhesion layer, and backside RDL to complete this wafer-level 3-D integration hybrid scheme. Table I lists the dimension and design of the TSV parameters, including via diameter, pitch, and TSV depth, used in this study.
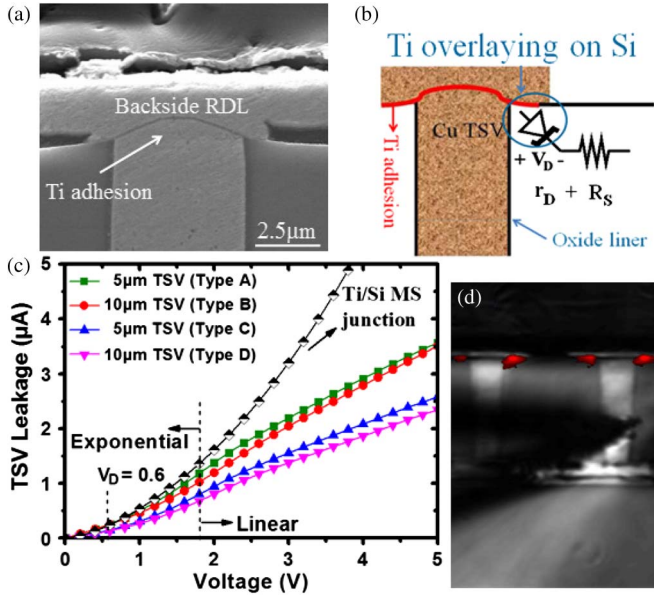
Fig. 1.    (a) SEM image of the backside RDL and Cu TSV (5-$\mu$m diameter and 40-$\mu$m depth), (b) schematic diagram of the leakage current path, (c) $I$–$V$ characteristics of Cu TSVs without process improvement, and (d) the leakage current location investigation of Cu TSV by OBIRCH analysis.

## III. RESULTS AND DISCUSSION

Fig. 1(a) shows the SEM image of the RDL and Cu TSV junction area. Passivation PI which provides the electrical isolation is patterned around Cu TSV. However, the large opening of passivation PI creates an unexpected contact area between the Ti adhesion layer of RDL and the Si substrate. As shown in Fig. 1(b), TSV leakage can be regarded as the injection current passing through the Ti/Si junction and forwarding toward the horizontal direction until it reaches another side. The following equations can theoretically express the overall resistance in series and the transport current [11]:

$$R_{\text{total}} = r_D + R_S = \left( A^* \cdot \frac{\partial J_{\text{MS}}}{\partial V} \right)^{-1} + R_S \qquad (1)$$

$$J_{\text{MS}} = J_S \left[ \exp\left( \frac{qV}{\eta kT} \right) - 1 \right]. \qquad (2)$$

Herein, $r_D$ is the Ti/Si junction resistance, $A^*$ is the effective junction area of adhesion Ti overlaying, $R_S$ is the series resistance of the current path under the isolation layer, and $J_S$ is the reverse-saturation current density [11].

An Agilent 4156C precision analyzer collocated with a two-point SMU system was applied on one Cu TSV with voltage sweeping from the ground to $V_{\text{dd}}$ (0–5 V), while the leakage current in the neighbor Cu TSV was simultaneously measured. The $I$–$V$ characteristics of the TSV leakage with 5- and 10-$\mu$m diameters for different pitches are summarized in Fig. 1(c). It could be readily seen that the larger pitch of both two TSV sizes in the $I$–$V$ plot exhibits the same decreased shift of the leakage current in the voltage region from 2 to 5 V, and the result of the 5-$\mu$m TSV is slightly lower than that of the 10-$\mu$m one. Moreover, no matter how the TSV size or pitch changes, the current always initially increases exponentially at low applied voltage and then becomes linear when the voltage is larger than
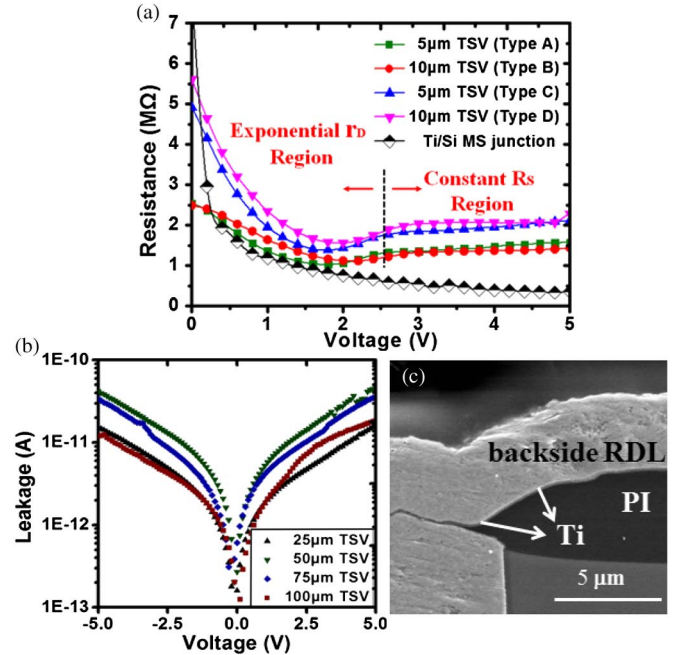


Fig. 2.    Electrical characterization of the 3-D integration scheme: (a) Two dominations of the $R$–$V$ characteristics, (b) $I$–$V$ characteristics of the structure using the improved process, and (c) SEM image of the structure using the improved backside process.

2 V. However, the large TSV leakage current ($>$ 3 $\mu$A at 5 V) injection into the substrate may cause large thermionic noise to interfere the property of device operation.

Since the scant information in the $I$–$V$ curve cannot explain its real transport behavior, location, path flow, and related parameters, OBIRCH analysis was applied to investigate the leakage current location, as shown in Fig. 1(d). As the applied voltage reaches 3 V, thermal sensitive laser points out that the accurate locations of leakage current are at corner junctions of the Cu TSV and backside RDL. It also indicates that the possible discharge path in this 3-D integration structure comes from the contact area of Ti from the RDL and the Si substrate, as shown in Fig. 1(b).

To further explore the mechanism of TSV leakage, one 50 $\mu$m $\times$ 50 $\mu$m Ti/Si metal–semiconductor junction was fabricated, and then, its normalized $I$–$V$ characteristics were measured, as shown in Fig. 1(c). The behavior of this Ti/Si junction can simulate the impact of the induced junction leakage current in TSV. Based on the characteristics of the fabricated metal-semiconductor Ti/Si junction, the TSV leakage should increase exponentially with the corresponding built-in $V_D = 0.6$ V.

The $R$–$V$ characteristics of the fabricated Ti/Si junction and Cu TSVs with different sizes/pitches can be obtained by the inverse of differential $I$–$V$, as shown in Fig. 2(a). All the TSV leakage curves present two main regions. It can be clearly inspected that, under low applied voltage, the large resistance of the Ti/Si metal-semiconductor junction results in an initial large TSV resistance. As the voltage increases, the resistance of the Ti/Si metal-semiconductor junction exponentially decreases. The effect of $r_D$ becomes minor, while the constant $R_S$ dominates the TSV leakage. Table I also lists the effective
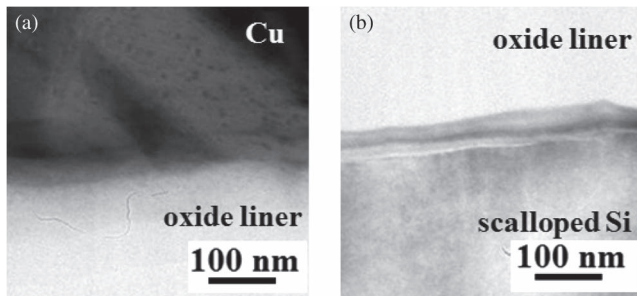
Fig. 3.  XTEM images in the middle of the TSV at (a) the copper side and (b) silicon side.

junction area $(A^*)$ of the TSV leakage and the pitch-relative $R_S$ extracted by using (1) and (2), respectively.

In order to decrease the leakage current, the adhesion layer of the Ti overlaying area $A^*$, which may come from overburden CMP, passivation PI, and backside Cu RDL, should be minimized. One improved fabrication using Si recessed and modified backside process can effectively achieve almost zero leakage current in this 3-D integration scheme. This modified approach has narrower via opening and thicker passivation PI layer. Fig. 2(b) shows the $I-V$ characteristics of the modified 3-D integration with different TSV sizes. All TSVs with the modified backside process have extremely low leakage current of 20 pA at 5 V, showing an excellent isolation property. In addition, Fig. 2(c) shows no Ti overlaying on Si in the TSV and RDL region using the modified backside process.

Cu TSV using the improved fabrication process was also investigated at different locations to ensure the overall insulation and filling quality. Fig. 3(a) and (b) shows the XTEM images in the middle of the TSV. There are no visible stacking fault around scalloped silicon and crack in the oxide liner, indicating that the leakage current inside the TSV should be extremely low, which is consistent with the measurement results.

## IV. CONCLUSION

In this letter, the backside-process-induced TSV leakage current in the 3-D integration scheme with Cu TSVs and Cu/Sn–BCB hybrid bonding has been investigated. The leakage current was inspected by OBIRCH analysis and compared with the typical Ti/Si metal–semiconductor junction current. These results identified the leakage location and proved the mechanism proposed. One improved process was employed in Cu TSVs, showing extremely low leakage current without visible defects. The improved Cu TSV scheme provides the fabrication feasibility in 3-D integration applications.

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