Design of Dual-Band ESD Protection for 24-/60-GHz Millimeter-Wave Circuits

Li-Wei Chu, *Student Member, IEEE*, Chun-Yu Lin, *Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—To effectively protect the millimeter-wave (MMW) circuits in nanoscale CMOS technology from electrostatic discharge (ESD) damages, a dual-band ESD protection cell for 24-/60-GHz ESD protection is presented in this paper. The proposed ESD protection cell consisted of a diode, a silicon-controlled rectifier, a PMOS, and two inductors. To verify the dual-band characteristics and ESD robustness, the proposed ESD protection circuit had been applied to a 24-/60-GHz low-noise amplifier (LNA). The measurement results showed over-2-kV human-body-model ESD robustness with little performance degradation on LNA. The proposed dual-band ESD protection cell was suitable for circuit designers for them to easily apply ESD protection in the dual-band MMW circuits.**

***Index Terms*—CMOS, dual-band, electrostatic discharge (ESD) protection, millimeter-wave (MMW), radio frequency (RF).**

I. Introduction

A CLEAR trend in wireless applications during recent years has been pushing toward to higher integration and multi-band operation, in order to enable low-cost high-functionality. Millimeter-wave (MMW) circuits become more attractive for many applications such as automotive radar sensors at 24/77 GHz and wireless communications at 24/60 GHz [1], [2]. Several dual-band MMW transceivers operated at these frequency bands have been realized [3], [4]. Nanoscale CMOS technologies have been widely used to implement radio-frequency (RF) and MMW circuits with the advantages of scaling-down feature size, improving high-frequency characteristics, low power consumption, high integration capability, and low cost for mass production. However, the thinner gate oxide in nanoscale CMOS technology seriously degrades the ESD robustness of IC products [5]. Therefore, on-chip ESD protection circuits must be added at all input/output (I/O) pads in ICs [6]–[10]. To support the dual-band MMW applications and to lower the fabrication costs, a dual-band ESD protection cell is needed. Fig. 1 presents the dual-band ESD protection circuit which is added to the input $(RF_{\rm IN})$ pad of the dual-band low-noise amplifier (LNA) against ESD damages. To minimize the impacts from the dual-band ESD protection circuit on RF performances, the dual-band ESD protection circuit at the input pads should be carefully designed.

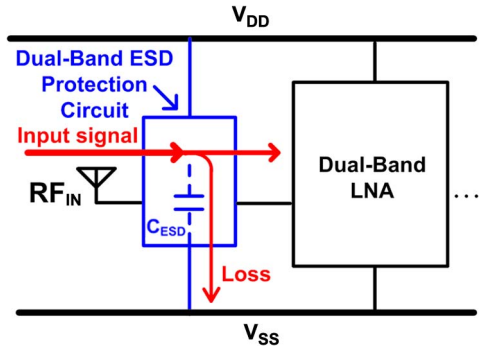


Fig. 1. Dual-band ESD protection circuit added to the input $(RF_{\rm IN})$ pad of dual-band LNA against ESD damages.

ESD protection devices cause the circuit performance degradation with several undesired effects [11]–[13]. The parasitic capacitance $(C_{\rm ESD})$ of the ESD protection device is one of the most important design considerations for MMW circuits. Conventional ESD protection devices with large dimensions have large parasitic capacitances, which are difficult to be well tolerated in the MMW circuits. The parasitic capacitance will cause signal loss from the pad to ground. Moreover, the parasitic capacitance will change the input matching condition. Besides, adding an ESD protection device to the MMW receiver will degrade the noise figure. As the operating frequencies of MMW circuits are further increased, on-chip ESD protection designs for MMW circuits are more challenging. Among the ESD protection devices, silicon-controlled rectifier (SCR) device has been reported to be useful for RF ESD protection design due to its high ESD robustness within a small layout area and low parasitic capacitance [6], [14]–[16]. Besides, the SCR device typically has a holding voltage of $\sim$1.5 V in the bulk CMOS processes [14], while the supply voltage $(V_{\rm DD})$ has been reduced to 1 V in a 65-nm CMOS process, so the SCR can be safely used without latchup danger. The device structure of the SCR device used in RF input $(RF_{\rm IN})$ pad is illustrated in Fig. 2. The SCR path between $RF_{\rm IN}$ and $V_{\rm SS}$ consists of P+, N-well, P-well, and N+. Besides, the parasitic diode path between $RF_{\rm IN}$ and $V_{\rm DD}$ consists of P+ and N-well/N+. However, SCR has some drawbacks, such as higher trigger voltage and slower turn-on speed. To reduce the trigger voltage of an SCR device, the trigger signal can be sent to

Manuscript received June 30, 2012; revised August 27, 2012; accepted August 28, 2012. Date of publication September 6, 2012; date of current version March 7, 2013. This work was supported in part by Taiwan Semiconductor Manufacturing Company, by the National Science Council of Taiwan under Contract NSC 101-2221-E-009-141, and by the "Aim for the Top University Plan" of National Chiao Tung University and the Ministry of Education of Taiwan.

L.-W. Chu is with the Department of Photonics and the Display Institute, National Chiao Tung University, Hsinchu 300, Taiwan.

C.-Y. Lin and M.-D. Ker are with the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: cy.lin@ieee.org; mdker@ieee.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TDMR.2012.2217498

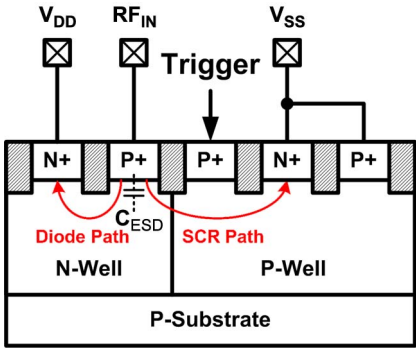


Fig. 2. Device cross-sectional view of SCR device used in $RF_{\rm IN}$ pad.

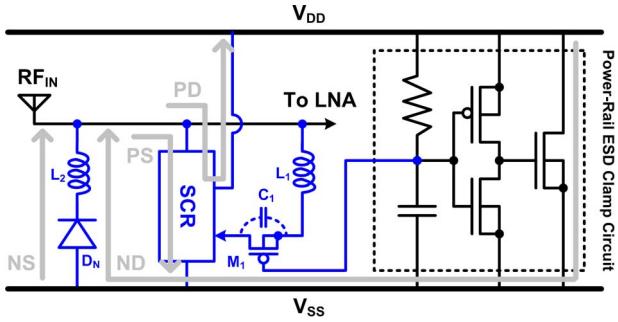


Fig. 3. Proposed dual-bad ESD protection scheme for $RF_{\rm IN}$ pad.

enhance the turn-on speed. Some design techniques have been reported to enhance the turn-on efficiency of SCR devices [14]. However, adding a trigger circuit to SCR device also increases the parasitic capacitance seen at the $RF_{\rm IN}$ pad, which is hard to tolerate for MMW circuits. In this paper, a novel SCR design is proposed for dual-band ESD protection at 24/60 GHz. Such ESD protection circuits have been successfully designed and applied to 24-/60-GHz LNA in a 65-nm CMOS process [17].

II. Proposed Dual-Band ESD Protection Designs

The proposed dual-band ESD protection cell is shown in Fig. 3, which consists of a diode $(D_{\rm N})$, an SCR, a PMOS (M_1), two inductors (L_1 and L_2), and a power-rail ESD clamp circuit. The L_1 is used to provide the trigger path between the $RF_{\rm IN}$ pad and the trigger port of the SCR device under ESD stress conditions. The resistor and capacitor used in the power-rail ESD clamp circuit are used to control the M_1. The M_1 at the trigger path is also turned on under ESD stress conditions. When the trigger signal passes from the $RF_{\rm IN}$ pad to the trigger port of the SCR device, the SCR device can be quickly turned on to discharge the ESD current. Fig. 3 also shows the ESD current paths under positive-to-$V_{\rm SS}$ (PS), positive-to-$V_{\rm DD}$ (PD), negative-to-$V_{\rm SS}$ (NS), and negative-to-$V_{\rm DD}$ (ND) ESD stress conditions. During PS ESD stress, ESD current will first pass through the L_1 and M_1 to trigger the SCR device. Since the L_1 used in this work is in the order of nH, the trigger current under ESD stress condition will not be blocked by L_1. The major ESD current will be discharged by the SCR device from the $RF_{\rm IN}$ pad to $V_{\rm SS}$. Under PD ESD stress, the ESD current will be discharged by the parasitic diode path embedded in the SCR device from the $RF_{\rm IN}$ pad to $V_{\rm DD}$. During NS ESD stress, the ESD current will be discharged by the forward-biased $D_{\rm N}$ and L_2 from the $V_{\rm SS}$ to $RF_{\rm IN}$ pad. Under ND ESD stress, the ESD current will be discharged by the power-rail ESD clamp circuit, $D_{\rm N}$, and L_2 from $V_{\rm DD}$ to $RF_{\rm IN}$ pad. The proposed dual-band ESD protection scheme in Fig. 3 can provide the corresponding current discharging paths with good ESD robustness.

Under normal power-on conditions, the M_1 is turned off to block the steady leakage current path from the $RF_{\rm IN}$ pad to the trigger port of SCR device. Under normal circuit operating conditions, there are two series LC resonators in this circuit. The resonant frequency of series L_1 and C_1 is designed < 24 GHz, while that of the series L_2 and $C_{\rm D}$ is designed at $24 \sim 60$ GHz, where C_1 and $C_{\rm D}$ denote the capacitances of M_1 and $D_{\rm N}$, respectively. As the frequency is higher than the resonant frequency of first series LC resonator and lower than that of second series LC resonator, the equivalent inductance $(L_{\rm eq1})$ of the first series LC resonator can be expressed as

$$L_{eq1} = L_1 - \frac{1}{\omega^2 C_1} \tag{1}$$

and the equivalent capacitance $(C_{\rm eq2})$ of the second series LC resonator can be expressed as

$$C_{eq2} = \frac{C_D}{1 - \omega^2 L_2 C_D} \tag{2}$$

where the ω is the angular frequency. The $L_{\rm eq1}$ can be used to eliminate the $C_{\rm eq2}$ and $C_{\rm ESD}$, where the $C_{\rm ESD}$ is the parasitic capacitance contributed by the SCR. The resonant frequency of parallel $L_{\rm eq1}$, $C_{\rm eq2}$, and $C_{\rm ESD}$, which is designed to be the first operating frequency (ω_{o1}) of MMW circuit, can be obtained by

$$\omega_{o1} = \frac{1}{\sqrt{L_{eq1}(C_{eq2} + C_{ESD})}}. \tag{3}$$

Similarly, as the frequency is higher than the resonant frequency of second series LC resonator, the inductance dominated the impedance. The equivalent inductance $(L_{\rm eq2})$ of second series LC resonator can be expressed as

$$L_{eq2} = L_2 - \frac{1}{\omega^2 C_D}. \tag{4}$$

The resonant frequency of parallel $L_{\rm eq1}$, $L_{\rm eq2}$, and $C_{\rm ESD}$, which is designed to be the second operating frequency (ω_{o2}) of MMW circuit, can be obtained by

$$\omega_{o2} = \frac{1}{\sqrt{(L_{eq1} // L_{eq2}) C_{ESD}}}. \tag{5}$$

The sizes of SCR and $D_{\rm N}$ depend on the required ESD robustness, while the size of M_1 depends on the required trigger current. Once the sizes of M_1, SCR, and $D_{\rm N}$ have been chosen, the required inductors (L_1 and L_2) can be determined through (1)–(5).

TABLE I
DEVICE DIMENSIONS AND MEASUREMENT RESULTS OF DUAL-BAND ESD PROTECTION CELLS

	Test Circuits	
	A	B
SCR (μm)	8	30
D_N (μm)	8	30
L_1 (nH)	0.58	0.58
L_2 (nH)	0.35	0.21
M_1 (μm / μm)	90/0.2	90/0.2
Area (μm x μm)	100x200	100x180
S_{11} at 24 GHz (dB)	-19.0	-18.5
S_{11} at 60 GHz (dB)	-15.6	-15.5
S_{21} at 24 GHz (dB)	-1.29	-1.35
S_{21} at 60 GHz (dB)	-1.22	-1.57
PS HBM (kV)	0.50	2.25
PD HBM (kV)	0.75	2.50
NS HBM (kV)	0.75	2.25
ND HBM (kV)	0.75	2.25

III. SIMULATION AND MEASUREMENT RESULTS OF PROPOSED DUAL-BAND ESD PROTECTION DESIGNS

A. Test Circuits

The test circuits have been designed and fabricated in a 65-nm CMOS process. The test patterns include the test circuits A and B. The device dimensions of the test circuits are listed in Table I. The size of SCR device used in the test circuits A and B are split as 8 μm and 30 μm, respectively. The size of $D_{\rm N}$ in test circuits A and B are also split as also 8 μm and 30 μm, respectively. The width/length of M_1 in each test circuit is kept at 90 μm/0.2 μm. Therefore, the required $L_1(L_2)$ are 0.58 nH (0.38 nH) and 0.58 nH (0.2 nH) for the test circuits A and B, respectively. Fig. 4 shows one chip photograph of test circuit B with cell size of 100 $\times$ 180 μm^2.

B. Circuit Performances

The performances of the test circuits are simulated by using the microwave circuit simulator ADS with the selected device dimensions. Since the SCR model is not provided in the given CMOS process, diodes with P+/N-well, N+/P-well, and N-well/P-well junctions are used to simulate the SCR devices. A signal source with 50-Ω impedance drives the port 1 ($RF_{\rm IN}$ pad) of the test circuit, and a 50-Ω load is connected to the port 2 to simulate the LNA. The voltage supply of $V_{\rm DD}(V_{\rm SS})$ is 1 V (0 V), and the dc bias of $RF_{\rm IN}$ is 0.5 V. The simulated reflection (S_{11}) parameters are shown in Fig. 5. These dual-band ESD protection circuits exhibit good input matching $(S_{11}-\text{parameters} < -10$ dB$)$ around 24 GHz and 60 GHz.

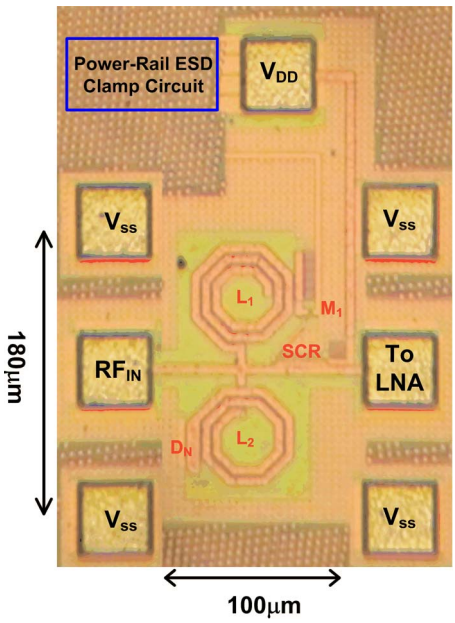


Fig. 4. Chip micrograph of test circuit B.

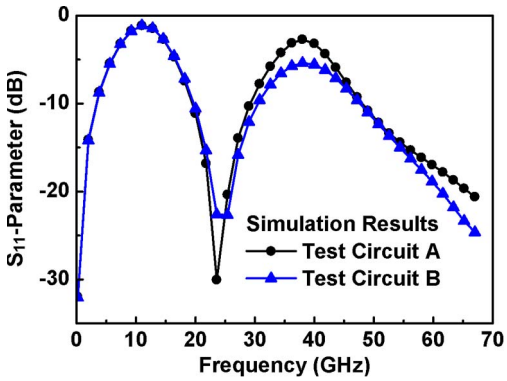


Fig. 5. Simulation results of the proposed dual-band ESD protection scheme on S_{11}-parameter.

The transmission (S_{21}) parameters around 24 GHz and 60 GHz are shown in Fig. 6(a) and (b). At 24 GHz (60 GHz) frequency, the test circuits A and B have about 0.91 dB (1.057 dB) and 1.232 dB (1.384 dB) power loss, respectively. Although the parasitic capacitance of the ESD protection devices can be resonated out, the losses are still contributed by the parasitic resistance of the SCR and $D_{\rm N}$.

With the on-wafer RF measurement, the S-parameters of these fabricated test circuits have been extracted from 0 to 67 GHz. The voltage supply of $V_{\rm DD}(V_{\rm SS})$ is 1 V (0 V), and the dc bias of $RF_{\rm IN}$ is 0.5 V $(V_{\rm DD}/2)$. The source and load resistances to the test circuits are kept at 50-Ω. In order to extract the intrinsic characteristics of the test circuits in high frequencies, the parasitic effects of the G–S–G pads have been removed by using de-embedding technique. The measured S_{11}-parameters and S_{21}-parameters versus frequencies of the two test circuits are shown in Figs. 7 and 8, respectively. As shown in Fig. 7, these ESD protection circuits exhibit good input matching $(S_{11}-\text{parameters} < -15$ dB$)$ around 24 or 60 GHz. At 24 GHz (60 GHz), the test circuits A and B have

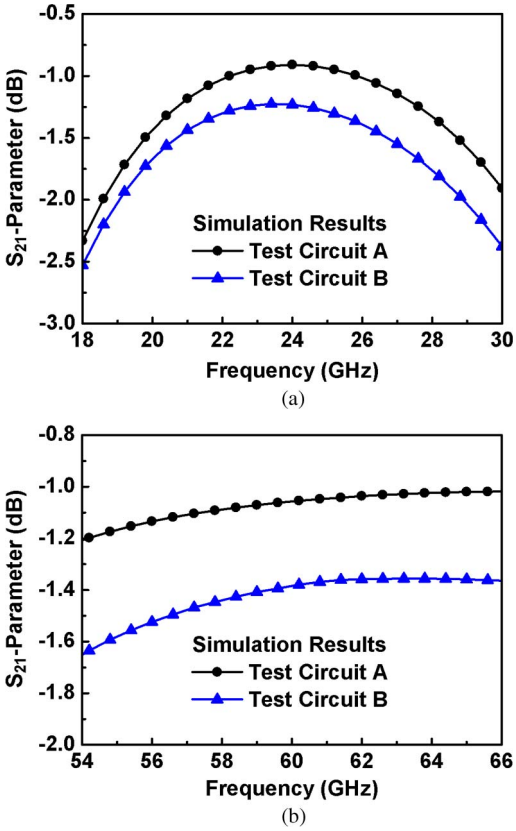


Fig. 6. Simulation results of the proposed dual-band ESD protection scheme on S_{21}-parameter around (a) 24 GHz and (b) 60 GHz.

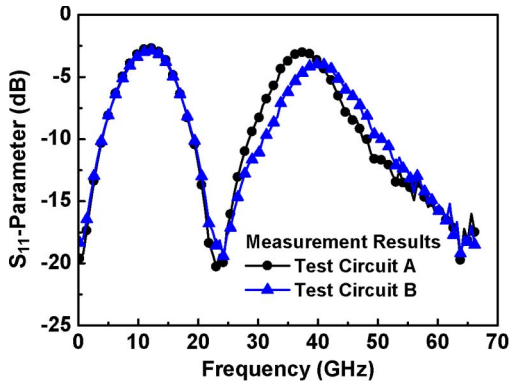


Fig. 7. Measured S_{11}-parameters of the two test circuits with the proposed ESD protection scheme under different device dimensions.

about 1.29 dB (1.22 dB) and 1.35 dB (1.57 dB) power loss, respectively.

C. ESD Robustness

The human-body-model (HBM) ESD pulses are stressed to each test circuit under PS, PD, NS, and ND ESD stress conditions. The failure criterion is defined as the I–V characteristics seen at $RF_{\rm IN}$ shifting over 30% from its original curve after ESD stressed at every ESD test level. The HBM ESD robustness of the two test circuits with the proposed ESD protection designs are listed in Table I. The HBM ESD levels of the proposed ESD protection circuits A and B can achieve

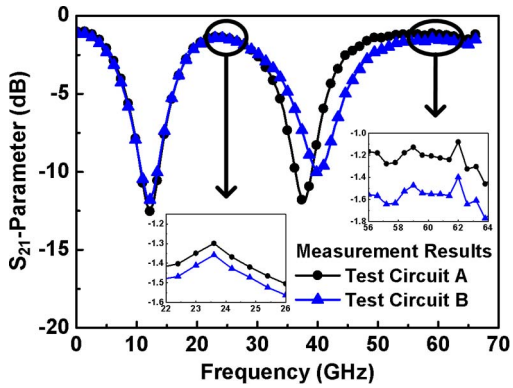


Fig. 8. Measured S_{21}-parameters of the two test circuits with the proposed ESD protection scheme under different device dimensions.

0.5 kV and 2.25 kV, respectively, which are obtained from the lowest levels among PS, PD, NS, and ND ESD tests. The HBM ESD robustness of the test circuits is almost proportional to the sizes of ESD protection devices.

The I–V characteristics of the ESD protection cells in high-current regions were characterized by using the transmission line pulsing (TLP) system with 10-ns rise time and 100-ns pulse width [18]. Fig. 9 shows the TLP-measured I–V curves of the fabricated ESD protection cells under PS-mode, PD mode, NS mode, and ND mode tests, respectively. The secondary breakdown currents (It_2) indicated the current-handling ability of ESD protection cells were obtained from the TLP-measured I–V curves. The secondary breakdown currents of ESD protection cells are listed in Table II.

To further investigate the effectiveness of the proposed dual-band ESD protection circuit in faster ESD-transient events, another very fast TLP (VF-TLP) system is also used with 0.2-ns rise time and 1-ns pulse width. The VF-TLP system can be used to capture the transient behavior of ESD protection circuits in the time domain of charged-device-model (CDM) ESD event [19]. The VF-TLP-measured It_2 of the proposed circuits are also listed in Table II. The tests circuits A and B under PS-mode tests can achieve VF-TLP-measured It_2 of 1.3 A and 2.88 A, respectively. The measured peak overshoot voltage versus VF-TLP current under such fast-transient CDM-like stress condition is shown in Fig. 10. When the VF-TLP pulse applied to $RF_{\rm IN}$ pad under PS-mode test, the maximum voltage overshoot on the $RF_{\rm IN}$ pad is 15.2 V (24.3 V) in the test circuit A (B) with 1.3-A (2.88-A) current passing through it, as shown in Fig. 10. These results determine that the proposed dual-band ESD protection circuits with inductor-triggered SCR are fast enough to be turned on among fast impulse response.

IV. Application to 24/60 GHz LNA

A. Implementation

One 24-/60-GHz dual-band LNA has been designed and fabricated in a 65-nm CMOS technology for verification. Fig. 11 shows the circuit schematic of the 24-/60-GHz LNA with the proposed dual-band ESD protection circuit. In order to implement 24-/60-GHz LNA without applying MOS switches, two LNAs (24 GHz and 60 GHz) are designed in parallel

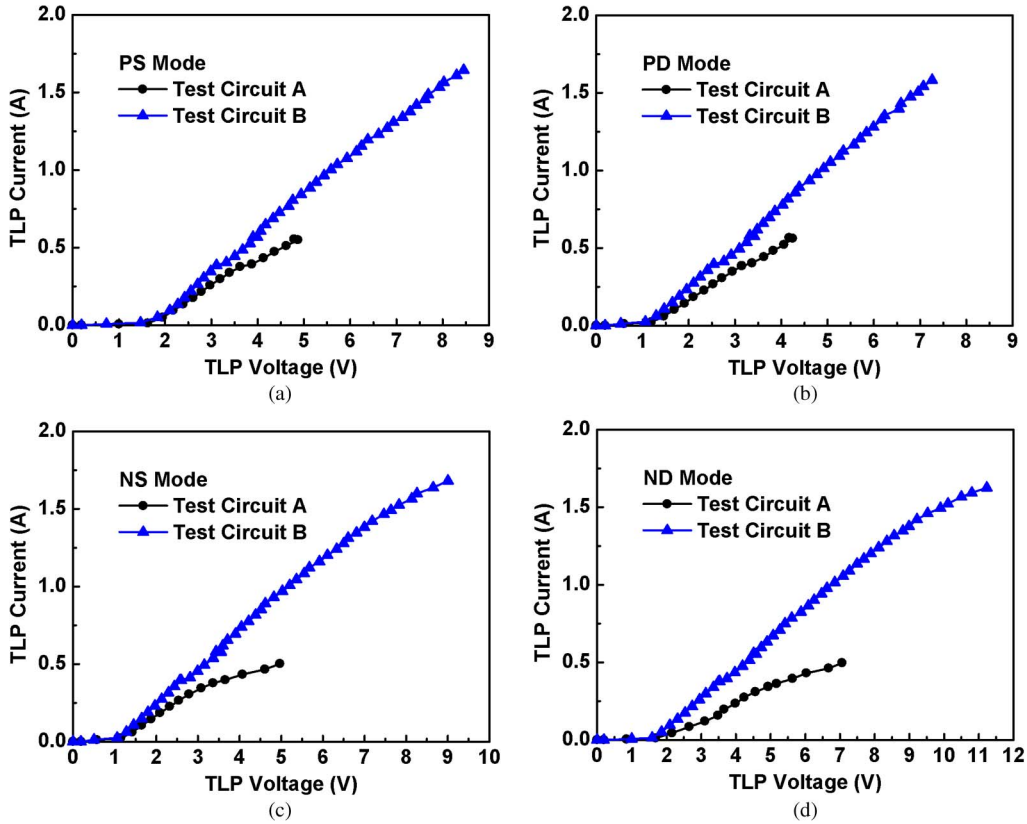


Fig. 9. TLP-measured I–V characteristics of the two test circuits with proposed dual-band ESD protection scheme under (a) PS-mode, (b) PD mode, NS mode, and (d) ND mode tests.

TABLE II
TLP-MEASURED AND VF-TLP-MEASURED I–V CHARACTERISTICS AMONG FOUR TEST CIRCUITS

TLP-Measured It_2 (A)	Test Circuits	
	A	B
PS Mode	0.55	1.64
PD Mode	0.57	1.58
NS Mode	0.50	1.68
ND Mode	0.57	1.63
VF-TLP-Measured It_2 (A)	**Test Circuits**	
	A	**B**
PS Mode	1.30	2.88
PD Mode	1.76	3.39
NS Mode	1.78	3.50
ND Mode	1.10	2.55

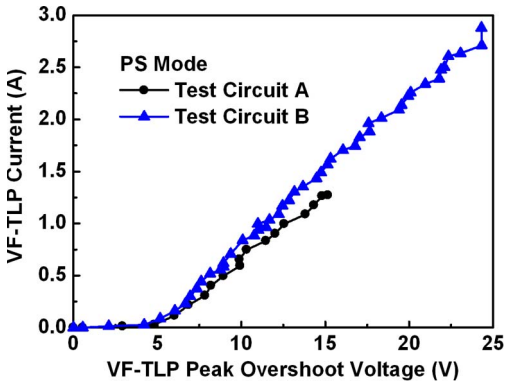


Fig. 10. VF-TLP-measured peak overshoot voltage of the two test circuits with proposed dual-band ESD protection scheme under PS-mode tests.

using single $RF_{\rm IN}$ and $RF_{\rm OUT}$ [20]. Each LNA consists of two-stages and the cascode configuration is applied to achieve high gain performance. Besides, the common-source and common-gate NMOS transistors are all with 56-μm gate width and 0.06-μm gate length. The ESD protection circuits A and B are applied to the 24-/60-GHz LNA circuit (LNA with ESD A and LNA with ESD B). The layout size of one circuit is 800 $\times$ 750 μm^2, including all testing pads and dummy layers. The dummy layers are kept away from the signal paths, so they will not influence the RF signals. In order to verify the RF characteristics and ESD robustness, the stand-alone LNA without ESD protection is also fabricated for comparison. The simulation results show that the gains (S_{21}) of stand-alone LNA, LNA with ESD A, and LNA with ESD B at 24/60 GHz are 16.5/11.9 dB, 15.9/11.3 dB, and 15.4/10.9 dB, respectively. The simulated noise figures of stand-alone LNA, LNA with ESD A, and LNA with ESD B at 24/60 GHz are 4.1/5.5 dB, 5.3/6.6 dB, and 5.5/7.3 dB, respectively. The power consumption of each LNA is 85 mW.

All the LNA circuits with and without ESD protection circuits are fabricated on the same wafer for comparison. Fig. 12

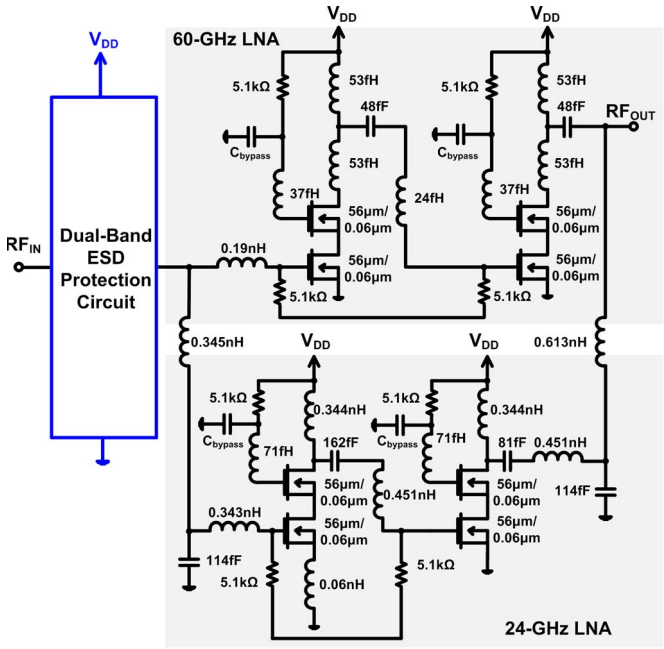


Fig. 11. Circuit schematic of 24-/60-GHz LNA with dual-band ESD protection circuit.

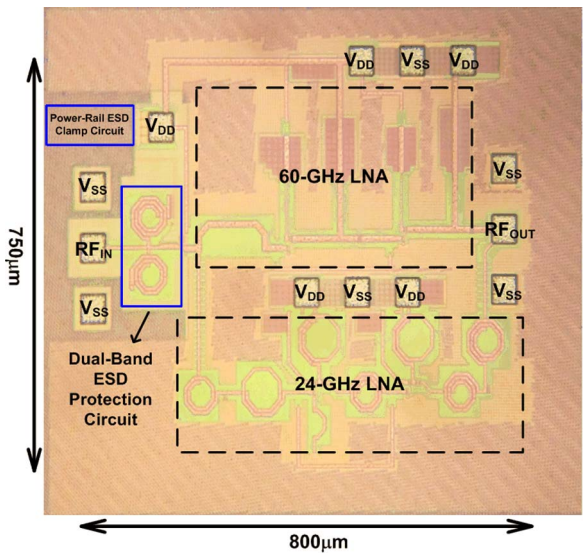


Fig. 12. Chip photograph of 24-/60-GHz LNA with ESD B.

shows a chip photograph of the 24-/60-GHz LNA with the ESD protection circuit B.

B. Circuit Performances Before ESD Tests

The RF characteristics are measured on wafer through G–S–G microwave probes with 100-μm pitch. The short–open–load–thru calibration has been done before the measurements. The gate bias of the designed 24-/60-GHz LNA is 0.73 V through bias tee at $RF_{\rm IN}$ and total dc power consumption is 88 mW under 1-V $V_{\rm DD}$ power supply. The measured S_{11}- and S_{21}-parameters of the dual-band LNA circuits are shown in Figs. 13 and 14, respectively. Although the operating frequencies of LNA are shifted to lower frequencies, the ESD

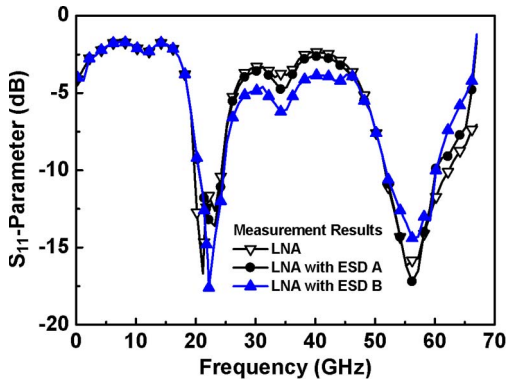


Fig. 13. Measured S_{11}-parameters of the dual-band LNAs with and without ESD protection circuits.

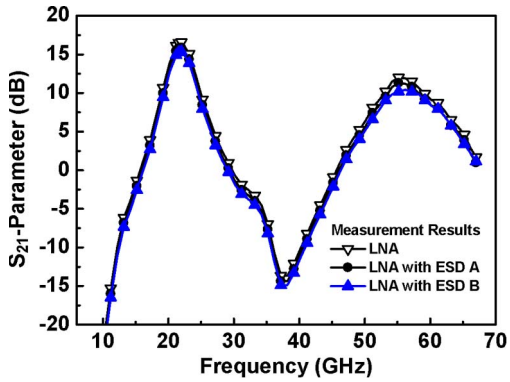


Fig. 14. Measured S_{21}-parameters of the dual-band LNAs with and without ESD protection circuits.

protection cells still can provide suitable ESD protection with only slight degradation on RF performances.

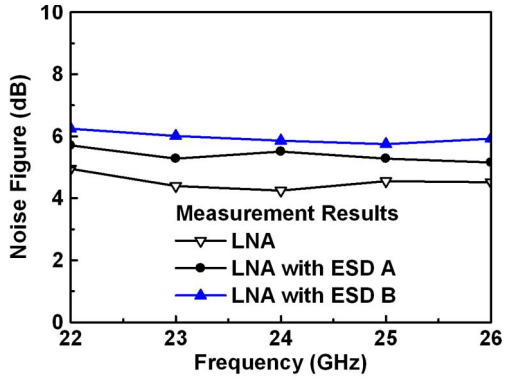
Under the same bias condition, the noise figures of the LNA with and without ESD protection circuits are shown in Fig. 15. The measured noise figures of stand-alone LNA, LNA with ESD A, and LNA with ESD B at 24/60 GHz are 4.3/6.1 dB, 5.5/7.4 dB, and 5.9/8.4 dB, respectively.

C. ESD Robustness

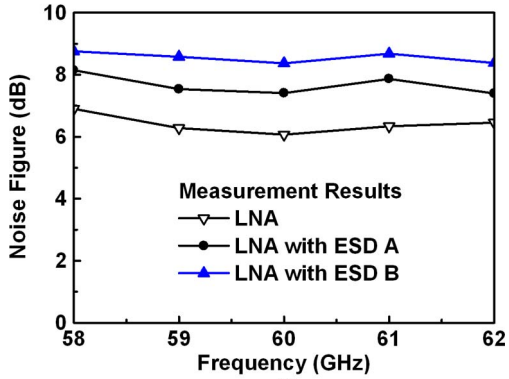
To compare the ESD robustness of the LNA with and without ESD protection circuits, the results of the HBM ESD stresses are shown in Table III. The LNA without ESD protection only sustains a very low ESD protection level ($<$ 100 V), which is far below the ESD specifications for commercial ICs. The ESD robustness of the LNA is substantially improved after inserting the proposed dual-band ESD protection circuit. The enhancement of ESD robustness is significant in that LNA with ESD A and ESD B achieve the HBM ESD level of 0.8-kV and 2.75-kV, respectively.

D. Circuit Performances After ESD Tests

The RF performances of all LNA circuits after ESD tests are re-measured and summarized in Tables IV–VI. All PS, PD, NS, and ND HBM ESD stresses are zapped to $RF_{\rm IN}$ pad of each test circuit. The stand-alone LNA is severely degraded after 100-V HBM ESD tests. In contrast, the LNA with ESD A and



(a)



(b)

Fig. 15. Measured noise figures of the dual-band LNAs with and without ESD protection circuits around (a) 24 GHz and (b) 60 GHz.

TABLE III
TEST RESULTS OF HBM ESD ROBUSTNESS AMONG LNA

HBM ESD Robustness (kV)	Mode			
	PS	PD	NS	ND
LNA	< 0.1	< 0.1	< 0.1	< 0.1
LNA with ESD A	1	1	0.9	0.8
LNA with ESD B	3	3	3	2.75

TABLE IV
MEASURED S_{21} AT 24/60 GHz OF LNA AFTER ESD TESTS

HBM ESD Tests	LNA	LNA with ESD A	LNA with ESD B
100 V	1.8 / 1.1 dB	14.4 / 9.2 dB	13.9 / 9.0 dB
500 V	Failed	14.4 / 9.3 dB	13.8 / 8.9 dB
750 V	Failed	9.5 / 3.6 dB	13.9 / 9.1 dB
2.5 kV	Failed	Failed	13.9 / 9.0 dB
2.75 kV	Failed	Failed	9.8 / 5.5 dB

that with ESD B are still excellent matching after 500-V and 2.5-kV HBM ESD tests, respectively.

E. Failure Analysis

Fig. 16 shows the chip photograph of ESD zapped LNA with the ESD protection circuit B after de-layer procedure.

TABLE V
MEASURED NOISE FIGURES AT 24/60 GHz OF LNA AFTER ESD TESTS

HBM ESD Tests	LNA	LNA with ESD A	LNA with ESD B
100 V	Failed	5.5 / 7.4 dB	5.9 / 8.4 dB
500 V	Failed	5.5 / 7.3 dB	6.0 / 8.5 dB
750 V	Failed	8.5 / 11.3 dB	6.0 / 8.3 dB
2.5 kV	Failed	Failed	5.9 / 8.5 dB
2.75 kV	Failed	Failed	8.3 / 12.5 dB

TABLE VI
MEASURED POWER CONSUMPTION OF LNA AFTER ESD TESTS

HBM ESD Tests	LNA	LNA with ESD A	LNA with ESD B
100 V	Failed	88 mW	88 mW
500 V	Failed	88 mW	88 mW
750 V	Failed	113 mW	88 mW
2.5 kV	Failed	Failed	88 mW
2.75 kV	Failed	Failed	96 mW

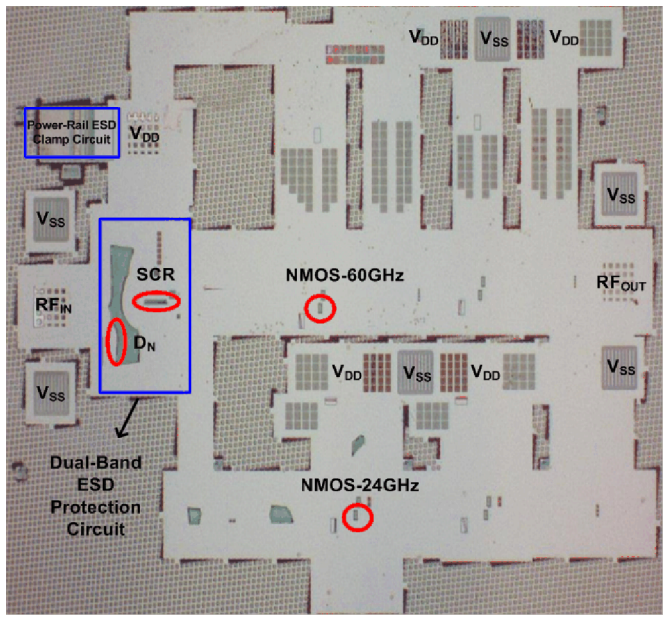
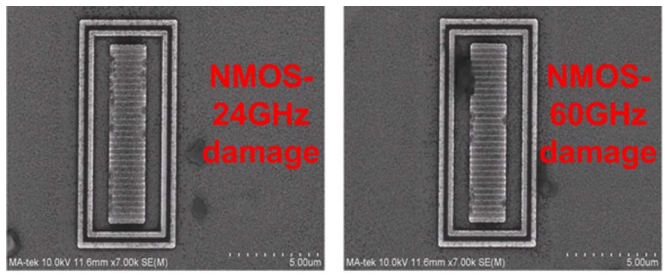
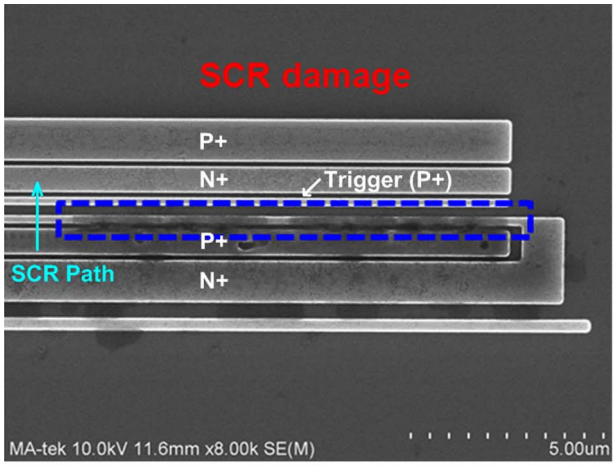


Fig. 16. Chip photograph of ESD zapped LNA with the ESD protection circuit B after de-layer procedure.

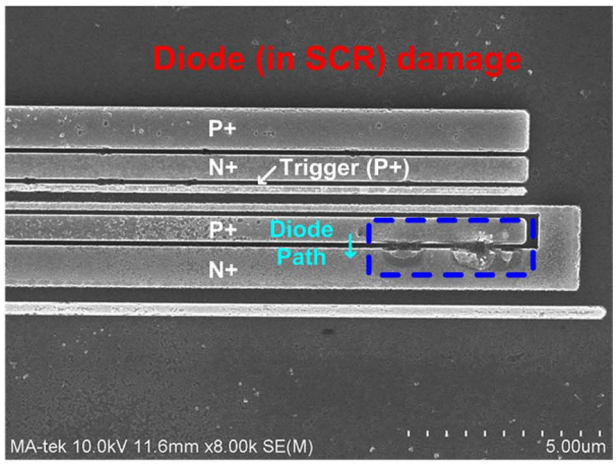


(a) (b)

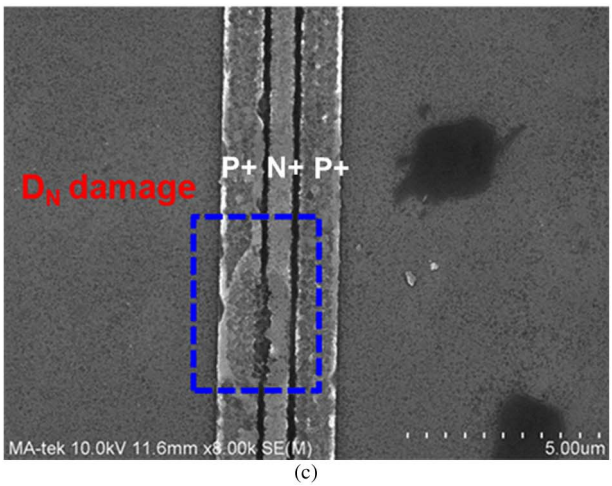
Fig. 17. SEM picture of NMOS in (a) 24 GHz LNA and (b) 60 GHz LNA, of the LNA without ESD protection.



(a)



(b)



(c)

Fig. 18. Failure sites of LNA with the proposed dual-band ESD B under (a) PS-mode, (b) PD mode, and (c) NS mode ESD tests.

Since the failure location of each zapping mode is concentrated, the red circles are denoted as D_{N}, SCR, NMOS of 24 GHz LNA (NMOS-24 GHz), and NMOS of 60 GHz LNA (NMOS-60 GHz) for scanning-electron-microscope (SEM) observing. Fig. 17 shows the SEM picture of the LNA without ESD protection. It has confirmed that the ESD damage, indicated by blue dashed square, is located on the poly-gate with dark and un-continuous marks after the PS-mode HBM ESD stress. Besides, the damage locations of Fig. 17(b) are more than those of Fig. 17(a), because the ESD current will direct damage the gate oxide which is closer to the RF_{IN} pad.

For the ESD protected LNA, Fig. 18 shows the failure sites of LNA with the proposed dual-band ESD protection circuit B under PS-mode, PD mode, and NS mode ESD tests. In PS mode, the input pad is zapped by a positive ESD stress and the V_{SS} pad is grounded. The dominant ESD current will flow through SCR path, as shown in Fig. 3, to discharge and the damage site is observed at SCR path and shown in Fig. 18(a) with blue dashed square. In PD mode, the input pad is zapped by a positive ESD stress and the V_{DD} pad is grounded. The ESD current will be gathered in the diode path, as shown in Fig. 3, and the damage site is inspected at diode and shown in Fig. 18(b) with blue dashed square. In NS and ND modes, the input pad is zapped by a negative ESD stress, and the V_{SS} and V_{DD} pad are grounded, respectively. Since the ESD current will be discharged by the forward-biased D_{N} in NS and ND mode, the damage site is found at D_{N} and shown in Fig. 18(c) with blue dashed square.

V. Conclusion

The novel ESD protection cell for 24-/60-GHz dual-band applications has been designed, fabricated, and characterized in a 65-nm CMOS process. The test circuits A and B have about 1.29 dB (1.22 dB) and 1.35 dB (1.57 dB) power loss at 24 GHz (60 GHz), respectively. Besides, they can sustain 0.5-kV and 2.25-kV HBM ESD tests, respectively. The VF-TLP-measured It_2 of these test circuits are also provided, which are 1.3 A and 2.88 A, respectively. The proposed dual-band ESD protection design can be used to achieve good RF performance and ESD robustness simultaneously. The test circuits with the proposed dual-band ESD have been successfully applied to the 24-/60-GHz LNA to verify the circuit performance and confirm the ESD protection ability. Besides, the ESD protection cell can be further designed for other MMW circuits, such as 24/77 GHz applications.

Acknowledgment

The authors would like to thank Taiwan Semiconductor Manufacturing Company for the review meetings during the circuit design and measurement, where the participants included M.-H. Song, C.-P. Jou, T.-H. Lu, J.-C. Tseng, M.-H. Tsai, T.-L. Hsu, P.-F. Hung, T.-H. Chang, and Y.-L. Wei.

References

[1] J. Hasch, E. Topak, R. Schnabel, T. Zwick, R. Weigel, and C. Waldschmidt, "Millimeter-wave technology for automotive radar sensors in the 77 GHz frequency band," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 3, pp. 845–860, Mar. 2012.

[2] H. Zirath, T. Masuda, R. Kozhuharov, and M. Ferndahl, "Development of 60-GHz front-end circuits for a high-data-rate communication system," *IEEE J. Solid-State Circuits*, vol. 39, no. 10, pp. 1640–1649, Oct. 2004.

[3] V. Giammello, E. Ragonese, and G. Palmisano, "Transmitter chipset for 24/77-GHz automotive radar sensors," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, 2010, pp. 75–78.

[4] V. Jain, F. Tzeng, L. Zhou, and P. Heydari, "A single-chip dual-band 22–29-GHz/77–81-GHz BiCMOS transceiver for automotive radars," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3469–3485, Dec. 2009.

[5] S. Voldman, *ESD: RF Technology and Circuits*. Hoboken, NJ: Wiley, 2006.
[6] C.-Y. Lin, L.-W. Chu, and M.-D. Ker, "ESD protection design for 60-GHz LNA with inductor-triggered SCR in 65-nm CMOS process," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 3, pp. 714–723, Mar. 2012.
[7] M. Tsai, S. Hsu, F. Hsueh, and C. Jou, "ESD-protected K-band low-noise amplifiers using RF junction varactors in 65-nm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 12, pp. 3455–3462, Dec. 2011.
[8] J. Gonzalez, H. Solar, I. Adin, D. Mateo, and R. Berenguer, "A 16-kV HBM RF ESD protection codesign for a 1-mW CMOS direct conversion receiver operating in the 2.4-GHz ISM band," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 9, pp. 2318–2330, Sep. 2011.
[9] M.-D. Ker, C.-Y. Lin, and Y.-W. Hsiao, "Overview on ESD protection designs of low-parasitic capacitance for RF ICs in CMOS technologies," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 2, pp. 207–218, Jun. 2011.
[10] A. Wang, H. Feng, R. Zhan, H. Xie, G. Chen, Q. Wu, X. Guan, Z. Wang, and C. Zhang, "A review on RF ESD protection design," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1304–1311, Jul. 2005.
[11] K. Gong, H. Feng, R. Zhan, and A. Wang, "A study of parasitic effects of ESD protection on RF ICs," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 393–402, Jan. 2002.
[12] C. Richier, P. Salome, G. Mabboux, I. Zaza, A. Juge, and P. Mortini, "Investigation on different ESD protection strategies devoted to 3.3 V RF applications (2 GHz) in a 0.18 μm CMOS process," *J. Electrostatics*, vol. 54, no. 1, pp. 55–71, Jan. 2002.
[13] S. Bronckers, G. Plas, G. Vandersteen, and Y. Rolain, "Substrate noise coupling mechanisms in lightly doped CMOS transistors," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 6, pp. 1727–1733, Jun. 2010.
[14] M.-D. Ker and K.-C. Hsu, "Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 2, pp. 235–249, Jun. 2005.
[15] M. Mergens, C. Russ, K. Verhaege, J. Armer, P. Jozwiak, R. Mohn, B. Keppens, and C. Trinh, "Speed optimized diode-triggered SCR (DTSCR) for RF ESD protection of ultra-sensitive IC nodes in advanced technologies," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 532–542, Sep. 2005.
[16] M.-D. Ker and C.-Y. Lin, "Low-capacitance SCR with waffle layout structure for on-chip ESD protection in RF ICs," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 5, pp. 1286–1294, May 2008.
[17] L.-W. Chu, C.-Y. Lin, S.-Y. Tsai, M.-D. Ker, M.-H. Song, C.-P. Jou, T.-H. Lu, J.-C. Tseng, M.-H. Tsai, T.-L. Hsu, P.-F. Hung, T.-H. Chang, and Y.-L. Wei, "Design of ESD protection cell for dual-band RF applications in a 65-nm CMOS process," in *Proc. EOS/ESD Symp.*, 2012.
[18] S. Voldman, R. Ashton, J. Barth, D. Bennett, J. Bernier, M. Chaine, J. Daughton, E. Grund, M. Farris, H. Gieser, L. Henry, M. Hopkins, H. Hyatt, M. Natarajan, P. Juliano, T. Maloney, B. McCaffrey, L. Ting, and E. Worley, "Standardization of the transmission line pulse (TLP) methodology for electrostatic discharge (ESD)," in *Proc. EOS/ESD Symp.*, 2003, pp. 1–10.
[19] C. Chu, A. Gallerano, J. Watt, T. Hoang, T. Tran, D. Chan, W. Wong, J. Barth, and M. Johnson, "Using VFTLP data to design for CDM robustness," in *Proc. EOS/ESD Symp.*, 2009, pp. 1–6.
[20] S. Wu and B. Razavi, "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2178–2185, Dec. 1998.

Li-Wei Chu (S'10) received the B.S. degree from the Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan, in 2006 and the M.S. degree from the Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2008, where he has been working toward the Ph.D. degree in the Department of Photonics and the Display Institute since 2008.

His current research interests include peripheral circuits integrated on panels for flat panel display applications and the design of 60-GHz electrostatic discharge protection circuits in CMOS process.

Chun-Yu Lin (S'06–M'09) received the B.S. degree from the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2006 and the Ph.D. degree from the Institute of Electronics, National Chiao Tung University, in 2009.

Since 2009, he has been a Postdoctoral Researcher with the Institute of Electronics, National Chiao Tung University. His current research interests include electrostatic discharge protection designs and biomimetic circuit designs.

Dr. Lin has served as the Secretary-General of Taiwan ESD Association since 2010.

Ming-Dou Ker (F'08) received the Ph.D. degree from the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, in 1993.

He was the Department Manager of the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute, Hsinchu. Since 2004, he has been a Full Professor with the Department of Electronics Engineering, National Chiao Tung University. During 2008–2011, he was the Vice President of I-Shou University, Kaohsiung, Taiwan. Since 2012, he has been the Dean of the College of Photonics, National Chiao Tung University, and he is also the Distinguished Professor with the Department of Electronics Engineering. He served as the Executive Director of the National Science and Technology Program on System-on-Chip in Taiwan (2010–2011) and is currently serving as the Executive Director of the National Science and Technology Program on Nano Technology in Taiwan (2011–2014). In the technical field of reliability and quality design for microelectronic circuits and systems, he has published over 450 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits (ICs), which have been granted with hundreds of U.S. patents and Taiwan patents. He had been invited to teach and/or to consult the reliability and quality design for ICs by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, circuits and systems for information display, and biomimetic circuits and systems for biomedical applications.

Prof. Ker was the Founding President of Taiwan ESD Association. He has served as a Member of the Technical Program Committee and the Session Chair of numerous international conferences for many years. He was selected as the Distinguished Lecturer in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008–2012). He served as an Associate Editor for the IEEE TRANSACTIONS ON VLSI SYSTEMS in 2006–2007. He is currently an Editor of the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY.