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InAs Thin-Channel High-Electron-Mobility Transistors with Very High Current-Gain Cutoff Frequency for Emerging Submillimeter-Wave Applications

Edward-Yi Chang[1*], Chien-I Kuo[1], Heng-Tung Hsu[2], Che-Yang Chiang[2], and Yasuyuki Miyamoto[3]

[1]*Department of Materials Science and Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.*
[2]*Department of Communications Engineering, Yuan Ze University, Chungli 32003, Taiwan, R.O.C.*
[3]*Department of Physical Electrons, Tokyo Institute of Technology, Meguro, Tokyo 152-8552, Japan*
E-mail: edc@mail.nctu.edu.tw

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60 nm InAs high-electron-mobility transistors (HEMTs) with a thin channel, a thin InAlAs barrier layer, and a very high gate stem structure have been fabricated and characterized. The thickness of the channel, as well as that of the InAlAs barrier layer, was reduced to 5 nm. A stem height of 250 nm with a Pt-buried gate was used in the device configuration to reduce the parasitics. A high DC transconductance of 2114 mS/mm and a current-gain cutoff frequency (f_T) of 710 GHz were achieved at V_{DS} = 0.5 V.

State-of-the-art high-electron-mobility-transistor (HEMT) technologies are capable of providing frequency conversion and amplification up to the submillimeter-wave frequency regime (>300 GHz) for ultrawide-band communication, imaging systems, remote atmospheric sensing, and space exploration applications.[1)] Recent literature reported characteristics of InGaAs/InAlAs HEMTs with a considerably high f_T and maximum oscillation frequency (f_{max}) exceeding 600 GHz.[2–8)]

Efforts devoted to increasing the frequency limits of operation included gate-length scaling,[9,10)] increasing the In content of transistor channels, narrowing the source–drain spacing,[6)] reducing the barrier layer or channel thickness to enhance the electron transport properties, reducing the parasitic resistances or capacitances, and improving the short channel effect.[11)] However, further scaling of the relevant device dimensions may require combinations of other device techniques such as optimal channel aspect ratio and high gate stem for future ultrahigh-speed applications.

The combination of 60 nm Pt-buried gate and stem height of 250 nm InAs channel HEMT with a thin channel and InAlAs barrier layer was fabricated successfully. The thicknesses of both the channel and InAlAs barrier layer were reduced to 5 nm. A thin InAlAs barrier layer is typically preferable for reducing the resistance across the Schottky barrier InAlAs/InAs heterostructure and achieving a high transconductance.[12)] The stem height of the gate was 250 nm to minimize the parasitics.[4)] The fabrication process was simplified through the growth of a thin barrier layer and Pt-buried gate during passivation to maintain an optimal channel aspect ratio compared with the two-step recess technique.[13)] The fabricated 60 nm devices demonstrated excellent DC and RF characteristics that benefitted from the reduction of parasitic resistance/capacitance and improvement of the channel aspect ratio and output conductance.

The epitaxial layer structure of the InAs thin-channel device was grown by MBE on a 3-in. InP substrate, as shown in Fig. 1. The structure consisted of a 600-nm-thick $In_{0.52}Al_{0.48}As$ buffer, a thin 2 nm pure InAs layer with 1 nm $In_{0.7}Ga_{0.3}As$ upper sub-channel and 2 nm $In_{0.7}Ga_{0.3}As$ lower subchannel, a 3-nm-thick InAlAs spacer, a Si δ-doping with $5 \times 10^{12}\,cm^{-2}$, a 2-nm-thick InAlAs barrier, and a 3-nm-thick InP etching stop. For the multilayer cap structure, 15-nm n^+-$In_{0.52}Al_{0.48}As$ ($2 \times 10^{18}\,cm^{-2}$), 15-nm n^+-$In_{0.53}Ga_{0.47}As$ ($2 \times 10^{19}\,cm^{-2}$), and 4-nm n^+-$In_{0.65}Ga_{0.35}As$ ($2 \times 10^{19}\,cm^{-2}$) layers were used from bottom to top to reduce the potential barrier across the undoped Schottky barrier, parasitic source/drain resistances, and contact resistance and to assist the electron tunneling under ohmic contact in such ultrahigh-speed HEMTs. After removing the cap layer, the measured room-temperature two-dimensional electron gas (2DEG) density and electron mobility were $3.02 \times 10^{12}/cm^2$ and $11{,}100\,cm^2\,V^{-1}\,s^{-1}$, respectively.

For the device fabrication, mesa isolation was conducted using a wet chemical phosphoric-based solution. A mesa sidewall was also obtained by using the mixture solution of succinic acid, H_2O_2 and NH_4OH. After surface pretreatment with the diluted HCl solution for 60 s, a 1.83 μm ohmic contact spacing between source and drain electrodes was formed by using nonalloyed Au/Ge/Ni/Au (20/40/14/220 nm). The low ohmic contact resistance of 0.018 Ω mm (with cap) and the channel sheet resistance of 119 Ω/□ (without cap) were attained by TLM. Subsequently, the recess engineering was performed carefully by using a citric acid/hydrogen peroxide mixture to etch the multilayer cap and controlling the side-recess length precisely.[14)] Finally, a 60 nm T-shaped gate was formed with a Pt (4 nm)/Ti (20 nm)/Pt (20 nm)/Au (250 nm) metal stack. After gate metal deposition, 100-nm-thick SiN_x was deposited as a passivation layer using PECVD at 250 °C for 1 h, which also caused the Pt front contact to react with the InP stop layer and $In_{0.52}Al_{0.48}As$ barrier layer, in other words, forming a Pt-buried gate. The inset image shows the 60 nm T-shaped gate with a stem height of 250 nm (Fig. 1). In addition, the Pt fully diffused into the Schottky barrier and improved the gate stability during passivation. The gate-to-channel distance was estimated at approximately 4 nm and the lateral recess length was approximately 70 nm.

Figure 2(a) shows the measured DC current–voltage characteristics of 60 nm gate InAs thin-channel HEMTs with $2 \times 20\,\mu m^2$ gate width. A favorable saturation with excellent pinch-off behaviors is observed in the figure. The on resistance R_{ON} was calculated at approximately 0.49 Ω mm at a V_{GS} of 0.3 V for the $L_g = 60$ nm D-mode HEMTs. Smaller output conductance values were obtained compared with the device structure in a previous study,[15)] in which a thicker channel and a thicker InAlAs barrier layer were used. The dependence of the output conductance (g_o) on the aspect ratio α (defined as the gate length divided by the total thickness of the channel and barrier layer) is plotted in

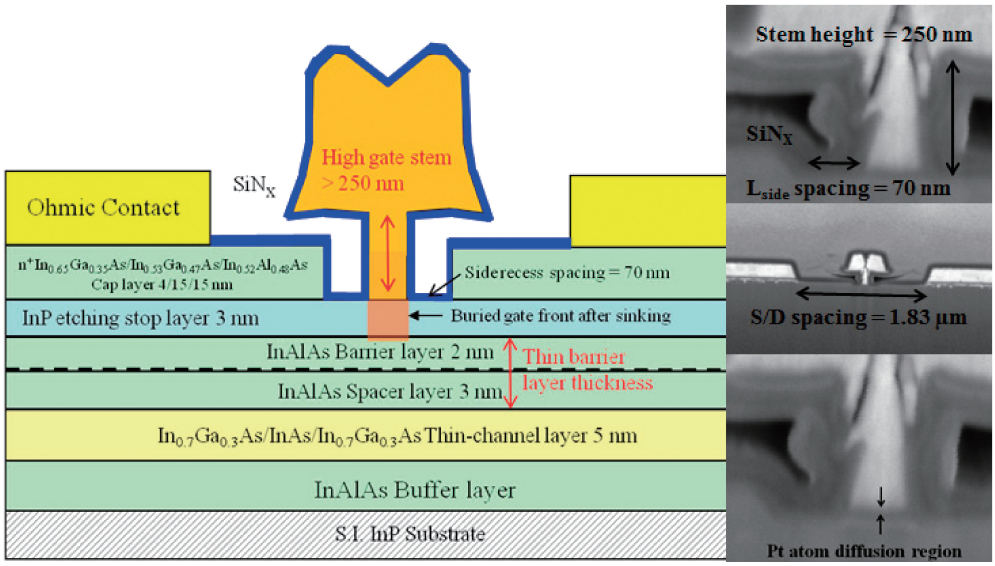
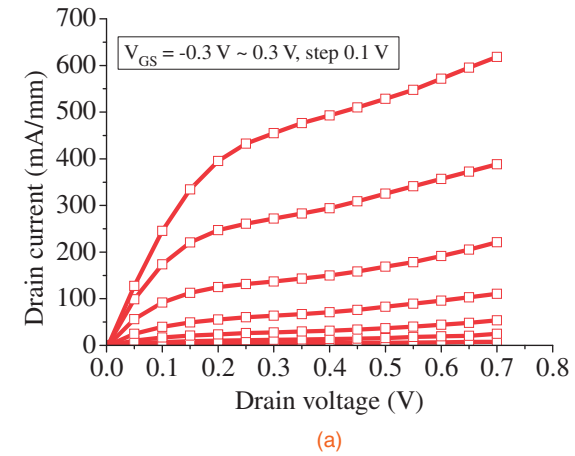


Fig. 1. Schematic view of thin-channel InAs HEMT structure. The inset SEM images are the high-stem T-gate.



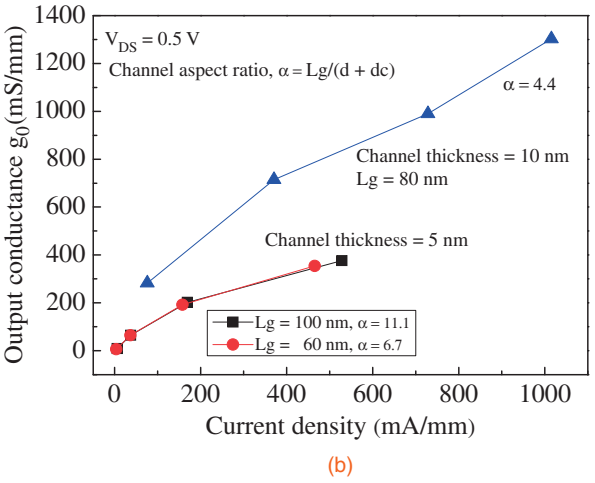


Fig. 2. (a) Drain–source current versus drain–source voltage curve for 60 nm device; (b) output conductance as a function of drain current for various channel-thicknesses.

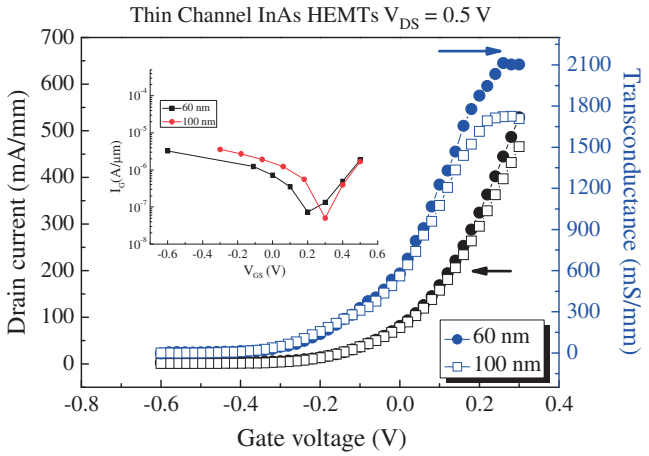


Fig. 3. Transconductance versus gate–source voltage with 60 and 100 nm gate lengths. The inset figure is the Schottky gate leakage current for these fabricated devices.

Fig. 2(b) for various gate lengths of 60, 80, and 100 nm. A higher α yields a lower g_o value, which implies that scaling of only the gate length is not sufficient for the reduction of the output conductance. The measured DC transconductance g_m and drain current versus V_{GS} with various L_g values are shown in Fig. 3. An increase of peak g_m value from 1726 to 2114 mS/mm was observed as the L_g was scaled down from 100 to 60 nm. The short gate-to-channel distance and the low source resistance (0.15 Ω mm) are the main reasons for such high g_m due to the improvement of carrier transport properties. Gate leakage current for thin-barrier devices with various gate lengths is shown in the inset of Fig. 3. For such device, the gate leakage current was slightly higher than those of our previous devices, which indicates a trade-off between the gate leakage current, and high output conductance for such thin-barrier HEMTs.

The RF performance was characterized from 2 to 110 GHz by using an HP 8510XF network analyzer with E7352 test heads calibrated by using a standard load-reflection-reflection-match method. The procedures of small-signal equivalent circuit modeling with the removal of the parasitic capacitances from the probing pads followed those described in Refs. 16–18. The extracted parasitic capacitance at the gate-source end was 11.3 fF and that at the drain–source end

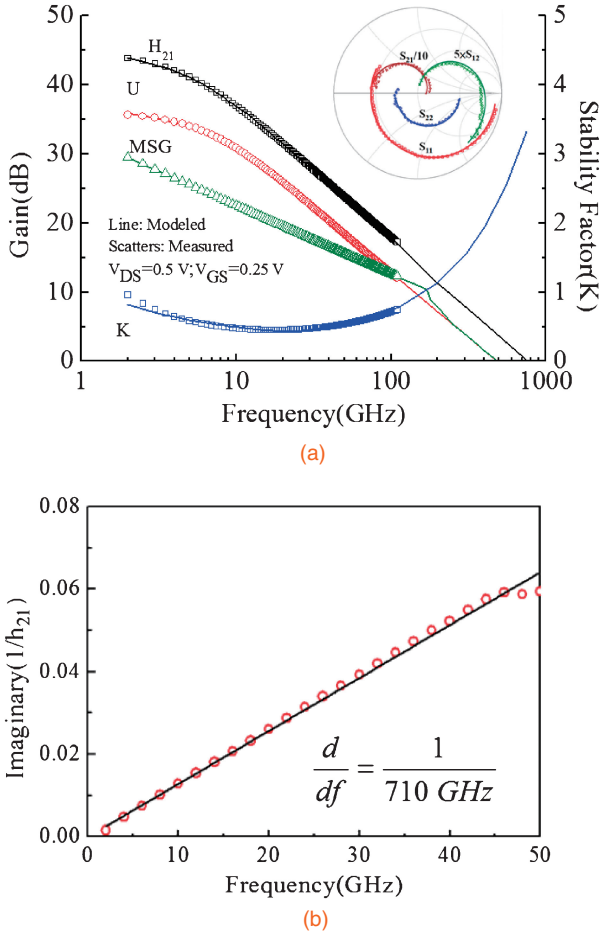


Fig. 4. (a) Frequency dependence of the current gain (H_{21}), Mason's unilateral gain (U), maximum stable gain (MSG), and stability factor (K) at $V_{DS} = 0.5$ V and $V_{GS} = 0.25$ V. The predictions of the equivalent circuit model are also included. (b) Slope of the imaginary component of the reciprocal of the current gain versus frequency, taken from the low-frequency portion of the measurement range.

was 9.5 fF. The de-embedded current gain (H_{21}), maximum stable gain (MSG), Mason's unilateral power gain (U), and stability factor (K) as functions of frequency at $V_{DS} = 0.5$ V and $V_{GS} = 0.25$ V are plotted in Fig. 4(a). The predictions of the equivalent circuit model are also included in the same figure. The f_T and f_{max} were extracted by extrapolating H_{21} and U with a -20 dB/decade slope to be 710 and 478 GHz, respectively. Measurement on multiple devices using different test systems was performed for verification purposes.

To avoid the ambiguity during the extrapolation procedure, we have also applied Gummel's approach [Eq. (5) in Ref. 19] to determine f_T. The slope of the imaginary component of the reciprocal of the current gain versus frequency, taken from the low-frequency portion of the measurement range, was plotted in Fig. 4(b). Equation (3) in Ref. 20 was applied for f_{max}. Both of these equations yielded good consistency. The large difference in f_T and f_{max} for the device was mainly because of the narrow-side recess length (L_{side}).[11] The small L_{side} concentrates the applied drain voltage in this short recess region to increase the lateral electric field under the gate electrode, which boosts the electron velocity and causes the high f_T.[21] A possible tradeoff between current gain and power gain can be made depending on the applications. We believe that the superior performance is attributed to the successful combination of high electron mobility of InAs, low parasitic resistance and capacitance obtained using a high-gate-stem structure, and the optimal channel aspect ratio through the use of the thin channel and barrier layer.

In summary, 60 nm InAs thin-channel HEMTs with a stem height greater than 250 nm and 5-nm-thick barrier layer thickness were characterized for frequencies in the submillimeter-wave range. The device exhibited a considerably high DC g_m of 2,114 mS/mm and a high f_T of 710 GHz when biased at $V_{DS} = 0.5$ V, indicating that the device is an excellent candidate for emerging submillimeter-wave applications. This high f_T is attributable to the use of a thin InAs transistor channel, a thin InAlAs barrier layer, and a Pt-buried gate, which reduces the gate-to-channel distance to 4 nm, thus, improving the channel aspect ratio. In addition, the use of a multicap layer and a high gate stem decreases the source and gate resistances, as well as the overall capacitance of the device.

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