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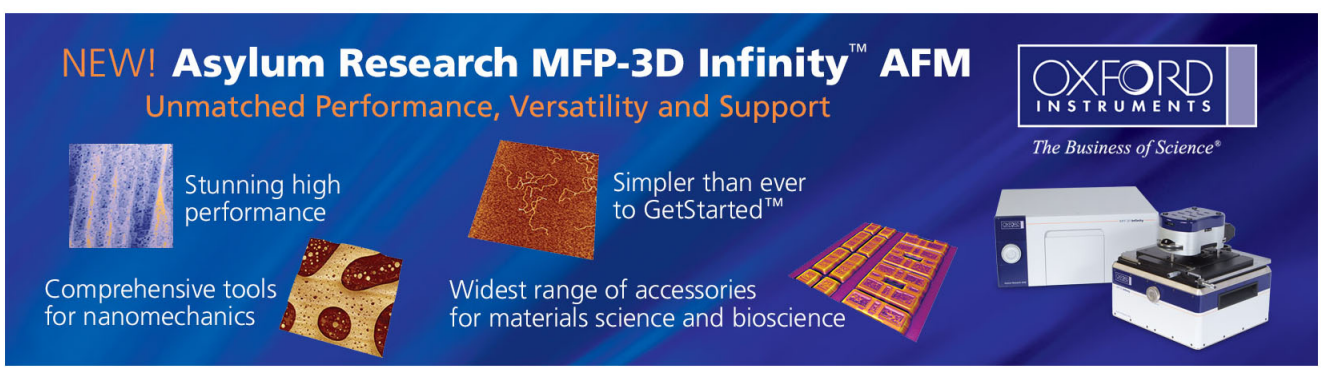

Robust bi-stable memory operation in single-layer graphene ferroelectric memory

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With the motivation of realizing an all graphene-based circuit for low power, we present a reliable nonvolatile graphene memory device, single-layer graphene (SLG) ferroelectric field-effect transistor (FFET). We demonstrate that exfoliated single-layer graphene can be optically visible on a ferroelectric lead-zirconate-titanate (PZT) substrate and observe a large memory window that is nearly equivalent to the hysteresis of the PZT at low operating voltages in a graphene FFET. In comparison to exfoliated graphene, FFETs fabricated with chemical vapor deposited (CVD) graphene exhibit enhanced stability through a bi-stable current state operation with long retention time. In addition, we suggest that the trapping/de-trapping of charge carriers in the interface states is responsible for the anti-hysteresis behavior in graphene FFET on PZT. © *2011 American Institute of Physics*. [doi:10.1063/1.3619816]

Graphene is considered to be an exceptional material with high potential for future electronics, owing to its excellent electronic properties;[1] linear electron energy dispersion, and high room temperature mobility. If feasible, an all graphene-based circuit, including logic, analog, and memory devices, would be of great interest to further extend the performance of current Si-based electronics. Among various device applications, graphene based memory structures are still in their infancy in comparison to its logic and analog applications. To date, graphene memory has been demonstrated through chemical modification,[2] filament-type memristor,[3] nanomechanical switch,[4] and graphene FFETs.[5–7] In graphene FFETs, however, the ambipolar conduction leads to undesirable on/off states for memory applications. Moreover, the absence of an electronic bandgap and controlled doping makes it difficult to resolve such issues. Therefore, a systematic study of graphene FFET is beneficial to realize graphene-based memory structures.

In this Letter, we investigate graphene/PZT FFET structures using exfoliated- and CVD-SLG and their mechanism of operation. We show that exfoliated SLG can be optically identified on a PZT substrate and exhibit a hysteresis of the V-shaped conductance with a large memory window at low operating gate voltages. We compare exfoliated- with CVD-SLG FFETs and show that devices made of CVD-SLG exhibit a robust bi-stable current state with a long retention time.

In order to construct the SLG FFET, we first engineered a ferroelectric substrate to identify SLG. Previously, we have demonstrated that SLG is invisible under the optical microscope unless the underlying layers are optimized for high contrast.[8] Applying Fresnel's model of a tri-layer system SLG/PZT/Pt, an optimal PZT thickness (t_{PZT}) of 180 nm was chosen to ensure a large capacitive coupling for field effect and for high contrast under 600 nm wavelength visible light [Figs. 1(a), 1(b), and inset of 1(c)]. As previously reported, CVD graphene was grown on Cu foils[9] then transferred to the PZT substrates, which were prepared by a sol-gel process.[10] Finally, Raman spectroscopy was used to characterize both exfoliated and CVD graphene samples, which exhibit single Lorentzian peaks at the G and 2D bands.[8] An absence of the D band and a high 2D/G ratio (>2) clearly confirm the existence of high-quality SLG films [Fig. 1(c)].[9]

Two-terminal SLG FFETs were fabricated using standard e-beam- and photo-lithography for exfoliated- and CVD-SLG, respectively, to deposit metal electrodes. The Pt layer underneath the PZT was used as the gate electrode, and leakage currents were less than 1 nA when 7 V ($<10^{-6}$ A/cm^2) was applied between the channel and gate electrodes. The channel lengths ranged from 0.8–10 μm with a length to width ratio of 0.5–2. Electrical measurements were performed at room temperature in a vacuum environment with a pressure of 1.1×10^{-6} Torr. In order to characterize device behavior, a source-drain bias (V_{ds}) was kept constant while the gate voltage (V_g) was swept in a closed loop from 0 V $\rightarrow$ $+V_{g(sweep)} \rightarrow -V_{g(sweep)} \rightarrow 0$ V, where $V_{g(sweep)}$ is the maximum sweep voltage of the gate. All gate dependent drain current (I_d-V_g) measurements were repeatable with current values following the same paths.

For exfoliated-SLG FFETs, a hysteretic behavior of I_d is clearly observed with a double minimum symmetry when V_g is swept, which results from the nonlinear-hysteresis of the

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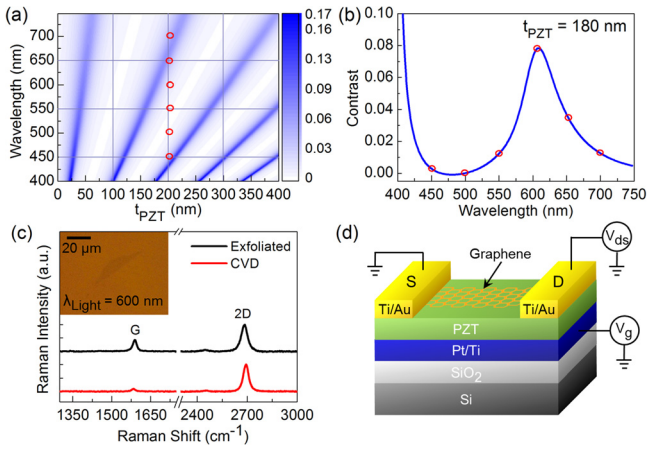

FIG. 1. (Color online) (a) 3D color plot of the contrast as a function of wavelength and t_{PZT}. (b) Contrast as a function of the wavelength at $t_{PZT} = 180$ nm. The red circles indicate equivalent points in top row. (c) Raman spectrum of exfoliated- and CVD-SLG on PZT. (Inset shows an optical image of a large exfoliated-SLG on 180 nm-thick PZT at 600 nm visible wavelength. (d) Schematic device structure of SLG FFET.

ferroelectric PZT [Fig. 2(a)]. The two minimum conductance points occur at both positive and negative $V_{g(sweep)}$, which we define as V^+_{gmin} and V^-_{gmin}, respectively. At V^+_{gmin} and V^-_{gmin}, the Fermi level aligns with the Dirac point and is satisfied when the electrostatic potential from the ferroelectric dipoles compensate the pre-existing potential caused by the residual dopants. Furthermore, the minimum conductivity has a value of $4e^2/h$, which is attributed to the high dielectric constant ($\kappa \approx 400$–500) of PZT and coincides with previous values in high-κ environments.[11]

Several observations of the transport behavior should be noted to better understand practical device operation. We observe the ratio of hysteretic switching between maximum and minimum conductance of 250%. The maximum conductance occurs where the current saturates in the high carrier density regime ($>10^{12}$/cm^2) and is determined by short-range scatterers.[11] The asymmetry of the saturation between hole and electron conduction, as seen at maximal negative or positive gate voltages, respectively, is attributed to doping by the contact metals near the graphene/metal interface.[12]

In the case of CVD-SLG FFETs, the main difference in comparison to the exfoliated-SLG is the initial doping level and the presence of carrier dependent scattering sources,[13] where heavy chemical doping is introduced from the etchant solution during the process of removing the copper catalyst.[14] The chemical doping shifts the Fermi level below the Dirac point and suppress the modulation of electron charge carriers. These effects give rise to the observed hysteresis behavior, which is shown in Fig. 2(b). A clear bi-stable memory operation appears in CVD-SLG FFET, which is analogous to what is observed for dual-gated graphene polymer-FFETs.[7]

A desirable condition for a functional memory device is a bi-stable current state. Although one can operate the exfoliated graphene FFETs by using an asymmetrical loop sweep on V_g to achieve memory functionality,[5] the ambipolar conduction behavior of graphene creates a minimum conductance point within a small voltage range (0.1–0.3 V) and produces an unstable current state, $d^2I_d/dV_g^2 < 0$ near $V_g \approx$ Dirac point. The doped CVD-SLG, however, offers an advantage by suppressing the electron modulation and creating a bi-stable state that can operate at a wide bias range with an enhanced stability. Identical bi-stable hysteresis loops were observed for 98% of the fabricated devices, which corroborates the robustness of CVD-SLG FFET memory structures.

In order to relate the electrical hysteresis characteristics of the graphene FFET to the ferroelectric properties of PZT, subsequent I_d-V_g measurements were taken at various $V_{g(sweep)}$ [Figs. 2(a) and 2(b)], and the corresponding polarization measurements (P-V_g) were performed on a capacitor structure of Pt/PZT/Ti/Au on the same PZT substrate under the same $V_{g(sweep)}$ [inset of Fig. 2(c)]. As $V_{g(sweep)}$ was increased, both the coercive field (E_C) and remnant polarization (P_R) nearly saturated at $V_{g(sweep)} = 7$ V with $E_C \sim 130$ kV/cm and $P_R \sim 25$ μC/cm^2, which are inherent material properties dependent on the fabrication method of thin film PZT.

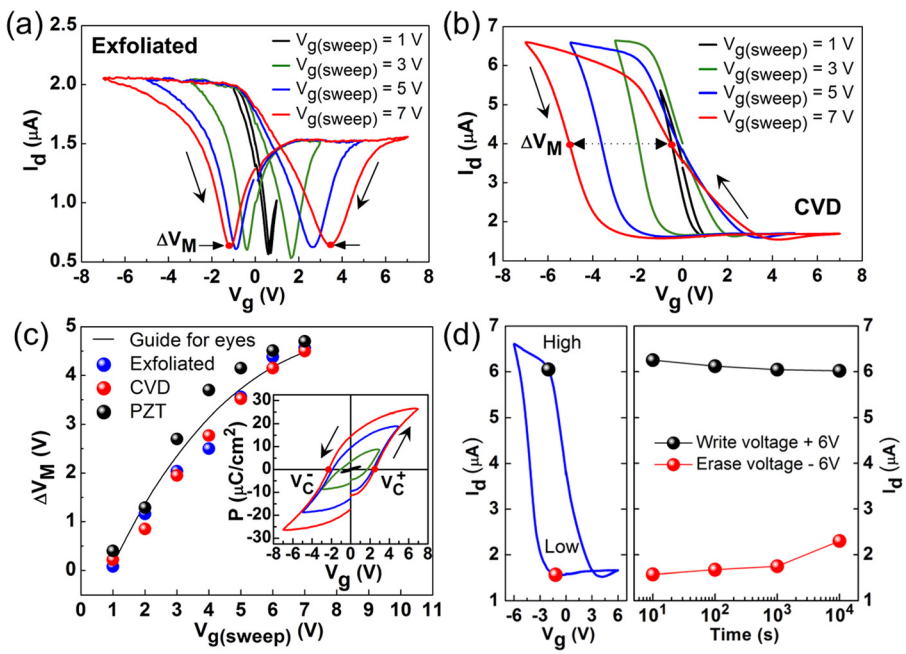

FIG. 2. (Color online) (a) Hysteresis characteristics of the exfoliated-SLG FFET with varied $V_{g(sweep)}$ at $V_{ds} = 0.5$ mV. (b) Hysteresis characteristics of CVD-SLG FFET with varied $V_{g(sweep)}$ at $V_{ds} = 5$ mV. (c) ΔV_M as a function of $V_{g(sweep)}$. The blue and red circles correspond to the ΔV_M extracted from transfer characteristics of exfoliated- and CVD-SLG FFETs, respectively. The black circles correspond to the ΔV_M extracted from the P-V_g of the PZT capacitor. (Inset shows the P-V_g of a 180 nm-thick PZT capacitor.) The colors indicate sweeping voltages (1, 3, 5, and 7 V) in each figure. (d) Retention time characteristics of CVD-SLG FFET after applying writing voltages of ±6 V. Readout was performed at $V_g = -1$ V and $V_{ds} = 5$ mV.

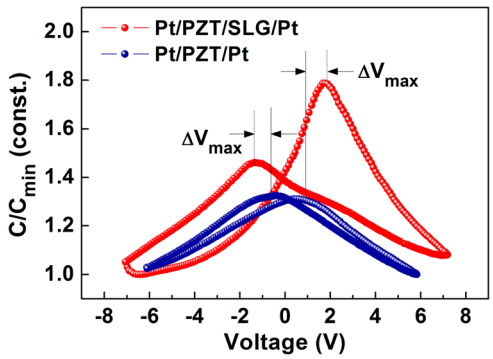

FIG. 3. (Color online) C-V characteristics of Pt/PZT/Pt and Pt/PZT/SLG/Pt capacitors.

In a FFET, the memory window (ΔV_M) is theoretically equal to $\Delta V_M = V_C^+ - V_C^-$, where V_C is the coercive voltage. Since graphene is a zero-bandgap material, it is difficult to define a threshold voltage. Thus, it is rational to define the degree of hysteresis for the exfoliated-SLG FFET as the voltage difference of the minimum conductance points. In the case of CVD-SLG FFET, we define the ΔV_M as the difference in V_g that occur at the current value corresponding to the midpoint of the maximum and minimum possible current values of the device. These are clearly labeled in Figs. 2(a) and 2(b). With these definitions, we compare the memory window obtained at subsequent sweeping voltages between the SLG-FFETs and PZT capacitor [Fig. 2(c)]. As $V_{g(sweep)}$ is incrementally increased, both the memory windows increase and nearly saturate near 7 V, which shows that the electrical hysteresis of the graphene FFET follows the ferroelectric property. In traditional semiconductor FFETs, the memory window is far less than $2 \times V_C$;[15] however, our SLG FFETs show a significant advantage since the window width is nearly identical to the hysteresis of the PZT.

Another important factor to consider when characterizing a nonvolatile memory device is its retention characteristics. The retention time of a memory device is a measure of the devices ability to produce high fidelity output after writing stored data. Figure 2(d) displays the retention characteristics

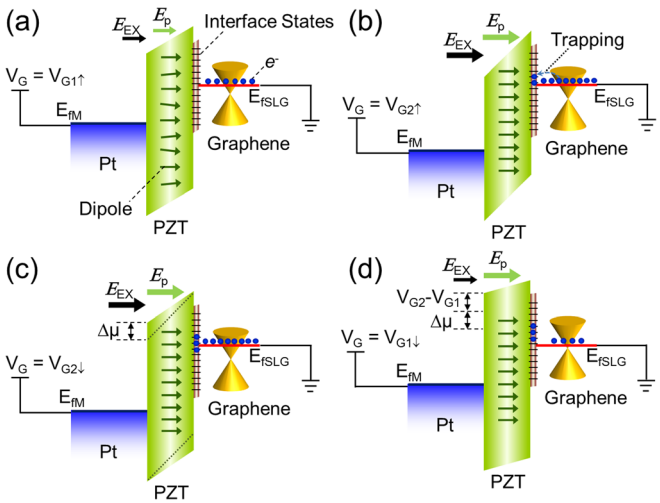

FIG. 4. (Color online) Band diagram of SLG-FFET at various bias conditions depending on sweep direction: (a) $V_g = V_{G1\uparrow}$, (b) $V_g = V_{G2\uparrow}$, (c) $V_g = V_{G2\downarrow}$, and (d) $V_g = V_{G1\downarrow}$.

of the bi-stable state device, which has a large ΔV_M of 4.2 V and a high/low current ratio of 420% at $V_{g(sweep)} = 6$ V. The data points represent I_d after applying a writing voltage of ± 6 V. The read operation was done at a V_g of -1 V ($<V_C$), since the high/low current states were accessible at this voltage without affecting the pre-programmed polarization state. Both states show good retention times up to 1000 s.

Here, we note that the observed current hysteresis has an opposite direction from the polarization direction of the PZT as illustrated by arrows on Fig. 2. Two possible mechanisms can lead to such observation; one is due to charge trapping in the interface states[16] and the other is polarization screening from water molecules located between graphene and PZT.[6] To investigate the effect of graphene on the interface of PZT and gate-electrode, we compare the capacitance-voltage characteristics (C-V) [Fig. 3] of a ferroelectric capacitor with (Pt/SLG/PZT/Pt) and without graphene (Pt/PZT/Pt). As indicated in Fig. 3, the position and value of the normalized capacitance maxima drastically changes (ΔV_{max}), which can be either caused by the work function difference of the two metal plates and/or charges at the interface states.[17]

Based on above results, we explain one possible mechanism for the anti-hysteresis effect. As we positively increase the V_g beyond the Dirac point (e.g., $V_g = V_{G1}$), the external electric filed (E_{EX}) and the dipole moments (E_p) of PZT induce electrons in graphene [Fig. 4(a)]. When E_{EX} and E_p increase (e.g., $V_g = V_{G2} > V_{G1}$), the electrons become trapped by the interface states [Fig. 4(b)]. Once V_g reaches $V_{g(sweep)}$, the trapped electrons remain at the interface states by E_p and reduce the electrochemical potential ($\Delta\mu \propto \Delta V_{max}$) of PZT [Fig. 4(c)].[18] Therefore, upon reversing the V_g direction, the number of electrons induced in graphene would be less than that at the same V_g (e.g., $V_g = V_{G1}$) [Fig. 4(d)]. As a result, the I_d-V_g shows anti-hysteretic behavior contrary to the P-V_g hysteresis.

In conclusion, we performed a systematic study of SLG FFETs, which can provide alternative avenues for exploring unprecedented graphene based memory structures.

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