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Citation: Applied Physics Letters **102**, 073507 (2013); doi: 10.1063/1.4791676
View online: http://dx.doi.org/10.1063/1.4791676
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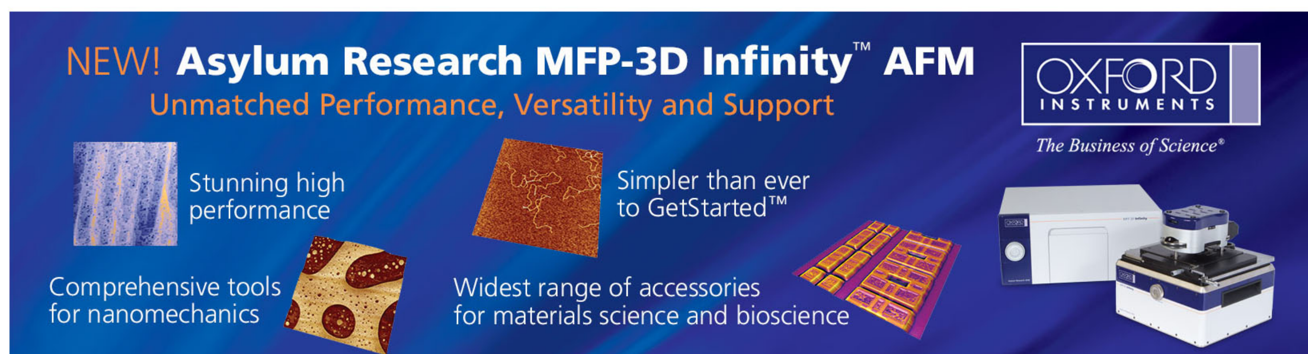

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APPLIED PHYSICS LETTERS **102**, 073507 (2013)

Hole injection-reduced hot carrier degradation in n-channel metal-oxide-semiconductor field-effect-transistors with high-k gate dielectric

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(Received 16 November 2012; accepted 29 January 2013; published online 22 February 2013)

This work finds a significant difference in degradation under hot carrier stress (HCS) due to additional hole injection in n-channel metal-oxide-semiconductor field-effect-transistors with high-k gate dielectric. A comparison performed on degradation of input/output (I/O) and standard performance (SP) devices showed that performance degradation of the I/O device is worse than the SP device under HCS. For the SP device, both channel-electrons and hot holes can inject into gate dielectric, in which hole acts to diminish the stress field. However, I/O device shows only electron injection. The proposed model is confirmed by gate induced drain leakage current and simulation tool. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4791676]

The continuous scaling-down of metal oxide semiconductor field effect transistors (MOSFETs) is driving conventional SiO_2-based dielectric to only a few atomic layers thick, leading to excessive gate leakage current and reliability issues.[1] To solve the leakage current problem, a high-k material is utilized as gate insulator to reduce both tunneling gate leakage and power consumption in complementary MOS circuits.[2–4] Furthermore, the high-k/metal gate can be integrated with silicon on insulator techniques.[5–8] Additionally, charge trapping in high-k gate stacks remains a key reliability issue, since it causes the threshold voltage (V_{th}) shift and drive current degradation[9–12] due to the filling of pre-existing traps in the high-k dielectric layer.[13–15] In addition, charge trapping effect is found to have great impact on hot carrier stress (HCS)-induced device instability since carriers tend to be injected into the high-k layer.[16,17] HC injection is a critical issue for submicron transistors since devices encounter higher lateral electric field and this issue is even more severe in high-k/metal gate MOSFETs. However, most studies mainly focus on investigating the influences of channel lengths, stress voltages, high k materials, and temperature effect to analyze n-MOSFET characteristics under HCS.[18–20] There are only few studies to investigate the effect of interfacial layer (IL) thickness on HCS-induced degradation in n-MOSFETs, even less for high-k/metal gate devices. Since the mechanism of that thicker IL has a more significant degradation than thinner IL device under HCS not been discussed extensively, and, therefore, we are interested to investigate this unusual behavior in high k metal gate n-MOSFETs. In this work, we utilize the three characteristics, namely, transconductance (G_m), drain current (I_D), and subthreshold swing (SS) to illustrate the degree of degradation. The I/O device shows more significant degradation than the standard performance (SP) device under identical impact ionization conditions. This unusual phenomenon can be explained by the gate induced drain leakage (GIDL) current, which demonstrates that channel hot electron or hot hole trapping near the drain side acts to enlarge or reduce the channel carrier kinetic energy under HCS, respectively. In addition, the simulation tool Integrated Systems Engineering-Technology Computer Aided Design (ISE-TCAD) is used to support the model that we propose in this work.

TiN/HfO_2 n-MOSFETs with an IL thickness of 10 and 30 Å were studied in this paper as an element of high-performance 28-nm CMOS technology. Both devices were fabricated using a conventional self-aligned transistor which progressed to the gate-first process. The process parameter (S/D implants, halo/LDD implants, activate temperature, thin films thickness) of I/O and SP devices was only an IL thickness that has significant difference, others almost use the same process parameter. For gate-first process devices, high quality thermal oxides with different thicknesses of 10 and 30 Å were grown on a (100) Si substrate as an IL oxide layer. After standard cleaning procedures, 30 Å of HfO_2 film was sequentially deposited by atomic layer deposition. Next, 10 nm of TiN film was deposited by radio frequency physical vapor deposition, followed by poly-Si deposition as a low resistance gate electrode. The activation of source/drain and poly-Si gate was performed at 1025 °C. The channel and source/drain doping concentrations of I/O and SP devices were about $1 \times 10^{18}\,cm^{-3}$ and $1 \times 10^{21}\,cm^{-3}$, respectively. In this study, the dimensions of the devices were width (W)/length (L) = 10/1 μm. The devices with IL thickness of 10 and 30 Å were subjected to the maximum substrate current ($I_{B,max}$) during HCS conditions while at 3 V and 3.1 V drain voltage (V_D), respectively. The stress was briefly interrupted to measure the drain current-gate voltage (I_D-V_G) to extract V_{th}, G_m, I_D, and SS. In the gate-to-drain capacitance (C_{GD}) measurement, a high capacitance measurement was applied to the gate electrode, and drain electrodes were connected to a low capacitance measurement with frequency = 2 MHz,

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and GIDL current was measured at $V_G = -0.5$ V and $V_D = 2.4$ V. All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer.

Figures 1(a) and 1(b) show the I_D-V_G and corresponding G_m-V_G at the linear region measurement after HCS for high k/metal gate n-MOSFETs for the I/O and SP devices. Stress condition was selected at the identical $I_{B,max}$ for both devices. It can be seen that I_D, G_m, and SS degrade under HCS in both devices. This is attributed to channel electrons that are accelerated by lateral electric field, producing impact ionization which generates interface states (N_{it}) near the drain side.[21] Accordingly, the insets of Figs. 1(a) and 1(b) show the C_{GD} measurement before and after HCS. There is a shift which indicates that damages are located at the drain side after HCS. Also, the direction of shift is rightward to demonstrate a crucial behavior in all the devices that of channel electron injection in the gate dielectric near the drain side.[22] However, both performance degradation and C_{GD} shift in the I/O device are more significant than those in the SP device.

Additionally, the degradation of I_D, G_m, and SS versus stress time was extracted for SP and I/O devices, as shown in Fig. 2. Obviously, the characteristic of the I/O device displays more significant degradation under HCS. This phenomenon is unlike conventional I/O devices. Generally, I/O

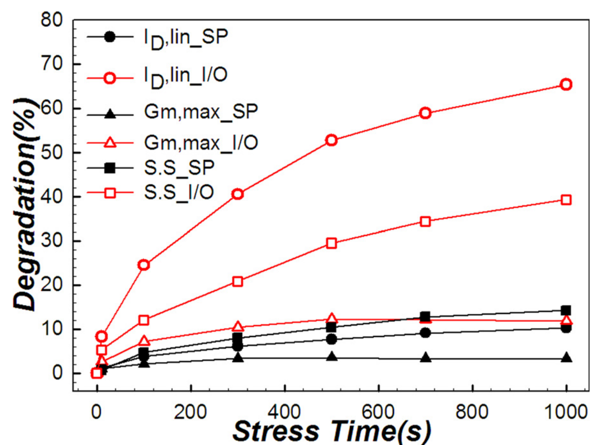

FIG. 2. The degradation of I_D, G_m, and SS versus stress time extracted for SP and I/O devices under HCS.

devices have thicker gate oxides that correspond to better reliability during operation. Due to this, these devices can retain good signal propagation. However, the experiment result shows this undesired degradation behavior for I/O devices under HCS. To clarify this degradation behavior, we use GIDL current to confirm carrier injection.

Figures 3(a) and 3(b) show I_D-V_G and corresponding I_B-V_G at $V_D = 2.4$ V for I/O and SP devices. It can be seen that

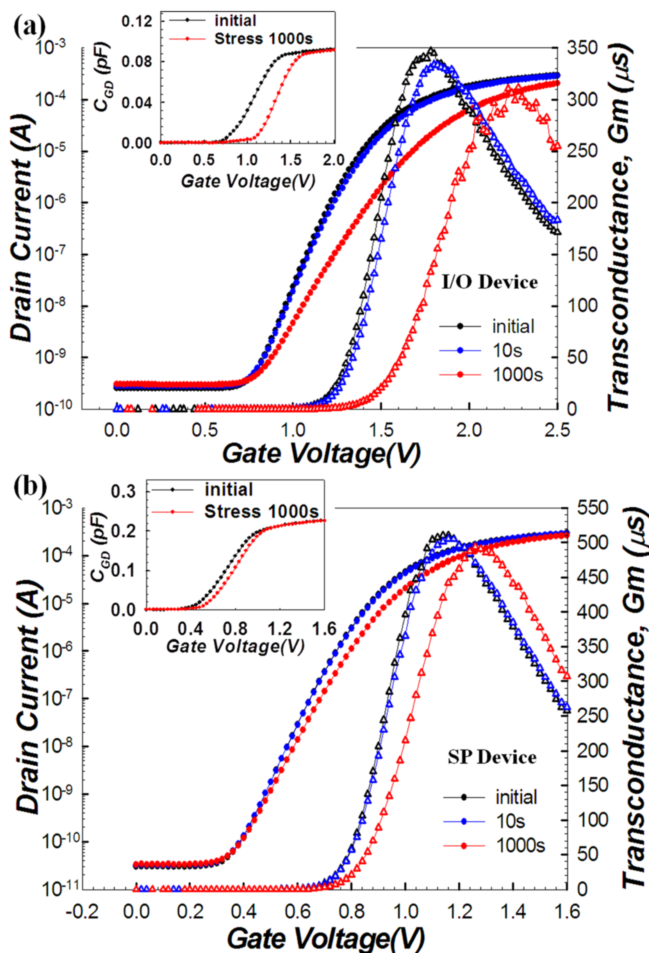

FIG. 1. I_D-V_G and corresponding G_m-V_G at linear region measurement after HCS for high k/metal gate n-MOSFETs for (a) I/O and (b) SP devices. Insets show the C_{GD} measurement after HCS.

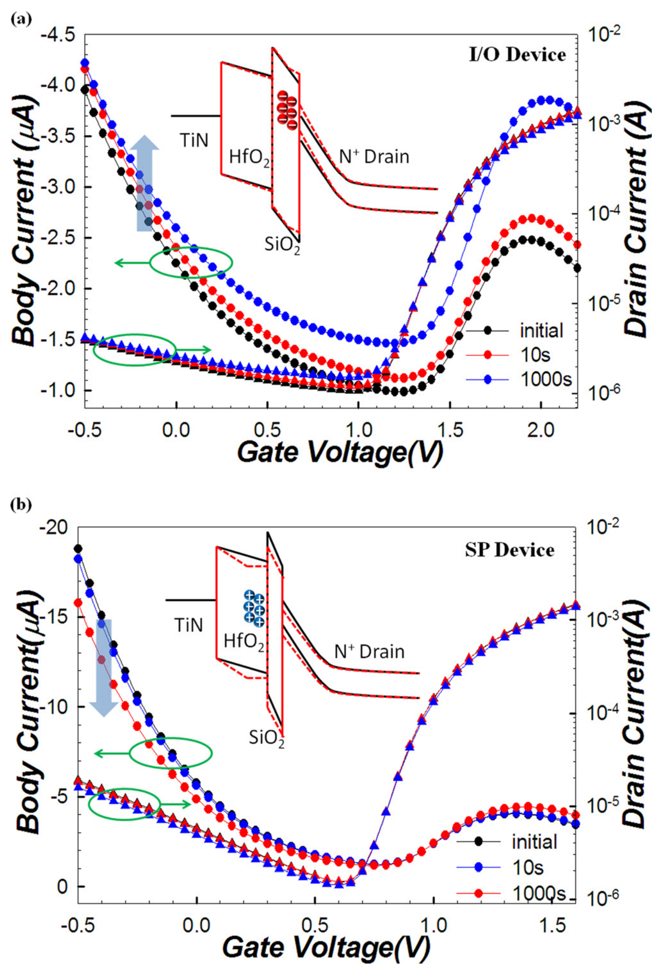

FIG. 3. I_D-V_G and corresponding I_B-V_G measurement showing GIDL current varying with stress time at $V_D = 2.4$ V for (a) I/O and (b) SP devices. Insets show (a) electron trapping decrease (b) hole trapping increase in band-to-band tunneling distance.

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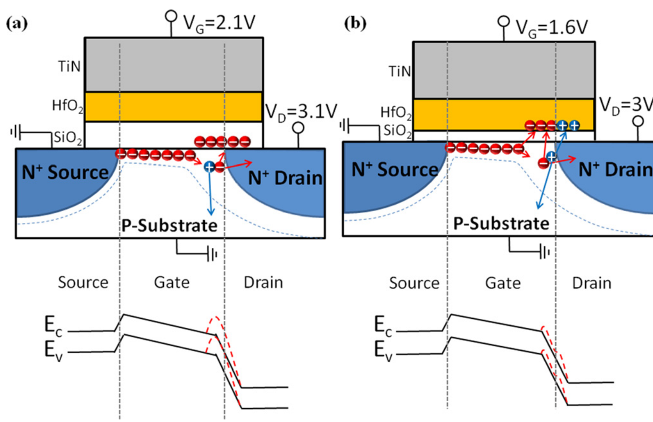

FIG. 4. Diagram of device profile corresponding to lateral energy band showing (a) electron injection into oxide layer (b) hole injection into high-k layer above overlap at drain side during HCS.

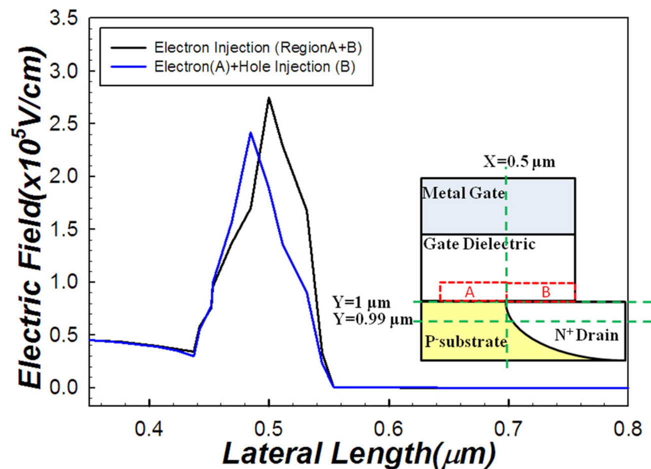

FIG. 5. The lateral electric field in T-CAD simulation at $Y = 0.99\,\mu$m. Inset shows two simulation conditions: (a) electron injection within regions A and Band (b) electron and hole injections at regions A and B, respectively.

I_B and/or I_D under off-state ($V_G < 0$) (i.e., GIDL current) shows contrary trends in I/O and SP devices after HCS. For the I/O device, GIDL current increases as stress time increases, indicating that electrons inject into the gate dielectric near the drain side and decreases the band-to-band tunneling distance, as shown in the inset of Fig. 3(a).[23] This is consistent with the previous studies which indicate lucky electron trapping in the oxide near the drain side for n-MOSFETs.[24] However, GIDL current shows hole trapping within the high-k layer for SP device under HCS. Combining this result and C_{GD} behavior indicates that the lower degradation of the SP device under HCS can be attributed to hole injection.

In further detail, the mechanism of degradation for both devices results from impact-induced mobility degradation, further decreasing I_D and G_m. Additionally, channel electron injection produces a rise in barrier height, leading to V_{th} shift. According to this, the electron injection-induced barrier height rise increases the potential difference between gate and drain (V_{GD}), as shown in Fig. 4(a). The negative charge induced by electron trapping makes the channel energy bands bend upward near the drain side, which enhances the electric field and electron kinetic energy. Under significant depletion due to the HC condition, channel electrons can still influence the rise in barrier height, gaining much kinetic energy and resulting in aggravated HC degradation.

Nevertheless, performance degradation of the SP device under HCS is lower than in the I/O device. The inset of Fig. 3(b) shows that hole trapping increases the band-to-band tunneling distance. This is because stress V_{GD} induces an electric field towards the gate, which can make positive carriers (holes) tend to move toward the gate, resulting in hole trapping. Unlike this SP device, it is difficult for hole injection to occur in I/O devices due to heavier effective mass and thicker gate oxide, even though the electric field in the gate-drain overlap is in the direction of the gate. Therefore, we would like to propose that hole trapping can counteract the electron injection-enhanced electric field. As Fig. 4(b) shows, the trapped hole could form a buffer region at the depletion region (near drain side) to reduce the electron field, in turn reducing electron kinetic energy and capability for impact ionization.

ISE-TCAD simulation provides additional support for our claim. Fig. 5 shows the lateral electric field with higher V_D for channel electron injection and for both electron and hole injections. We define SiO_2/Si interface as 1 μm along vertical direction (Y-axis) as a reference point. The extraction of electric field was selected at a position 10 nm below channel surface (i.e., $Y = 0.99\,\mu$m), deeper than the inversion layer. Two conditions are considered: (1) electron injection within regions A and B and (2) electron and hole injection at regions A and B, respectively, as shown in the inset of Fig. 5. It can be found that even far from the channel surface, the influence of carrier injection can still vary the electric field within the depletion region. For electron injection, stress electric field can be indeed enhanced. However, when electron and hole both inject into gate dielectric, the stress field becomes weaker than during only electron injection. Consequently, the result of this simulation demonstrates the behavior we proposed, indicating hole injection near the drain side can reduce stress electric field during HCS.

It has been generally thought that MOSFETs with thicker ILs can obtain good reliability but at a sacrifice to performance. However, the opposite seems supported in our experiment. I_D, G_m, and SS for the I/O device are worse than for the SP device under identical HCS conditions. This is because thinner IL more easily traps holes and these trapped holes form a buffer region at the depletion region (near the drain side) to reduce the electron field, in turn reducing the capability for impact ionization. Therefore, the hole injection reduced hot carrier degradation model was proposed to illustrate the unusual phenomenon.

Part of this work was performed at United Microelectronics Corporation. The work was supported by the National Science Council under Contract No. NSC 101-2120-M-110-002.

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