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HfO_2 nanocrystal memory on SiGe channel

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ABSTRACT

This study proposes a novel HfO_2 nanocrystal memory on epi-SiGe (Ge: 15%) channel. Because SiGe has a smaller bandgap than that of silicon, it increases electron/hole injection and the enhances program/erase speeds. This study compares the characteristics of HfO_2 nanocrystal memories with different oxynitride tunnel oxide thicknesses on Si and epi-SiGe substrate. Results show that the proposed nonvolatile memory possesses superior characteristics in terms of considerably large memory window for two-bits operation, high speed program/erase for low power applications, long retention time, excellent endurance, and strong immunity to disturbance.

1. Introduction

Nanocrystal memory has recently attracted a lot of attention for applications in next-generation nonvolatile memory [1–8]. Based on discrete storage nodes, nanocrystal memories address the important issue for vertical and lateral stored charge migration, and have great potential to achieve excellent retention characteristics. Some studies report the use of high-k dielectric materials to replace the trapping layer of silicon-oxide-nitride-oxide-silicon-like (SONOS-like) structures due to its high trapping state densities for charge-trapping efficiency improvement, deep trap energy level for better charge retention and thermodynamic stability, proper conduction and valence band offset with Si, low lattice mismatch with silicon, and excellent electrical properties [9,10]. Based on the advantages of high-k material SONOS-like memories and nanocrystal memory, HfO_2 nanocrystal memory [11,12] has the advantages of high program/erase speed (P/E speed), low power consumption for programming and erasing voltage, excellent charge retention, and better potential for scalability below the 50-nm node, according to the International Technology Roadmap for Semiconductors (ITRSs) [13]. Especially, the fabrication of HfO_2 nanocrystal memory is fully compatible with current CMOS technologies.

SiGe channel is also very attractive for device scaling down. To continue the trend of metal–oxide-semiconductor-field-effect-transistor (MOSFET) scaling, a strained SiGe channel acting as a high mobility channel has attracted a lot of interest in many studies for a long time [14–16]. Flash memory applications can use the SiGe channel to improve program/erase speed and lower the operation voltage. For programming, the drain current of flash memory devices becomes larger due to the mobility enhancement from the strain effect of SiGe layer. This increases the number of channel hot electrons, which in turn increases the likelihood of hot electrons injecting into the trapping layer under the same gate voltage. For erasing, the band-to-band tunneling (BTBT) current increases dramatically with increasing Ge content in SiGe channel because the generation rate of electron–hole pairs is exponentially inversely proportional to the band gap [17,18]. As the electron hole pairs generation increases, the number of electron tunneling through the tunneling oxide increases, improving the P/E speed. Therefore, the SiGe channel can improve the program and erase speeds of flash devices while lowering operation voltage. Introducing the SiGe channel into flash devices allows low power consumption and high operating efficiency.

This study explores the newly-proposed nonvolatile flash memories with HfO_2 nanocrystals and epi-SiGe channel (Ge: 15%) for improving memory performance, and discusses the use of oxynitride tunnel oxide with different thicknesses. The epi-SiGe channel achieved high program/erase speeds because the SiGe bandgap is smaller than that of silicon, implying increased electron/hole injection. As a result, combining SiGe channel and HfO_2 nanocrystals

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produced superior flash memory characteristics, such as a larger memory window, high P/E speeds, long retention time, excellent endurance, and strong immunity to disturbance.

2. Experimental

Fig. 1 shows the fabrication process of the HfO_2 nanocrystal memory. This figure provides an example of the fabrication process of the HfO_2 nanocrystal SiGe memory devices using a LOCOS isolation process on a p-type, 5–10 Ω cm, (100) 150-mm silicon substrate (Fig. 1). First, 120 nm SiGe channel (Ge: 15%) was grown by an ultra high vacuum chemical vapor deposition system (UHVCVD). Then, 2 nm and 5 nm thick oxynitride tunnel layer was thermally grown at 900 °C in a furnace system. The other splits were grown the same tunnel layer on silicon substrate for comparison. A 12-nm-thick amorphous $HfSiO_x$ silicate layer was then deposited by co-sputtering with pure silicon (99.9999% pure) and pure hafnium (99.9% pure) targets in an oxygen gas ambient. The co-sputtering process was performed at 7.6×10^{-3} Torr at room temperature with precursors of O_2 (3 sccm) and Ar (24 sccm); both dc sputter powers were set at 150 W. The samples were then subjected to RTA treatment in an O_2 ambient at 900 °C for 1 min to convert the $HfSiO_x$ silicate film into separated HfO_2 and SiO_2 phases to form HfO_2 nanocrystals [11,12]. A blocking oxide of 8-nm thickness was then deposited through high-density-plasma chemical vapor deposition (HDPCVD), followed by a N_2 densification process at 900 °C for 1 min. Poly-Si deposition, gate patterning, source/drain (S/D) implanting, and other standard CMOS procedures were subsequently completed to fabricate the HfO_2 nanocrystal memory devices. The Ge ratio of SiGe epi layer was 15%. The band gap of SiGe channel can be modulated by tuning its Ge contents [17,18]. Table 1 summarizes the split table for these experiments. The insert graph shows the I_d–V_g curve for the SiGe channel and Si device. Results shows that the drain current of SiGe channel device is about 1 order better than the Si channel at the same size (W/L = 2 μm/2 μm).

3. Results and discussion

Figs. 2a and 2b show the programming and erasing characteristics, respectively, of the fabricated HfO_2 nanocrystal memory on the SiGe substrate with two different tunnel oxide thicknesses 2 nm and 5 nm. The experiments in this study used channel hot

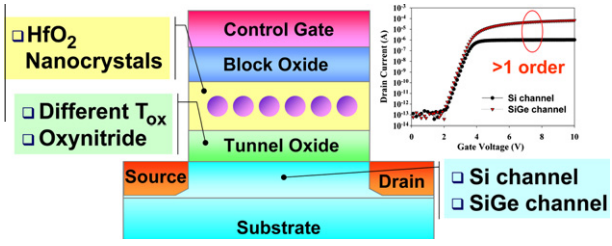

Fig. 1. Schematic cross section and split process of the HfO_2 nanocrystal memories.

Table 1
Split table of the HfO_2 nanocrystal SiGe memories.

	S/D type	Blocking oxide	Trapping layer	Tunnel oxide
SiGe epi	nMOS	SiO_2	HFO_2 nanocrystals	Oxynitride (2 nm, 5 nm)
Si substrate				Oxynitride (2 nm, 5 nm)

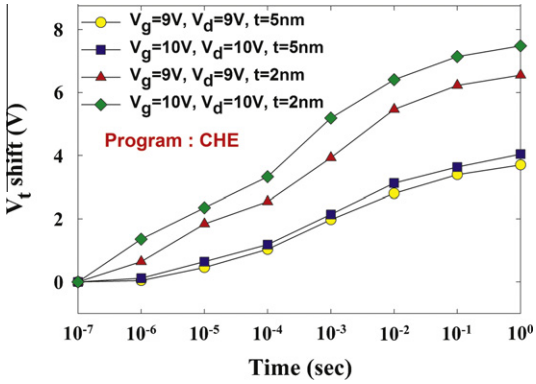

Fig. 2a. Program characteristics of HfO_2 nanocrystal memories on SiGe substrate with different tunnel oxide thickness.

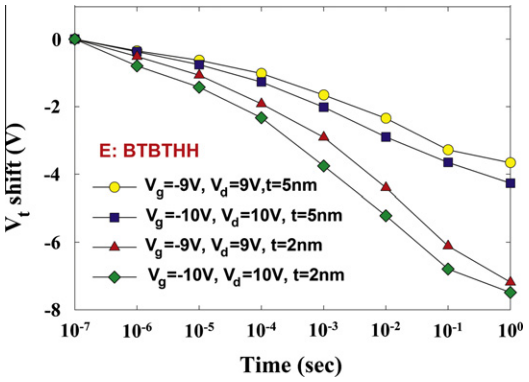

Fig. 2b. Erase characteristics of HfO_2 nanocrystal memories on SiGe substrate with different tunnel oxide thickness.

electron for programming and band-to-band hot hole for erasing. The bias conditions for programming were V_g = 10 V and V_d = 10 V, and V_g = 10 V and V_d = −10 V for erasing. Since the channel length of our memory cells was of 2 μm, the applied drain voltages should be sufficiently large for rapid programming and erasing. As the memory cell is continuously scaled, the applied voltage shall be lowered accordingly for controlling the power consumption. The memory with thinner tunnel oxide exhibited slightly improved program speed and better erasure performance when operated with the short pulse width. Figs. 3a and 3b show the program and erase characteristics of HfO_2 nanocrystal memories on the Si and SiGe substrates. The memory device on the SiGe substrate achieved high speed program/erase (10 μs/0.1 ms) performance with a 2 V memory window. The boost on programming speed may come from mobility enhancement from the strain effect of SiGe layer, as suggested by the increased drain current of the memory device in the insert graph of Fig. 1. Thus, more channel hot electrons were generated and had a higher probability of injecting into the trapping layer through tunneling oxide under the same gate voltage. For the erasing speed enhancement, band-to-band tunneling current increased due to the small band gap SiGe channel and its enhanced generation rate of electron–hole pairs. As a result, the SiGe channel significantly improved the program and erase speeds of the flash device.

Fig. 4 illustrates the retention time characteristics the fresh HfO_2 nanocrystal memory devices on the Si and SiGe substrate with two different tunnel oxide thicknesses at a testing temperature of 25 °C. The retention characteristic of 20% charge loss was almost the same up to 10^8 s for both 5 nm tunnel oxide splits. This good retention performance can be ascribed to the sufficiently deep trap energy

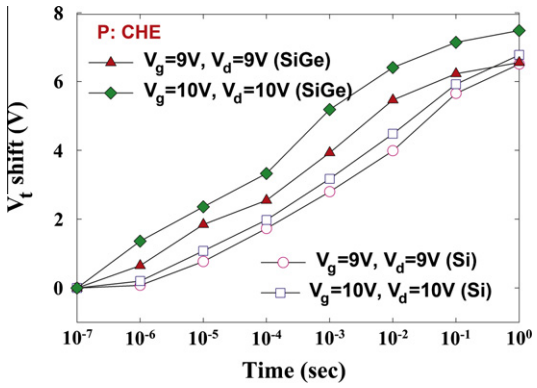

Fig. 3a. Program characteristics of HfO_2 nanocrystal memories on the Si substrate and SiGe substrate.

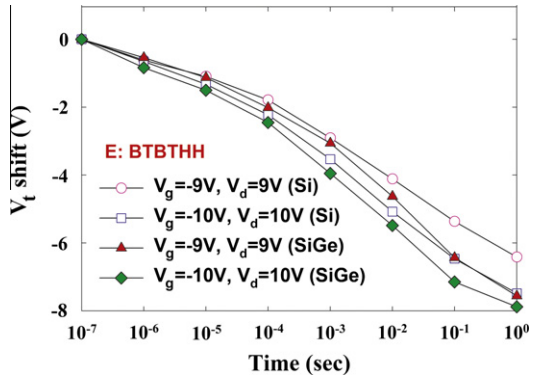

Fig. 3b. Erase characteristics of HfO_2 nanocrystal memories on the Si substrate and SiGe substrate.

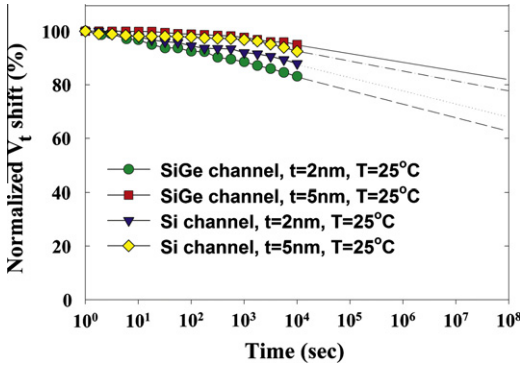

Fig. 4. Retention time characteristics the fresh HfO_2 nanocrystal memory on Si and SiGe channel with two different tunnel oxide thicknesses at a testing temperature of 25 °C.

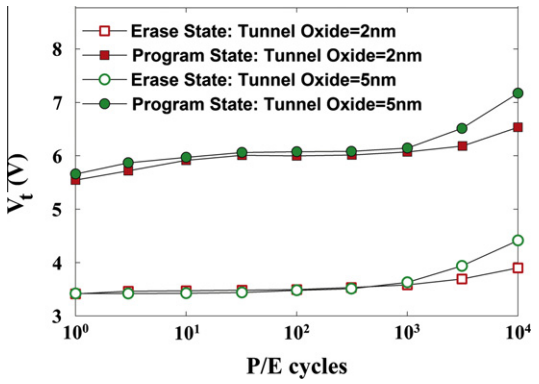

Fig. 5. Endurance characteristics with different tunnel oxide thicknesses after 10^4 P/E cycles.

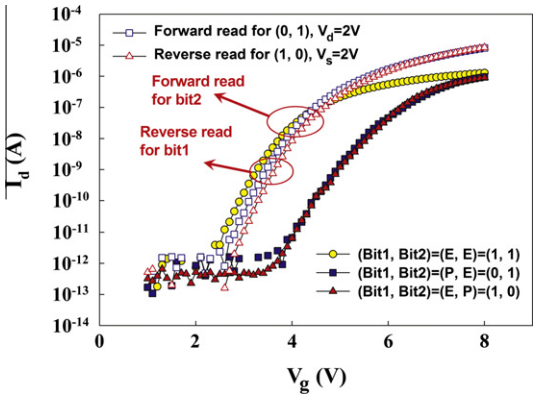

Fig. 6. 2 bits/cell operation for the SiGe HfO_2 nanocrystal memory. E: erased; P: programmed; Bit1: drain side; Bit2: source side.

levels in hafnium silicate [19,20]. Compared with 2 nm tunnel oxide splits, the SiGe channel device showed slightly worse characteristics than the control sample. The quality of this thin tunneling oxide grown on epi-SiGe layer may not have been good enough, allowing the stored charge to leak out, decreasing retention poorer. Fig. 5 shows the endurance characteristics with different tunnel oxide thicknesses after 10^4 P/E cycles. Despite significant memory window narrowing, a memory window of approximately 2 V remained even after 10^3 P/E cycles. The cause of the narrowing over cycling might be due to two factors. The first factor is the mismatch between the localized spatial distributions for the injected electrons and holes due to channel hot-electron programming and band-to-band hot-hole erasing. Uncompensated electrons might cause the V_t to increase gradually over P/E cycling [21–23]. The second factor is the stress-induced electron traps generated in the tunnel oxide during cycling. The rate of memory window narrowing increased upon increasing P/E cycles, while the one with thick tunnel oxide exhibited more serious memory window closure. Fig. 6 demonstrates the feasibility of performing two-bit operation with the proposed HfO_2 nanocrystal SiGe memory through a reverse read scheme in a single cell. The I_{ds}–V_{gs} curves clearly indicate that forward and reverse reads can detect the information stored in the programmed Bit1 and Bit2, respectively. The logical "1" indicates that electrons were erased in the storage node. As an example, (Bit1, Bit2) = (1,0) means that Bit1 is in its erased state and Bit2 is in its programmed state. To demonstrate the two-bit effect, a programming bias is firstly applied to write electrons into Bit2 by CHE injection. The accelerated electrons are injected into the narrow region in trappering layer near the source junction. Then, V_s = 2 V was applied for reverse reading of bit1. Second, V_d = 2 V was applied for forward reading of Bit2. In reverse reading, the read voltage had be large enough to generate a depletion region, which can be extended to screen out the localized trapped charges at source side, such that the programmed cell has low V_{th} (or high current). Thus, a significant threshold shift of ΔV_{th} = 2 V between these (1,0)-reverse and (1,0)-forward curves is observed. Table 2 summarizes the bias conditions for two-bit operation.

Fig. 7 demonstrates the erase-state threshold voltage instability induced by read disturbance of HfO_2 nanocrystal SiGe memory cell with 2 nm tunnel oxide under several operation conditions. For

Table 2
The bias conditions summary table for two-bit operation.

		Program (V)	Erase (V)	Read (V)
Bit1	V_g	9	−9	2
	V_d	9	9	0
	V_s	0	0	2
Bit2	V_g	9	−9	2
	V_d	0	0	2
	V_s	9	9	0

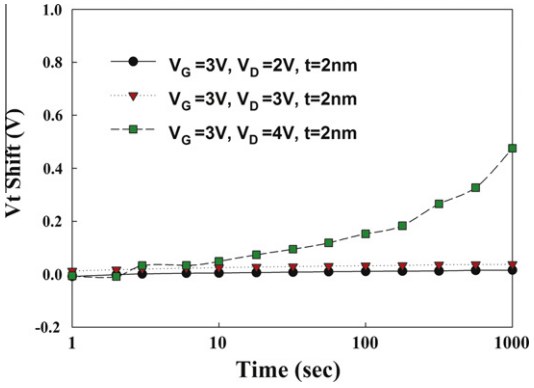

Fig. 7. Read disturbance induced erase-state threshold voltage instability in 2 nm tunnel oxide HfO_2 nanocrystal SiGe memory cell.

two-bit operation, the applied bitline voltage in a reverse-read scheme must be large enough (>1.5 V) to "read through" the trapped charge in the neighboring bit. The read-disturb effect is the result of two factors: the word-line voltage and the bit-line voltage. The word-line voltage during read may enhance room temperature (RT) drift in the neighboring bit [24]. On the other hand, a relatively large read bit-line voltage may cause unwanted channel hot-electron injection, which subsequently results in a significant threshold voltage shift of the neighboring bit. The experiments in this study applied gate and drain biases and grounded the source. Results clearly demonstrated that almost no read disturbance occurred in the HfO_2 nanocrystal SiGe-channel flash memory under low-voltage reading (V_g = 3 V; V_d = 2 V). For a larger memory window, only a small read disturbance (ca. 0.45 V) appeared after operating at V_d = 4 V after 1000 s at 25 °C. Fig. 8 shows the programming drain disturbance of the proposed HfO_2 nanocrystal SiGe flash memory. Two different drain voltages (V_d = 8 and 10 V) were applied in the programming drain disturbance measurement for the devices with two different tunnel oxides 2 nm and 5 nm. A sufficient programming drain disturb margin existed (ΔV_t < 0.4 V) for the device with as thin as 2 nm oxide after programming at a V_d value of 10 V for 1000 s. Fig. 9 shows the gate disturbance characteristics in the erasing state. Gate disturbance may occur during programming for cells sharing a common word-line when one of the cells is being programmed. A threshold voltage shift of only 0.55 V, i.e., negligible disturbance, appeared under the following conditions: V_g = 10 V; $V_s = V_d = V_{sub}$ = 0 V; stressed for 1000 s. Exactly why this memory exhibited such excellent gate disturb characteristics with such a thin tunnel oxide is unclear; a non-negligible current would be present in the tunnel oxide when a voltage of 10 V was applied to the gate electrode. Using a serial capacitor voltage divider model, the voltage drop at the tunnel oxide was estimated at 1.07 V if the trapping layer is assumed to be a HfO_2 film, rather than nanocrystal. Even though a 1.07 drop causes a significant leakage current through an individual 2 nm oxide layer, the data retention in the memory cell is related to the direct tunneling leakage current induced by such a

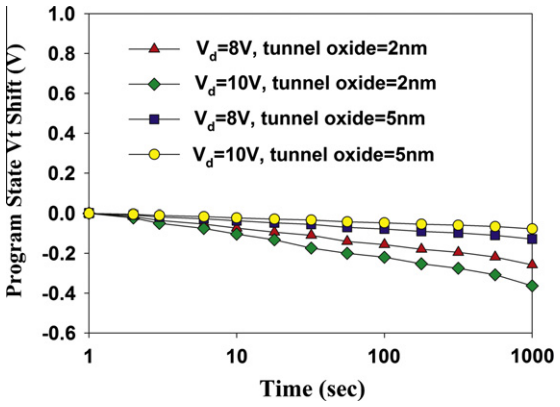

Fig. 8. Programming drain disturbance of the proposed HfO_2 nanocrystal SiGe flash memory.

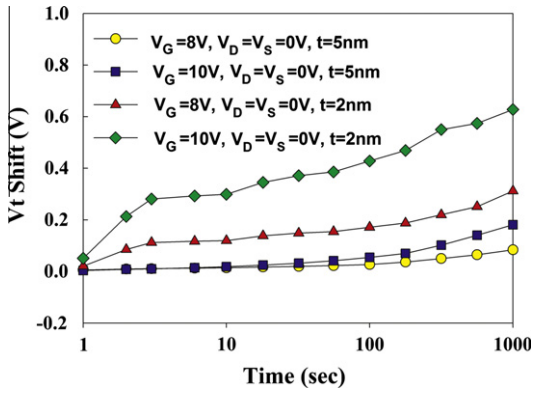

Fig. 9. Gate disturbance characteristics in the erasing state.

voltage and the total tunneling situation in the whole gate stack. In other words, the effect of the potential barrier presented by a high-k material on the tunneling current must be taken into account. It is incorrect to state that a large direct tunneling current will definitely exist in the interfacial layer and, in turn, that it will induce significant disturbance during programming.

4. Conclusion

This study proposed a novel, simple, and reliable technique for HfO_2 nanocrystals with SiGe channel (Ge: 15%). Electron/hole injection increased because SiGE has a smaller bandgap than silicon. The proposed design achieved superior characteristics in terms of large memory windows, high speed program/erase, long retention time, excellent endurance, no significant disturbance, and 2-bit operation. Given this superior performance, HfO_2 nanocrystal flash memory on SiGe channel is suitable for two-bit operation and has great potential for replacing the ONO stack in conventional SONOS-type Flash memories.

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References

[1] Liu Zengtao, Lee Chungho, Narayanan Venkat, Pei Gen, Kan Edwin Chihchuan. Metal nanocrystal memories – part I: device design and fabrication. IEEE Trans Electron Dev 2002;49(9):1606–13.

[2] Liu Zengtao, Lee Chungho, Narayanan Venkat, Pei Gen, Kan Edwin Chihchuan. Metal nanocrystal memories – part II: electrical characteristics. IEEE Trans Electron Dev 2002;49(9):1614–22.
[3] De Blauwe Jan. Nanocrystal nonvolatile memory devices. IEEE Trans Nanotechnol 2002;1(1):72–7.
[4] Zhou Huimei, Li Bei, Yang Zheng, Zhan Ning, Yan Dong, Lake Roger K, et al. TiSi2 nanocrystal metal oxide semiconductor field effect transistor memory. IEEE Trans Nanotechnol 2011;10(3):499–505.
[5] Chen Jing Hao, Wang Ying Qian, Yoo Won Jong, Yeo Yee-Chia, Samudra Ganesh, Chan Daniel SH, et al. Nonvolatile flash memory device using ge nanocrystals embedded in hfalo high-k tunneling and control oxides: device fabrication and electrical performance. IEEE Trans Electron Dev 2004;51(11):1840–8.
[6] Liu Yueran, Dey Sagnik, Tang Shan, Kelly David Q, Sarkar J, Banerjee Sanjay K. Improved performance of sige nanocrystal memory with VARIOT tunnel barrier. IEEE Trans Electron Dev 2006;53(10):2598–602.
[7] Jung JH, Jin JY, Lee I, Kim TW, Roh HG, Kim Y-H. Memory effect of ZnO nanocrystals embedded in an insulating polyimide layer. Appl Phys Lett 2006;88:112107.
[8] Ammendola Giuseppe, Ancarani Valentina, Triolo Virginia, Bileci Marco, Corso Domenico, Crupi Isodiana, et al. Nanocrystal memories for FLASH device applications solid-state electronics. Solid-State Electron 2004;48(9):1483–8.
[9] Min Fang Hung, Yung Chun Wu, Zih Yun Tang. High performance gate-all-around poly-Si nanowire with Si nanocrystals nonvolatile memory. Appl Phys Lett 2011;98:162108.
[10] Gritsenko VA, Nasyrov KA, Novikov Yu N, Aseev AL, Yoon SY, Lee Jo-Won, et al. A new low voltage fast SONOS memory with high-k dielectric. Solid-State Electron 2003;47(10):1651–6.
[11] Lin Yu-Hsien, Chien Chao-Hsin, Lin Ching-Tzung, Chang Chun-Yen, Lei Tan-Fu. Novel two-bit HfO_2 nanocrystal nonvolatile flash memory. IEEE Trans Electron Dev 2006;53(4):782–9.
[12] Lin Yu-Hsien, Chien Chao-Hsin, Lin Ching-Tzung, Chang Chun-Yen, Lei Tan-Fu. High performance nonvolatile HfO_2 nanocrystal memory. Electron Dev Lett 2005;26(3):154.
[13] International technology roadmap for semiconductors (ITRSs); 2010.
[14] Welser J, Hoyt JL, Gibbons JF. Electron mobility enhancement in strained-Si n-type metal–oxide-semiconductor field-effect transistors. Electron Dev Lett 1994;15(3):100–2.
[15] Ghani T, Armstrong M, Auth C, Bost M, Charvat P, Glass G, et al. A 90 nm high volume manufacturing logic technology featuring novel 45 nm gate length strained silicon CMOS transistors. Int Electron Dev Meeting (IEDM) 2003:11.6.1–3.
[16] Fossum Jerry G, Zhang Weimin. Performance projections of scaled CMOS devices and circuits with strained Si-on-SiGe channels. IEEE Trans Electron Dev 2003;50(4):1042–9.
[17] Weltzer LM, Banerjee SK. Enhanced CHISEL programming in flash memory devices with SiGe buried layer. Non-Volatile Memory Technology Symposium; 2004. p. 31–3.
[18] Wang Chi-Chao, Chang-Liao Kuei-Shu, Lu Chun-Yuan, Wang Tien-Ko. Enhanced band-to-band-tunneling-induced hot-electron injection in p-channel flash by band-gap offset modification. Electron Dev Lett 2006;27(9):749–51.
[19] Sugizaki T, Kobayashi M, Ishidao M, Minakata H, Yamaguchi M, Tamura Y, Sugiyama Y, Nakanishi T, Tanaka H. Novel multi-bit SONOS type flash memory using a high-k charge trapping layer. In: Proc VLSI Symp Technology Dig Technical papers; 2003. p. 27–8.
[20] Zhu WJ, Ma Tso-Ping, Tamagawa Takashi, Kim J, Di Y. Current transport in metal/hafnium oxide/silicon structure. IEEE Electron Dev Lett 2002;23(2):97–9.
[21] Shappir Assaf, Lusky Eli, Cohen Guy, Bloom Ilan, Janai Meir, Eitan Boaz. The two-bit NROM reliability. IEEE Trans Dev Mater Reliab 2004;4:397–403.
[22] Vianello Elisa, Driussi Francesco, Esseni David, Selmi Luca, Widdershoven Frans, van Duuren Michiel J. Explanation of SILC probability density distributions with nonuniform generation of traps in the tunnel oxide of flash memory arrays. IEEE Trans Electron Dev 2007;54:1953–62.
[23] Naseer Babu P, Govind G, Prasad SMS, Bhat KN. Electrical and reliability studies of wet N_2O tunnel oxides grown on silicon for flash memory applications. IEEE Trans Electron Dev 2007;7:420–8.
[24] Tsai WJ, Yeh CC, Zous NK, Liu CC, Cho SK, Wang T, et al. Positive oxide charge-enhanced read disturb in a localized trapping storage flash memory cell. IEEE Trans Electron Dev 2004;51(3):434–9.