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PMOS-based power-rail ESD clamp circuit with adjustable holding voltage controlled by ESD detection circuit

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ABSTRACT

A new power-rail ESD clamp circuit designed with PMOS as main ESD clamp device has been proposed and verified in a 65 nm 1.2 V CMOS process. The new proposed design with adjustable holding voltage controlled by the ESD detection circuit has better immunity against mis-trigger or transient-induced latch-on event. The layout area and the standby leakage current of this new proposed design are much superior to that of traditional *RC*-based power-rail ESD clamp circuit with NMOS as main ESD clamp device.

1. Introduction

In advanced nanoscale CMOS process, electrostatic discharge (ESD) protection has become the major concern of reliability for integrated circuits (ICs). The nanoscale device with thinner gate oxide and shallower diffusion junction depth seriously degrades the ESD robustness of ICs and raises the difficulty of ESD protection design for ICs implemented in nanoscale CMOS technology [1]. Therefore, an efficient ESD protection element is highly required by IC industry. To achieve whole-chip ESD protection, the power-rail ESD clamp circuit is a vital basis, as shown in Fig. 1 [2]. In Fig. 1, the power-rail ESD clamp circuit can protect the internal circuits with efficient discharging path under various ESD stress conditions.

The ESD clamp device drawn in the layout style of big field-effect transistor (BigFET) had revealed excellent ESD protection performance in advanced nanoscale CMOS ICs [3–6]. For the ESD-transient detection circuit, there are two design skills, the *RC*-delay [3,4] and the capacitance-coupling designs [5,6], to effectively trigger the BigFET transistor under ESD stress condition. The traditional *RC*-based power-rail ESD clamp circuit is shown in Fig. 2. The *RC* time constant is generally designed large enough about several hundreds nanosecond to keep the ESD clamp device at "ON" state under ESD stress condition. However, the extended *RC* time constant of the ESD-transient detection circuit suffers not only the larger layout area but also the mis-trigger of the ESD clamp circuit under fast-power-on or "hot-plug" applications [3].

Besides, low standby leakage of the ESD clamp circuit is highly demanded by the hand-held, portable, and battery powered products. In advanced CMOS technology, the leakage current of NMOS was often larger than that of PMOS in the same device dimension. Therefore, PMOS is suggested to be used as ESD clamp device [7].

In this work, the parasitic capacitance of the ESD clamp PMOS transistor drawn in BigFET layout style is used as a part of ESD-transient detection circuit. This new design has been verified in a 65 nm 1.2 V CMOS technology. From the measured results, the proposed power-rail ESD clamp circuit has features of area efficiency, low leakage current, and high immunity against mis-trigger.

2. New power-rail ESD clamp circuit

2.1. New ESD-transient detection circuit

The new proposed power-rail ESD clamp circuit is illustrated in Fig. 3. The ESD-transient detection circuit consists of two transistors (M_n and M_p), two resistors (R_n and R_p), and diode string. The PMOS transistor drawn in BigFET layout style (M_{clamp}) is used as ESD clamp device. The gate terminal of M_{clamp} is linked to the output of the ESD-transient detection circuit, which can command M_{clamp} at "ON" or "OFF" state.

In Fig. 3, the diode string in ESD-transient detection circuit is used to adjust the holding voltage to overcome the transient-induced latch-on issue. In this work, the ESD-transient detection circuits with zero, one, and two diodes were investigated in silicon chip. The measured results reveal that the holding voltage of the power-rail ESD clamp circuit can be adjusted by modifying the

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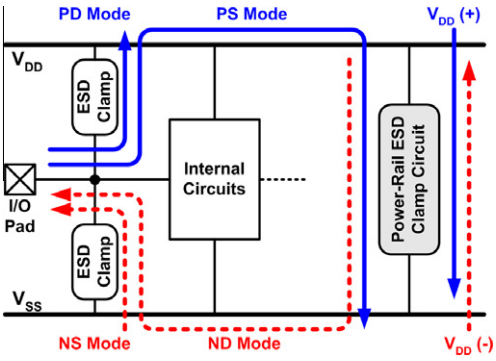

Fig. 1. Whole-chip ESD protection design with power-rail ESD clamp circuit under different ESD stress conditions.

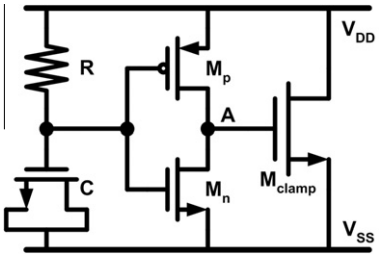

Fig. 2. Traditional *RC*-based power-rail ESD clamp circuit.

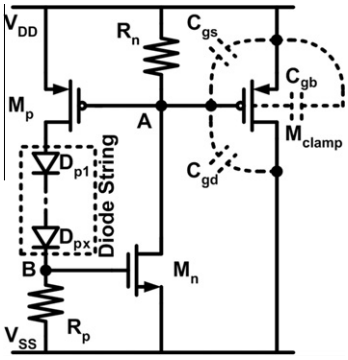

Fig. 3. Proposed power-rail ESD clamp circuit with diode string in the ESD-transient detection circuit.

number of the diodes in the ESD-transient detection circuit. In addition, the new proposed power-rail ESD clamp circuit can be totally turned off after power-on transition because the nodes A and B are kept at V_{DD} and V_{SS} through the resistors R_n and R_p, respectively.

Verified in the test chip, the ESD clamp PMOS transistor is drawn in BigFET layout style without silicide blocking in a 65 nm 1.2 V CMOS process. Compared with the power-rail ESD clamp circuit with the traditional *RC*-based ESD-transient detection circuit, the layout area of the new proposed ESD-transient detection circuit is much smaller, as illustrated in Fig. 4a–d. The dimension of M_{clamp} in all circuits verified in the silicon test chip is kept the same of 2000 μm/0.1 μm. According to the layout area of the new proposed power-rail ESD clamp circuits, the cell height of the whole power-rail ESD clamp circuit is reduced by 30%, and the layout area of the ESD-transient detection circuit is reduced by 54.5%.

2.2. Operation principle under ESD stress

The ESD clamp PMOS transistor is drawn in BigFET without silicide blocking. Large C_{gd}, C_{gs}, and C_{gb} parasitic capacitances essentially exist in the ESD clamp PMOS transistor. These parasitic capacitances and the resistor R_n can be used to realize capacitance-coupling mechanism in the power-rail ESD clamp circuit. In Fig. 3, the gain (G) of the coupling effect caused by C_{gd}, C_{gs}, C_{gb}, and R_n during the positive V_{DD}-to-V_{SS} ESD stress condition can be expressed as:

$$G = \frac{V_A}{V_{DD}} = \left| \frac{\frac{1}{j\omega C_{gd}}}{\frac{1}{j\omega C_{gd}} + \left(\frac{1}{R_n} + j\omega(C_{gs} + C_{gb})\right)^{-1}} \right| \quad (1)$$

According to the device sizes used in this work, the gain is 0.64 with $C_{gd} \fallingdotseq C_{gs}$ = 0.44 pF, C_{gb} = 0.35 pF, R_n = 40 kΩ, and signal frequency of 50 MHz derived from 5 ns fast-rising edge of the ESD voltage pulse.

A 3 V voltage pulse with a rise time of 5 ns is applied to the V_{DD} node while the V_{SS} node was grounded to simulate the fast-rising edge of the HBM ESD event, as shown in Fig. 5a. The coupling voltage at node A (V_A) of the proposed circuit is exactly equal to 0.64 V_{DD} before the ESD-transient detection circuit is turned on. When the voltage difference between V_{DD} and V_A is getting larger, the sub-threshold current of M_p can produce enough voltage difference on R_p to further turn on M_n, the V_A will be quickly pulled down to the ground level to trigger on the ESD clamp PMOS transistor. In Fig. 5b, the pulled-down V_A of the proposed circuit can be kept at low voltage level during whole voltage pulse duration. However, the V_A in the traditional *RC*-based power-rail ESD clamp circuit, as shown in Fig. 2, is elevated to the voltage level higher than the NMOS threshold voltage of ~0.58 V for only the first period of ~300 ns. The design parameters, including the device sizes of each transistor and resistor, are listed in Table 1.

According to the design window of the ESD protection circuit for avoiding the latch-on issue, the holding voltage (V_h) of the ESD protection circuit is an important index to exceed the normal circuit operation voltage V_{DD}. The holding voltage of the proposed power-rail ESD clamp circuit can be indicated as:

$$\begin{aligned} V_h &= V_{ds(M_p)} + nV_{ON(Diode)} + V_{gs(M_n)} \\ &= V_{ds(M_p)}\big|_{I_{ds}=V_{THN}/R_p} + nV_{ON(Diode)} + V_{THN} \approx nV_{ON(Diode)} + V_{THN}, \end{aligned} \quad (2)$$

where n and V_{ON} are the number and the turn-on voltage of the diode, respectively. Based on the simulation results, the V_h can be represented as the summation of V_{ON} (0.71 V) and V_{THN} (0.58 V) due to minor V_{ds} (~few milli-volt).

For the new proposed power-rail ESD clamp circuit with zero diode in Fig. 3, the V_h would be only 0.58 V. It would be a high risk to apply this structure to the circuit with 1.2 V operation voltage. However, the V_h can be theoretically adjusted to 1.29 V and 2.00 V by adding the diodes in the ESD-transient detection circuit. The new proposed power-rail ESD clamp circuit with adjustable holding voltage can be safely applied to protect any internal circuits from the transient-induced latch-on event.

3. Experimental results

The test chip to verify the proposed power-rail ESD clamp circuit has been fabricated in a 65 nm 1.2 V CMOS process. As shown in Fig. 6a and b, the layout area of the proposed ESD-transient detection circuit is reduced by 54.5% from that of traditional *RC*-based one.

3.1. DC I–V measurement

The leakage currents of the power-rail ESD clamp circuits at 1.2 V normal circuit operation voltage are measured in Fig. 7. The leakage current of the traditional *RC*-based power-rail ESD clamp circuit is 86.9 nA at room temperature. However, the proposed

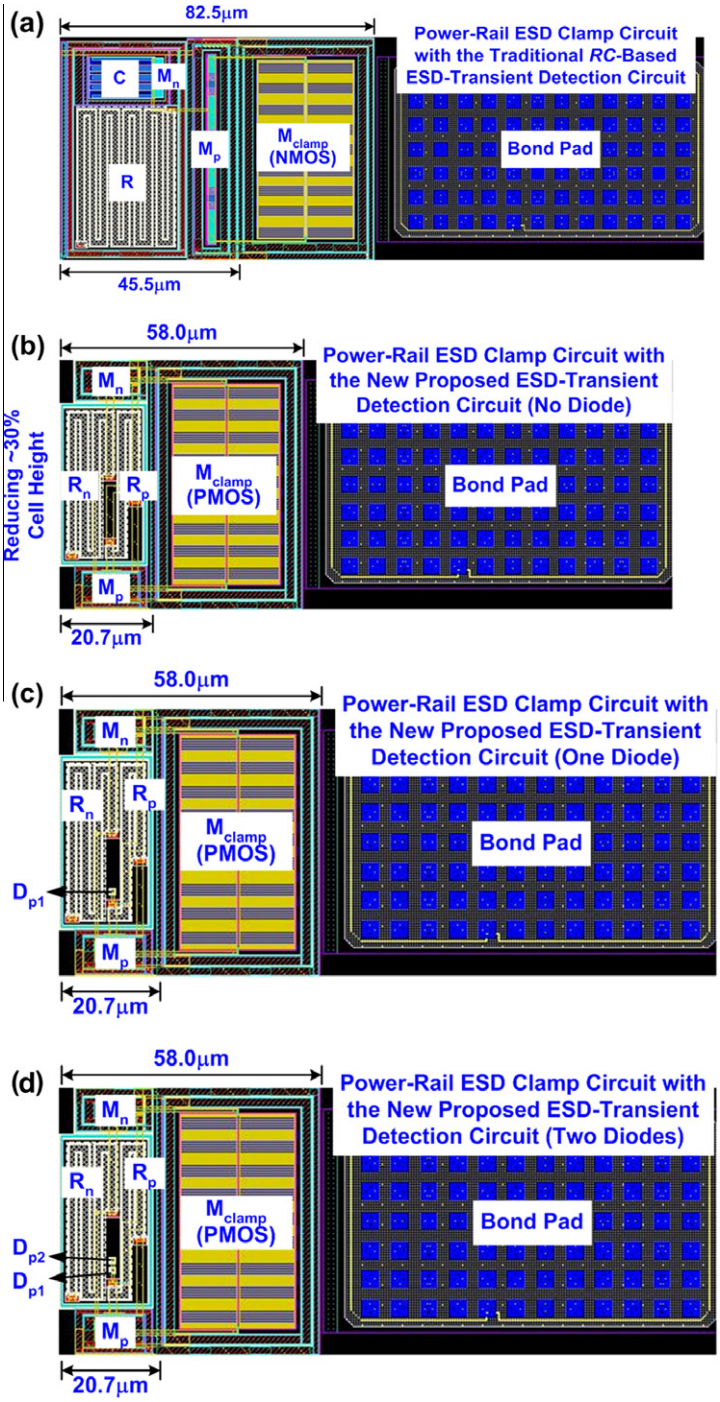

Fig. 4. Comparison on the layout areas among the four power-rail ESD clamp circuits. The M_{clamp} is drawn in a BigFET layout style with the same W/L = 2000 μm/0.1 μm, which is triggered by (a) the traditional *RC*-based ESD-transient detection circuit, (b) the proposed ESD-transient detection circuit with no diode, (c) the proposed ESD-transient detection circuit with one diode and (d) the proposed ESD-transient detection circuit with two diodes.

power-rail ESD clamp circuits with different numbers of diodes have the leakage currents in the range of 15–17 nA. The leakage current of the proposed power-rail ESD clamp circuit is largely reduced by 80.4%. Therefore, the proposed power-rail ESD clamp circuit with lower leakage current is more adequate for the portable products, which highly require low standby leakage current.

3.2. Transmission Line Pulsing (TLP) measurement and ESD robustness

The transmission line pulsing (TLP) generator with a pulse width of 100 ns and a rise time of ~2 ns is used to measure the fabricated power-rail ESD clamp circuits [8]. As shown in Fig. 8a, there are no differences among the curves higher than 3.5 V because the device sizes of M_{clamp} in all proposed power-rail ESD clamp circuits are the same. The second breakdown currents (It_2) of the traditional *RC*-based and the proposed power-rail ESD clamp circuits are 5.44A and 5.01A, respectively.

The measured holding voltages of the proposed ESD-transient detection circuits with zero, one, and two diodes are 0.56 V, 1.25 V, and 2.12 V, respectively, as shown in Fig. 8b. They are very close to the theoretical ones of 0.58 V, 1.29 V, and 2.00 V calculated from Eq. (2). The ESD-transient detection circuit with the

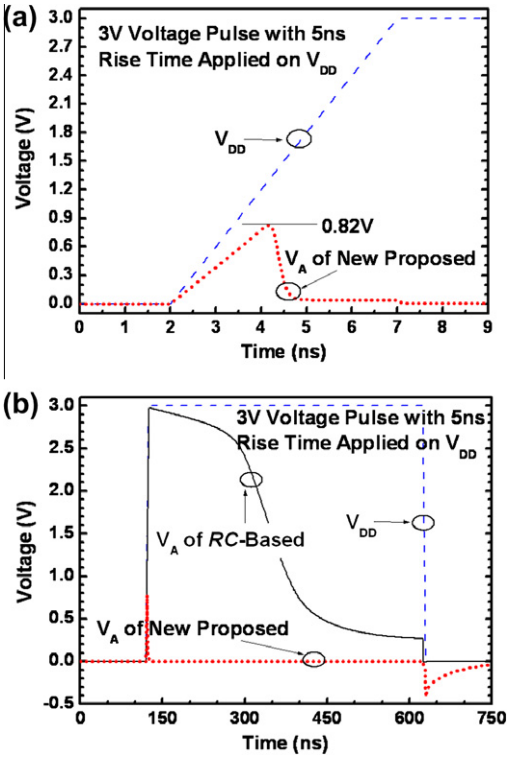

Fig. 5. The simulation results of the voltage transient on V_{DD} and node A under a 3 V voltage pulse with a rise time of 5 ns. (a) The voltage waveforms in the period of rising transition and (b) the voltage waveforms during the whole voltage pulse of 500 ns.

Table 1
The device sizes of the power-rail ESD clamp circuits.

Design parameters	*RC*-based ESD clamp circuit (NMOS)	New proposed ESD clamp circuit (PMOS)
Capacitor	64 μm/2 μm (*W*/*L*)	None
Resistor (Ω)	*R* = 113 k	R_n = 40 k; R_p = 20 k
PMOS transistor (M_p)	184 μm/60 nm	24 μm/60 nm
NMOS transistor (M_n)	36 μm/60 nm	12 μm/60 nm
ESD clamp transistor (M_{clamp})	2000 μm/100 nm	2000 μm/100 nm
Diode (D_n)	None	0.057 μm^2

adjustable holding voltage has been successfully verified, which can be safely applied to protect any internal circuits from the transient-induced latch-on event.

Table 2 shows the HBM and MM ESD robustness of these four power-rail ESD clamp circuits. The HBM ESD robustness of all power-rail ESD clamp circuits are over 8 kV. The MM ESD robustness of the traditional *RC*-based and the proposed power-rail ESD clamp circuits are 450 V and 350 V, respectively.

3.3. Turn-On verification

For the turn-on verification, a 3 V voltage pulse with 5 ns rise time to simulate the rising transition of HBM ESD event is applied to the V_{DD} power line with the grounded V_{SS}. In Fig. 9a, the voltage waveform of the traditional *RC*-based design rises as the time increases. On the contrary, the voltage waveforms of the proposed designs with different numbers of diodes are clamped to the specific voltage levels during the whole pulse duration due to the positive feedback mechanism in the proposed ESD-transient detection circuit.

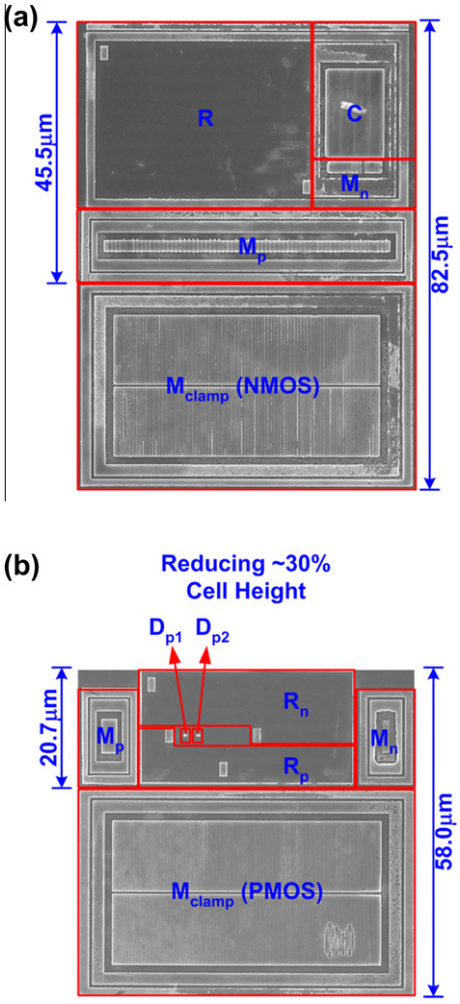

Fig. 6. Chip microphotographs of (a) the traditional *RC*-based power-rail ESD clamp circuit and (b) the proposed power-rail ESD clamp circuit with two diodes in its ESD-transient detection circuit.

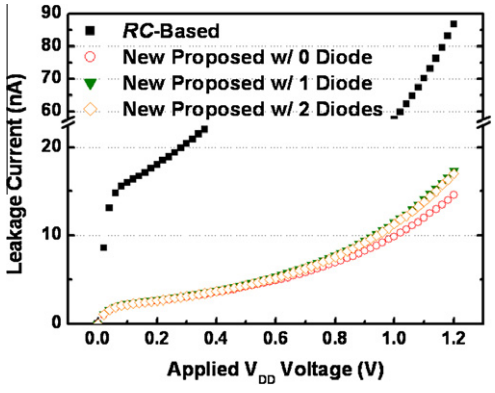

Fig. 7. The measured DC *I*–*V* curves of the traditional *RC*-based and the proposed power-rail ESD clamp circuits at room temperature.

Some previous studies [3,4] had shown that the ESD-transient detection circuits with the *RC*-based design and feedback mechanism were easily mis-triggered into the latch-on state [9] under the fast power-on condition. For the fast power-on condition, a voltage pulse with 1.2 V and 2 ns rise time is applied in this work. As shown in Fig. 9b, the voltage waveforms of the proposed power-rail ESD clamp circuits with one and two diodes are not degraded. The proposed power-rail ESD clamp circuits have high immunity

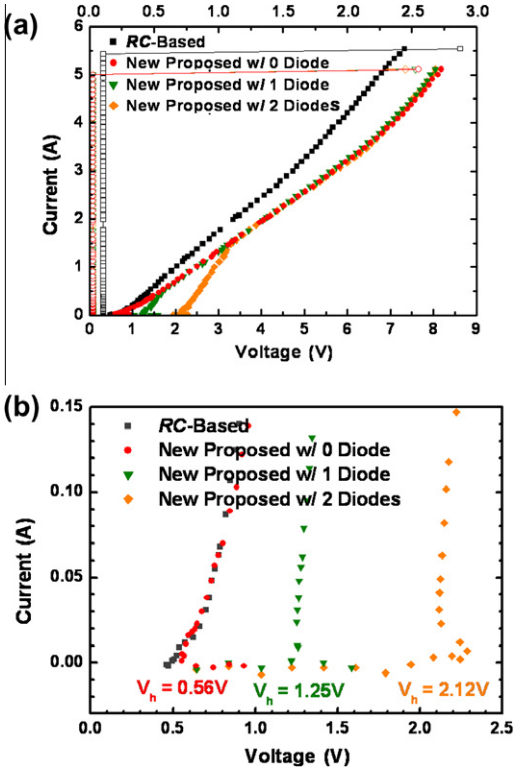

Fig. 8. TLP measured *I–V* curves of (a) the power-rail ESD clamp circuits and (b) the zoomed-in illustration for the holding voltages.

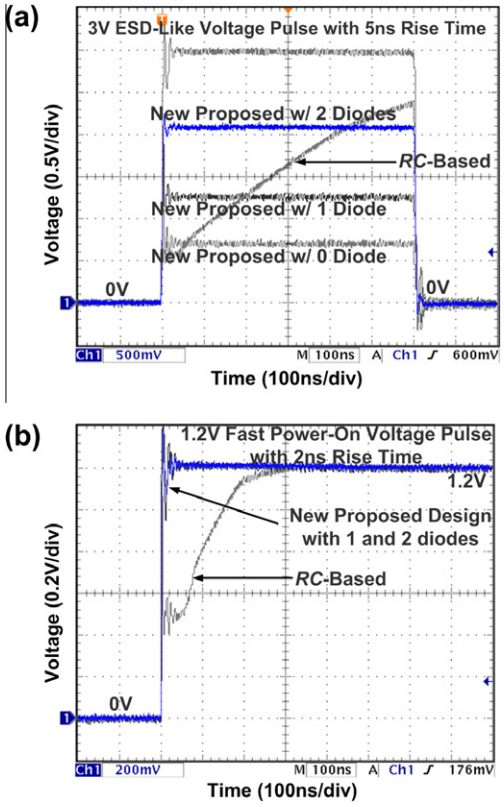

Fig. 9. The voltage waveforms monitored on the power-rail ESD clamp circuits under (a) ESD-transient-like condition and (b) fast power-on condition.

Table 2
The measured results of second breakdown current and ESD levels of four power-rail ESD clamp circuits.

Power-rail ESD clamp circuits	It_2 (A)	HBM level (kV)	MM level (V)
Traditional *RC*-based	5.44	>8	450
New proposed with 0 diode	5.01	>8	350
New proposed with 1 diode	5.01	>8	350
New proposed with 2 diodes	5.01	>8	350

against mis-trigger due to adjustable holding voltage. On the contrary, the *RC*-based power-rail ESD clamp circuit dramatically suffers the mis-trigger, which spends about 300 ns to return back the normal circuit operation voltage level of 1.2 V, as shown in Fig. 9b.

In addition, Fig. 10 is the setup of transient noise measurement for the latch-on concerns. The voltage pulse is applied to the V_{DD} to test the device under test (DUT). The voltage and current waveforms of the DUT during the transient can be monitored by the oscilloscope. The transient noise with 3 V voltage level and a rise time of 5 ns is purposely added to V_{DD} power line with 1.2 V operation voltage. As shown in Fig. 11a–c, the new proposed ESD-transient detection circuit with zero diode is the only circuit to suffer the latch-on issue because its holding voltage is much lower than the 1.2 V operation voltage. However, the holding voltage of the new proposed ESD-transient detection circuit can be adjusted by adding the diodes. Therefore, the ESD-transient detection circuits with positive feedback mechanism and the adjustable holding voltage can be free to latch-on issue. Since the feedback mechanism was not used in the traditional *RC*-based power-rail ESD clamp circuit, the latch-on event was not occurred in such a measurement.

3.4. Transient-induced latch-up (TLU) measurement

The transient-induced latch-up (TLU) measurement has been used to investigate the susceptibility of DUT to the noise transient

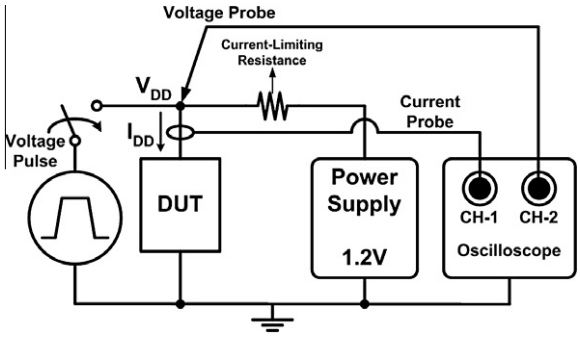

Fig. 10. The setup of transient noise measurement.

or glitch on the power lines under normal circuit operation condition. The TLU measurement setup with bipolar trigger waveform can accurately simulate the practical system-level ESD event [10]. The setup for TLU measurement is shown in Fig. 12 [9,10]. The charging voltage (V_{charge}) has positive ($V_{charge} > 0$) and negative ($V_{charge} < 0$) polarities. The positive (negative) V_{charge} can generate the positive-going (negative-going) bipolar trigger noise into the power pins of the DUT. A 200 pF capacitor is employed as the charging capacitor. The supply voltage of 1.2 V is used as V_{DD} and the noise trigger source is directly connected to DUT through the relay in the measurement setup. The current-limiting resistance of 4.7 Ω is used to avoid electrical overstress (EOS) damage in the DUT under a high-current latch-on state. The voltage and current waveforms of the DUT at V_{DD} node after TLU measurement are monitored by the oscilloscope.

The measured V_{DD} and I_{DD} transient responses of the traditional *RC*-based power-rail ESD clamp circuit under the TLU

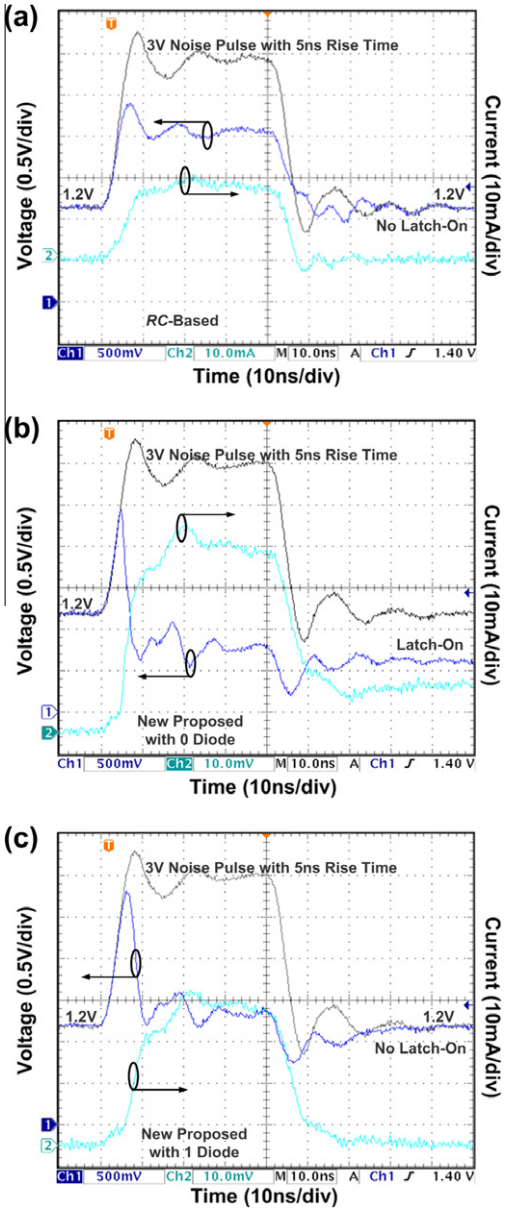

Fig. 11. The measured voltage and current waveforms of power-rail ESD clamp circuit, realized with (a) the traditional *RC*-based ESD-transient detection circuit, (b) the proposed ESD-transient detection circuit with no diode and (c) the proposed ESD-transient detection circuit with one diode, under transient noise condition with 3 V overshooting on 1.2 V V_{DD}.

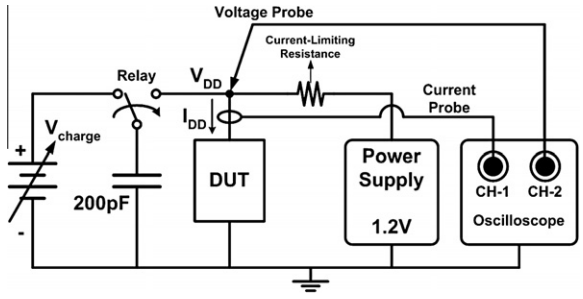

Fig. 12. The setup for transient-induced latch-up (TLU) measurement [9,10].

measurement with V_{charge} of +1 kV and −1 kV are shown in Fig. 13a and b, respectively. In Fig. 13, the latch-on event is not occurred because the feedback mechanism is not used in the *RC*-based

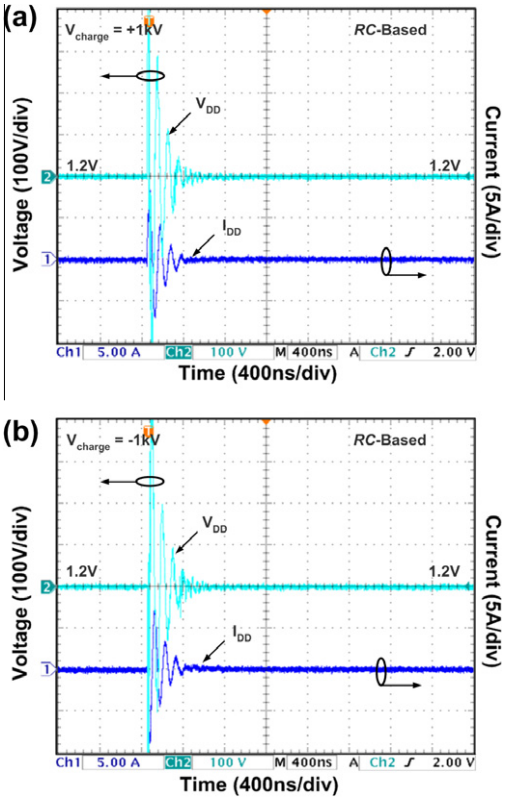

Fig. 13. Measured V_{DD} and I_{DD} waveforms on the traditional *RC*-based power-rail ESD clamp circuit under TLU measurement with V_{charge} of (a) +1 kV and (b) −1 kV.

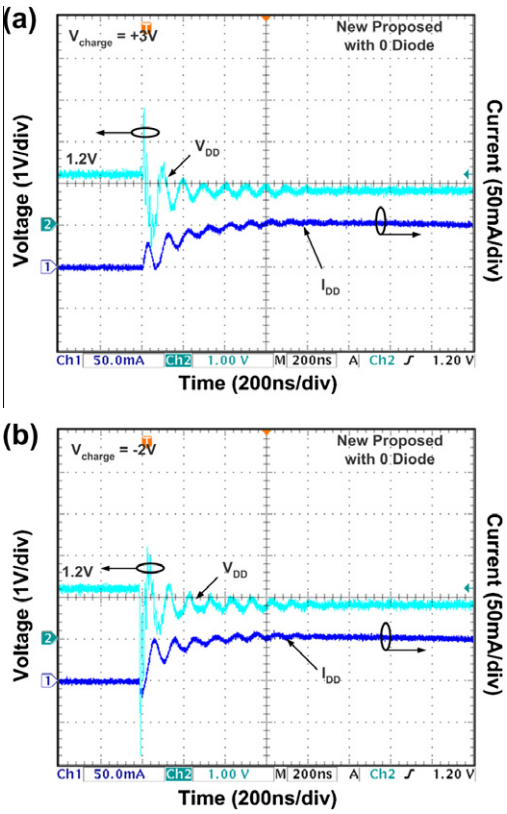

Fig. 14. Measured V_{DD} and I_{DD} waveforms on the new proposed power-rail ESD clamp circuit with no diode under TLU measurement with V_{charge} of (a) +3 V and (b) −2 V.

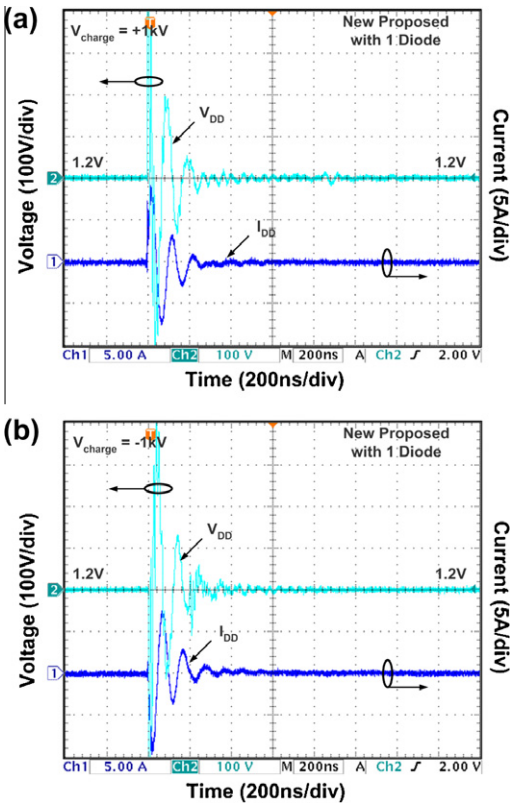

Fig. 15. Measured V_{DD} and I_{DD} waveforms on the new proposed power-rail ESD clamp circuit with one diode under TLU measurement with V_{charge} of (a) +1 kV and (b) −1 kV.

Table 3
The comparison on TLU levels among four power-rail ESD clamp circuits.

Power-rail ESD clamp circuits	Positive TLU level	Negative TLU level
Traditional *RC*-based	Over + 1 kV	Over −1 kV
New proposed with 0 diode	+3 V	−2 V
New proposed with 1 diode	Over + 1 kV	Over −1 kV
New proposed with 2 diodes	Over + 1 kV	Over −1 kV

power-rail ESD clamp circuit. Due to the holding voltage lower than V_{DD}, the new proposed power-rail ESD clamp circuit with zero diode suffered the latch-on issue under TLU measurement for V_{charge} of +3 V and −2 V, as shown in Fig. 14a and b. The measured results of the new proposed power-rail ESD clamp circuits with the diodes under the TLU measurement with V_{charge} of +1 kV and −1 kV are also shown in Fig. 15a and b. In Fig. 15, the new proposed power-rail ESD clamp circuits with adjustable holding voltage can successfully overcome transient-induced latch-on issue. The TLU levels (the minimum V_{charge} to induce the latch-on on V_{DD}) among the four power-rail ESD clamp circuits are listed in Table 3.

4. Conclusion

New power-rail ESD clamp circuit with adjustable holding voltage has been successfully verified in a 65 nm 1.2 V CMOS technology. The proposed ESD-transient detection circuit adopts the capacitance-coupling mechanism to command the ESD clamp PMOS transistor. From the measured results, the proposed design has excellent immunity against mis-trigger and latch-on under the fast power-on condition. The proposed ESD-transient detection circuit is also efficient in layout area and standby leakage, which saves layout area and leakage current by more than 54.5% and 80.4%, respectively, compared with the traditional *RC*-based ESD-transient detection circuit.

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