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High-performance polycrystalline silicon thin-film transistors prepared via the laser crystallization of the prepatterned channel layer on the bottom-gate structure

Chao-Lung Wang *, I-Che Lee, Chun-Yu Wu, Yu-Ting Cheng, Po-Yu Yang, Huang-Chung Cheng

Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan
Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan

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A B S T R A C T

High-performance polycrystalline silicon thin-film transistors (TFTs) using an excimer laser crystallization of the prepatterned channel layer on the bottom-gate (BG) structure were fabricated to exhibit a field-effect mobility as high as 339 cm^2/V s and an on/off current ratio of 9.5×10^7 with respect to 102 cm^2/V s and 1.5×10^7 for the conventional top-gate (TG) TFTs, respectively. Such a superior performance is attributed to the cross-shaped grain boundary structure formed in the channel region owing to the two-dimensional location control of grain boundaries. Moreover, the prepatterned BG TFTs show better device-to-device uniformity than the conventional TG ones due to the manipulated grain boundaries. This technology is thus promising for the future applications of system-on-panel and three-dimension integrated circuits.

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1. Introduction

Low temperature poly-silicon (LTPS) thin film transistors (TFTs) have been extensively studied for the active-matrix-liquid-crystal displays (AMLCDs), active-matrix organic light-emitting displays (AMOLEDs), and three-dimensional integrated circuits (3D-ICs) applications [1,2]. The polycrystalline-Si (poly-Si) thin film transistors fabricated with conventional excimer laser crystallization (ELC) exhibit higher field-effect mobility, typically about 100 cm^2/V s, as compared to that of amorphous-Si (a-Si) TFTs. Therefore, the integration of the peripheral driver circuits and pixel elements on the same glass substrate can be realized [3]. In the early stage of the development of LTPS TFTs, bottom-gate (BG) TFTs have attracted considerable attention because it could be compatible with the process steps of traditional a-Si TFTs. However, the BG TFTs show worse electrical characteristics than the top-gate (TG) TFTs. The field-effect mobility of BG TFTs is generally lower than the TG ones because of the smaller grain size and poor crystallinity due to the BG electrode acting as the heat sink during ELC [4]. Therefore, adopting of TG TFTs in AMLCDs and AMOLEDs has become more popular than the BG ones. Although the ELC TG TFTs can achieve high field-effect mobility, the grain boundary distribution of ELC poly-Si films is non-uniform and randomly distributed. Consequently, ELC TG TFTs have encountered poor device-to-device uniformity, especially as the device dimension is comparable to the grain size and limits its practical applications for small-dimension TFTs in high resolution panels [5,6]. Thus, various technologies aimed at the grain boundary location control, such as the sequential lateral solidification (SLS) [7], grain filters method [8], grains controlled by air gap structure [9], dual-beam with thick oxide portion [10], and grains controlled by local heating system [11,12] have been proposed. However, based on these methods, the positions of the grain boundary can only be controlled one-dimensionally or require complex fabrication processes to enable the two-dimensional (2-D) location control of the grain boundaries.

In this paper, an ELC of the prepatterned channel layer on the BG structure has been adopted to fabricate the poly-Si TFTs. The prepatterned BG TFTs exhibited not only a superior device performance but also a much better device-to-device uniformity than the conventional TG ones owing to location-controlled grain boundaries.

2. Experimental details

Fig. 1 shows the schematic diagram of the key fabrication sequence of laser irradiation on the prepatterned active layer with the BG structure. First, in-situ phosphorus doped poly-Si layer with a thickness of 1000 Å was deposited on an oxidized silicon substrate with a low pressure chemical vapor deposition (LPCVD) system at 550 °C as the BG electrode after definition. Then, a 1000-Å-thick tetraethyl orthosilicate (TEOS) gate oxide and a 1000-Å-thick a-Si thin film were deposited using LPCVD, followed by a 500-Å-thick capping TEOS oxide to prevent the a-Si from the ablation during laser irradiation. Then, the capping oxide and a-Si thin film were sequentially etched as the active region by transformer-coupled plasma reactive ion etching. After standard RCA clean process, the laser crystallization was performed using a KrF excimer laser (λ = 248 nm) in a vacuum

* Corresponding author at: National Chiao Tung University, Lab. ED 309B, Engineering Bldg. 4, No. 1001, Ta-Hsueh Road, Hsinchu 30010, Taiwan. Tel.: +886 3 5712121x54218; fax: +886 3 5738343.
E-mail address: wang711018@yahoo.com.tw (C.-L. Wang).

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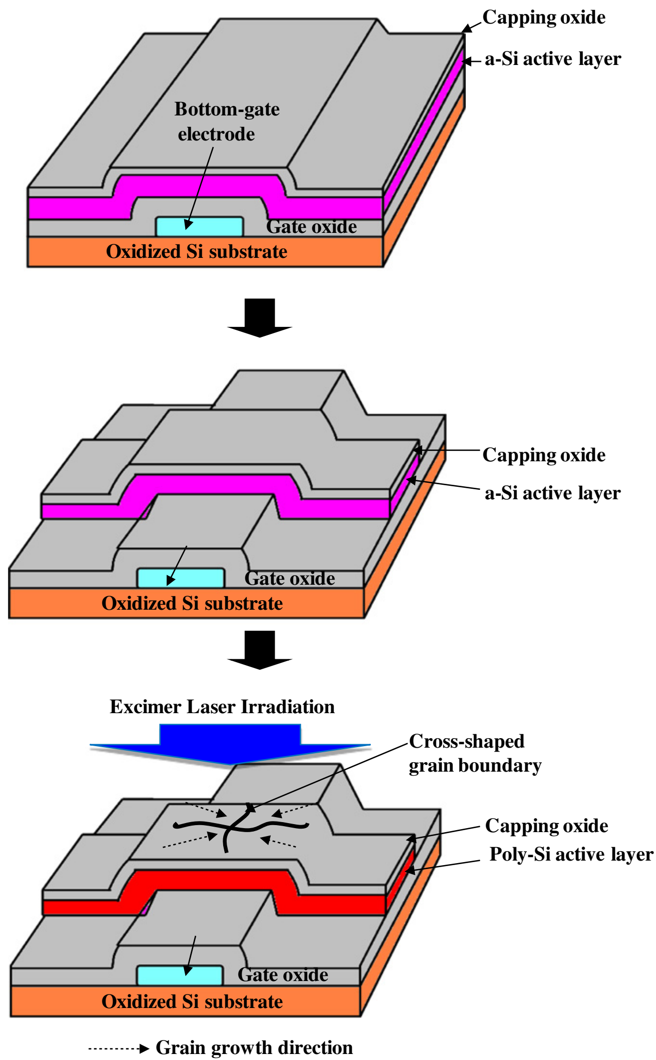

Fig. 1. Schematic diagram of the key processes for the TFTs prepared via the laser crystallization of the prepatterned channel layer on the BG structure.

chamber pumped down to 7.5×10^{-6} Pa at room temperature. The KrF excimer laser had a beam spot size of 23 mm × 1.8 mm and the pulse width of 30 ns. After laser irradiation and capping oxide removal, phosphorus ion implantation with a dose of 5×10^{15} cm^{-2} and an acceleration voltage of 40 keV was carried out to form the source and drain (S/D) regions. Next, a TEOS passivation oxide layer was deposited and the implanted dopants were activated by thermal annealing at 600 °C for 9 h in a furnace with nitrogen ambient. Finally, contact hole opening and metallization were completed to fabricate the prepatterned BG TFTs. No further hydrogenation plasma step was conducted during the device fabrication process. For comparison, conventional ELC TG TFTs with an average grain size of about 350 nm were also fabricated as the reference samples. After the TFTs fabrication, a semiconductor parameter analyzer (4156C, Agilent Technologies) integrated with a probe station was utilized to measure the current–voltage characteristics. After removing the capping oxide with Secco etching, surface micrograph of the crystallized poly-Si thin films was observed by a field-emission scanning electron microscopy (FE-SEM; Hitachi S-4700I; operating voltage: 15 kV). An atomic force microscopy (AFM; Digital Instrument D3100) operated in the tapping mode with silicon probe of 10 nm tip radius is utilized to analyze the surface structure of the prepatterned channel layer after removing the capping oxide and exposed gate oxide. The transmission electron microscopy (TEM; JEOL JEM-2000FX; operating voltage: 200 kV) was also adopted to analyze the cross-sectional device structures and the grain structure of the poly-Si films.

3. Results and discussion

Fig. 2(a)–(c) shows the SEM images of the Secco-etched poly-Si thin films with the BG structure after the excimer laser crystallization and capping oxide removal for the gate length of 1.0, 1.2, and 2.0 μm, accordingly. The constant laser energy density of 320 mJ/cm^2 and shot numbers of 20 are adopted. It can be observed that four grains are formed in the channel region via the super lateral growth (SLG) and the cross-shaped grain boundary is therefore produced as the gate length is shorter than 1.2 μm. In contrast, for the case of the gate length of 2.0 μm, the spontaneous nucleation is observed in the channel region owing to the supercooling of the complete-melting

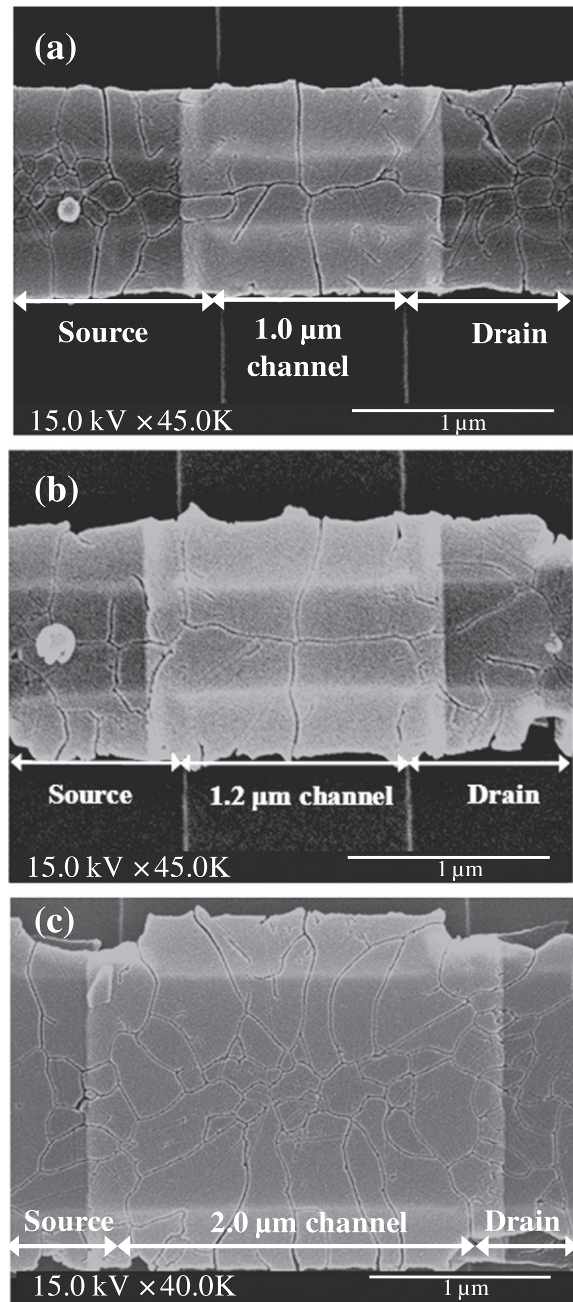

Fig. 2. SEM images of excimer-laser-crystallized poly-Si thin films with BG structure after Secco etching, in which the channel length is (a) 1.0 μm, (b) 1.2 μm, and (c) 2.0 μm, respectively.

silicon before the grain growths impinge in the middle of the channel region. Therefore, small grains are caused by the spontaneous nucleation in the area of the channel region. As a result, by adopting a moderate gate length, like 1.0 or 1.2 μm, the cross-shaped grain boundary structures can be formed in the channel region.

The dependence of the silicon grain structures on applied laser shot number is also investigated. Fig. 3(a) and (b) shows the Secco-etched SEM images of the prepatterned channel layer with the BG structure after laser irradiation shot of 1 and 20 times, correspondingly, for the gate length of 1 μm. The cross-shaped grain boundary structures are produced in the channel region for both cases. The result indicates that the 2-D location-controlled grain boundary can be achieved only by a single shot of the ELC. The multiple shots of the laser pulse cannot change the cross-shaped grain boundary structure in the channel region. However, the high density of intragrain defects formed under a single laser shot can be significantly reduced by multiple laser irradiations. Therefore, the 20 shots of laser pulse are adopted in this work to improve the crystallinity of the grain and device performance.

Fig. 4 displays the cross-sectional TEM image to analyze the microstructure of the prepatterned BG TFT. The TEM sample is prepared using focused-ion-beam technology. The beam voltage and beam current used during the potentially damaging steps of etching process are 30 kV and 100 pA, respectively. As shown in Fig. 4, it is observed that a single grain boundary perpendicular to the channel direction via the SLG phenomenon of the laser irradiation [13]. The electron diffraction image indicates that the silicon grain exhibits [110]-orientated with relation to the normal direction of the paper and the high crystallinity within the silicon grain due to the clear dot pattern.

Fig. 5(a) and (b) displays the cross-sectional surface roughness analysis of AFM images of the prepatterned channel layer with the BG structure before laser irradiation and after laser irradiation, respectively. The white dashed line Y–Y′ indicates the direction of the cross-sectional analysis, as shown in the insets of the AFM images. It can be clearly observed that the edge of the prepatterned channel layer becomes thinner than the center along the Y–Y′ direction after the laser irradiation. The result is attributed to the shrinkage of the prepatterned channel owing to surface tension effect during laser irradiation [9]. Since the heat capacity of the thinner melting Si is smaller than the thicker one after the laser irradiation, the edge of the channel will store the heat for a shorter time than the center of the channel. As a result, the edge of the channel will induce the temperature gradient from the center of the channel toward the edge and solidify at first.

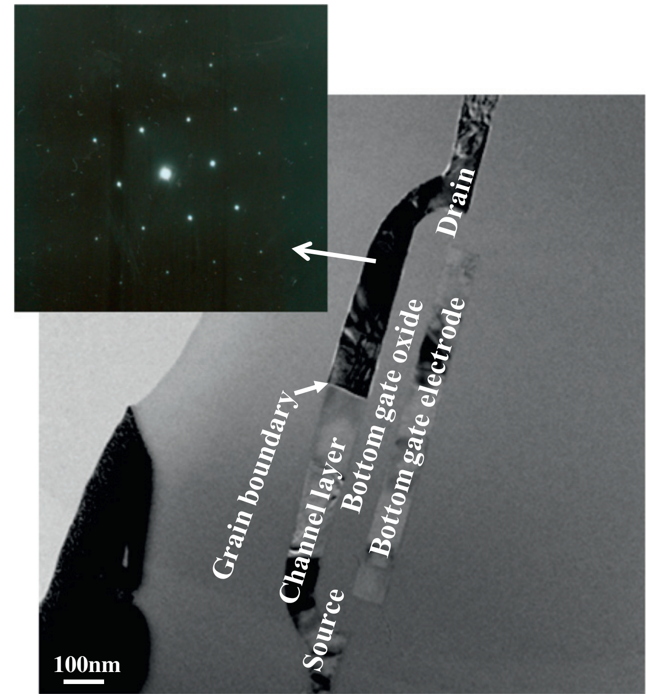

Fig. 4. Cross-sectional TEM image and the diffraction pattern of excimer-laser-crystallized poly-Si films with BG structure.

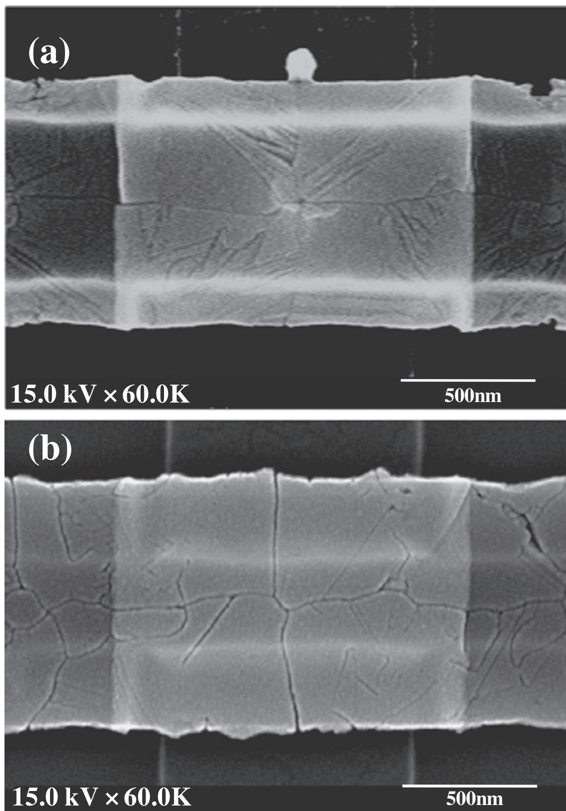

Fig. 3. SEM images of excimer laser crystallized poly-Si thin films with BG structure after Secco etching, in which the channel length is 1 μm, and the laser shot number is (a) 1 shot and (b) 20 shots, respectively.

Fig. 6 shows the schematic illustration of the mechanism of the proposed crystallization method that causes 2-D location-controlled grain boundary. When the excimer laser irradiates on the prepatterned active layer, the laser energy density is controlled to melt the thin channel region completely. Since the laser energy density is almost uniform in the local region, the thick region of a-Si film near the edges of the BG structure will be only partially melted and the X–X′ directional temperature gradient is created. Therefore, the grain growths from the solid portions toward the melted region, resulting in one grain boundary perpendicular to the channel direction in the middle of the channel region [11]. At the same time, the Y–Y′ directional temperature gradient is also produced on the prepatterned active layer, as mentioned above in Fig. 5. Therefore, the lateral thermal gradient along the Y–Y′ axis occurs and the cooling rate of the edge region of the channel layer is faster than the central region. The Y–Y′ directional thermal gradient can lead to the grain growths from the edge of the channel toward the center so that a single grain boundary parallel to the channel direction is formed. Consequently, the grain boundary location is well-controlled two-dimensionally owing to the spatial thermal gradient distribution in the channel region.

Typical transfer characteristics of the prepatterned BG and conventional TG TFTs with W = L = 1 μm are compared in Fig. 7(a). The field-effect mobility and subthreshold swing are evaluated from the linear region at $V_{ds} = 0.1$ V, and the on/off current ratio is defined at $V_{ds} = 1$ V. It is clearly evident that the prepatterned BG TFTs exhibited obvious improvement in the device characteristics than

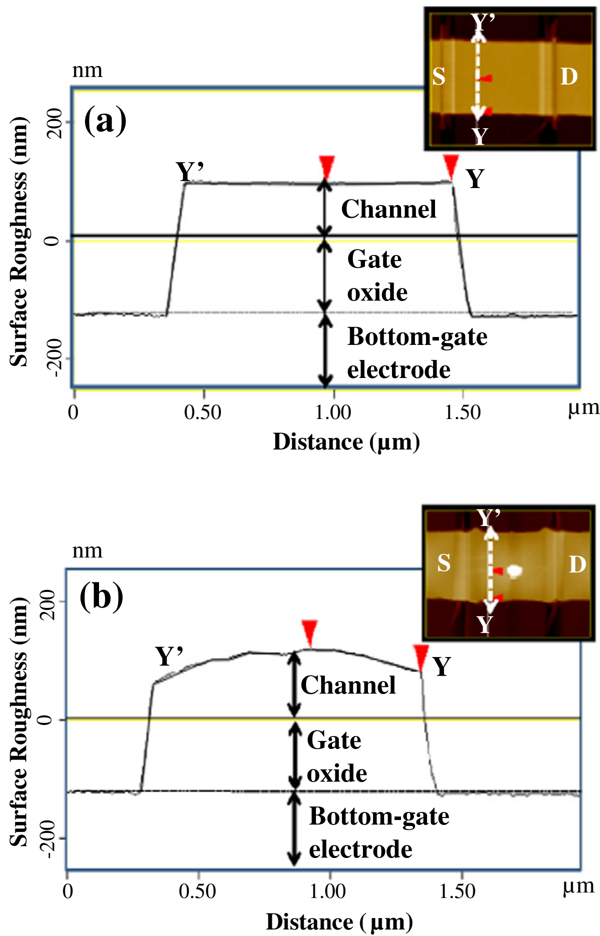

Fig. 5. Cross-sectional surface roughness analysis of AFM images and the inset are the corresponding AFM images of the prepatterned channel layer with BG structure (a) before and (b) after laser irradiation.

the conventional TG ones. The prepatterned BG TFTs show a superior field-effect mobility of 339 cm^2/V s, a low subthreshold swing of 0.354 V/dec, and a high on/off current ratio of 9.5×10^7 whereas the conventional ones show 102 cm^2/V s, 0.722 V/dec and 1.5×10^7,respectively. It is well known that the grain boundary acts a trapping

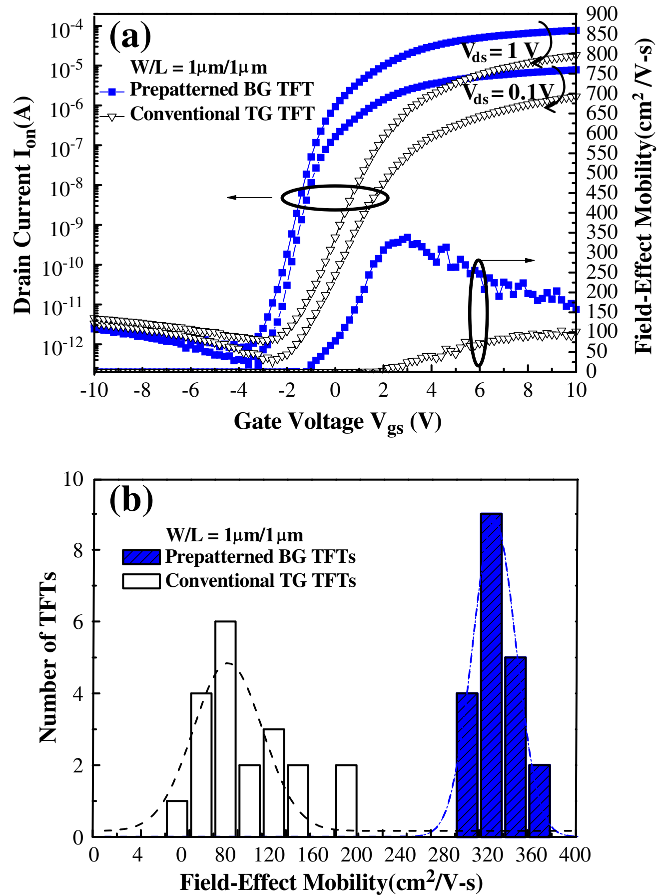

Fig. 7. (a) Typical transfer characteristics and (b) measured field-effect mobility distributions of the prepatterned BG and conventional TG TFTs for W = L = 1 μm.

center and degrades the device electric characteristics. The better performance of the prepatterned BG TFT is attributed to the presence of only one perpendicular and one parallel grain boundary along the channel direction. To investigate the uniformities of the prepatterned BG and the conventional TG TFTs, twenty TFTs are measured for each. Fig. 7(b) displays the field-effect mobility distributions of these two different TFTs for W = L = 1 μm. The prepatterned BG TFTs exhibit a

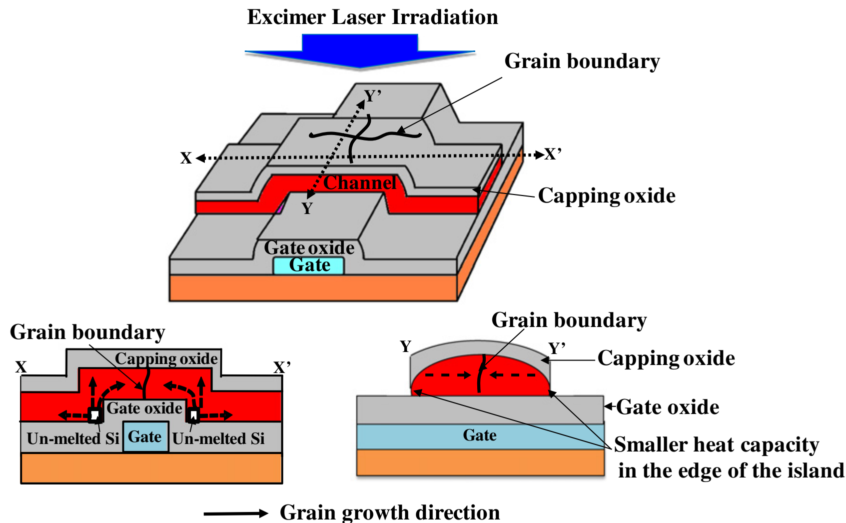

Fig. 6. Illustration of the mechanism of the excimer laser crystallization of the prepatterned channel on the BG structure.

relatively smaller deviation in field-effect mobility (from 302 to 368 cm^2/V s) than the conventional TG ones (71 to 213 cm^2/V s). The superior device-to-device uniformity of the prepatterned BG TFTs as compared to the conventional TG ones can be ascribed to the much smaller deviation of the grain boundaries inside the channel region owing to the 2-D location-controlled grain boundary structure.

4. Conclusions

The 2-D grain boundary location-controlled method via excimer laser crystallization of the prepatterned channel layer on a BG structure has been proposed to accomplish the channel regions with the cross-shaped grain boundary structure. Consequently, the prepatterned BG TFTs could attain a higher field-effect mobility of 339 cm^2/V s as compared with 102 cm^2/V s for the conventional TG ones. Uniform device characteristics of the prepatterned BG TFTs were also demonstrated owing to the artificially controlled grain boundaries. It depicts that the proposed method is suitable for the system-on-panel and 3D-IC applications.

Acknowledgments

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References

[1] Y.I. Park, T.J. Ahn, S.K. Kim, J.Y. Park, J.S. Yoo, C.Y. Kim, C.D. Kim, in: SID Tech. Digest, 2003, p. 487.
[2] J.H. Park, P. Krishna, K.C. Saraswat, Hailin Peng, Appl. Phys. Lett. 91 (2006) 143107.
[3] M.H. Lee, S.L. Wu, M.J. Yang, K.J. Chen, G.L. Luo, L.S. Lee, M.J. Kao, IEEE Electron Device Lett. 31 (2010) 824.
[4] Y. Mishima, K. Yoshino, M. Takei, N. Sasaki, IEEE Trans. Electron Devices 48 (2001) 1087.
[5] P.C. Yang, P.S. Kuo, S.C. Lee, IEEE Trans. Electron Devices 55 (2008) 2129.
[6] G.K. Giust, T.W. Sigmon, IEEE Electron Device Lett. 18 (1997) 296.
[7] M.A. Crowder, A.T. Voutsas, S.R. Droes, M. Moriguchi, Y. Mitani, IEEE Trans. Electron Devices 51 (2004) 560.
[8] R. Vikas, R. Ishihara, Y. Hiroshima, D. Abe, S. Inoue, T. Shimoda, W. Metsalaar, K. Beenakker, Jpn. J. Appl. Phys. 45 (2006) 4340.
[9] I.H. Song, S.H. Kang, W.J. Nam, M.K. Han, IEEE Electron Device Lett. 24 (2003) 580.
[10] R. Ishihara, P.Ch.V.D. Wilt, B.D.V. Dijk, A. Burtsev, J.W. Metselaar, C.I.M. Beenakker, Thin Solid Films 427 (2003) 77.
[11] A. Asano, U.S. Patent 0290200 (2007).
[12] H. Jiroku, M. Miyasaka, H. Tokioka, and T. Ogawa, U.S. Patent 6602765 (2003).
[13] C.C. Tsai, Y.J. Lee, J.L. Wang, K.F. Wang, I.C. Lee, C.C. Chen, H.C. Cheng, Solid State Electron. 52 (2008) 365.