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FOWLER–NORDHEIM LIMITED BAND-TO-BAND TUNNELING (FNBB) FOR *p*-MOSFET GATE CURRENT IN A FLOATING BULK CONDITION

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Abstract—A new mechanism of Fowler–Nordheim tunneling limited band-to-band tunneling (FNBB) has been identified to be responsible for the gate current measured from *p*-MOSFETs with the bulk (*n*-well) floated. This mechanism has been found to occur in the gate-to-drain overlap region. Two-dimensional device simulations have successfully reproduced this gate current and thus the physical parameter values of the band-to-band tunneling model have been obtained.

1. INTRODUCTION

A new drain leakage current in off-state MOSFETs due to band-to-band tunneling in the gate-to-drain overlap region has recently been investigated extensively[1–3]. In the work of[1–3], an analytical model for calculating the band-to-band tunneling current $I_{B\text{-}B}$, i.e. $I_{B\text{-}B} = \alpha_1 E_{si} \exp(-\alpha_2/E_{si})$ where α_1 and α_2 are two fitting parameters and E_{si} is the effective surface electric field, has been introduced. The parameter values in this expression have been reported to be extracted from the samples with the bulk grounded[1–3]. In this letter we present, for the first time, a new way for extracting the physical parameter values of the band-to-band tunneling model by reproducing the gate current of *p*-MOSFET devices measured in a floating bulk condition. We also present a new mechanism of Fowler–Nordheim (F–N) tunneling limited band-to-band tunneling, which has been found to occur in the gate-to-drain overlap region, to explain such gate current.

2. EXPERIMENTAL RESULTS

The devices were fabricated by 0.6 μm twin-well polysilicon CMOS process. The starting material was *p*-type ⟨100⟩ oriented Si wafers with resistivity of 8–12 Ω-cm. Phosphorus (6.0×10^{12} cm^{-2}, 150 keV) was implanted to form the *n*-well region. BF_2 (2.6×10^{12} cm^{-2}, 70 keV) was used as the threshold voltage implant. The gate oxide was grown in dry O_2 at 920°C to a thickness of 146 Å. After n^+ gate polysilicon was formed, BF_2 (10^{13} cm^{-2}, 45° angle rotating, 50 keV) was implanted to form the low-doped drain region. After the sidewall spacer TEOS (3000 Å) was formed, BF_2 (3×10^{15} cm^{-2}, 70 keV) was implanted to form the highly-doped drain region. The doping concentration near the corner has a peak value of about 3.0×10^{18} cm^{-3}. The devices used in this study have two different gate lengths of 1.0 and 20 μm each with the same gate width of 20 μm.

With the grounded drain, the devices have been characterized by making the source and the *n*-well both floated. The corresponding measured gate *I–V* characteristics at 27°C are shown in Fig. 1 for positive gate voltage $+V_G$ and for negative gate voltage $-V_G$. The $+V_G$ data at 75°C for 1.0 μm gate length are also presented in Fig. 1. From Fig. 1 we can observe that the measured gate current at $-V_G$ for gate length of 20 μm is greater than that of 1.0 μm by a factor of about 20, indicating the uniform distribution of the F–N tunneling current densities across the overall gate area. To account for the results measured at $+V_G$ as shown in Fig. 1, one must first consider the possible origins of the electrons generated in silicon. From Fig. 1 it can be clearly observed that at 27°C the thermal generation-limited F–N tunneling mechanism dominates the gate current in the positive gate voltage range of about between 12–17 V. This mechanism can be identified by noting from Fig. 1 that the corresponding gate current increases as the temperature increases from 27 to 75°C. However, thermal generation cannot create sufficient electrons and thus cannot account for a great change of about four orders of magnitude in the measured gate current when the positive gate voltage increases from 17 to 25 V. We attribute the band-to-band tunneling in the gate-to-drain overlap region to the origin of the electrons generated in silicon, some of which are drawn away via F–N tunneling to the gate. Figure 2 schematically shows the energy band diagram in the gate-to-drain overlap region for demonstrating this mechanism.

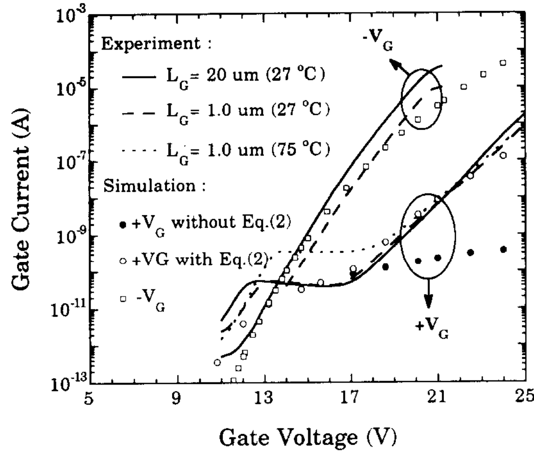

Fig. 1. The measured gate I–V characteristics at 27°C for positive and negative gate voltages with the gate length L_G as a parameter. The simulation results for $L_G = 1.0\,\mu$m are presented for $+V_G$ with and without including (2) as well as for $-V_G$. The experimental data at $+V_G$ for 75°C are also demonstrated.

This mechanism can be judged by observing some experimental data at $+V_G$: (i) the gate current slightly increases with increasing the temperature for 1.0 μm gate length, as demonstrated in Fig. 1 for $V_G > 19$ V; and (ii) the gate current is almost independent of the gate length, as also demonstrated in Fig. 1. Therefore, the band-to-band tunneling is responsible for the electrons available to the F–N tunneling. Such interpretation has been proved to be valid by the following two-dimensional device simulations.

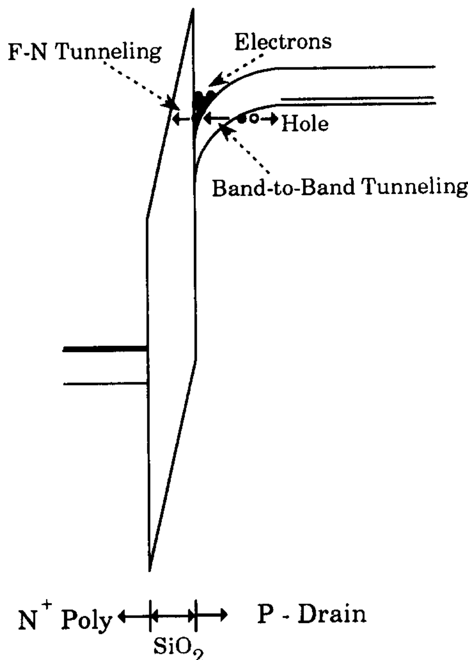

Fig. 2. The energy band diagram in the gate-to-drain overlap region for schematically demonstrating the FNBB mechanism.

3. SIMULATION AND DISCUSSION

Two-dimensional device simulations by utilizing the program MEDICI[4] have been performed to model the measured gate currents at $+V_G$ and $-V_G$. In this program both the band-to-band tunneling and the F–N tunneling have been taken into account in a self-consistent manner. A physical model for Fowler–Nordheim tunneling has been included in the continuity equation for the surface beneath the gate [5]:

$$J_G = \alpha E_{ox}^2 \exp(-\beta/E_{ox}), \tag{1}$$

where E_{ox} is the oxide field strength. The parameter values of $\alpha = 2.3 \times 10^{-6}$ A/V^2 and $\beta = 238.5$ MV/cm as cited in [6] have been used here. A generation rate G_{BB} for band-to-band tunneling has been included in the continuity equation for silicon bulk[7]:

$$G_{BB} = A_{BB}(E_{si}^2/E_g^{1/2}) \exp(-B_{BB} E_g^{3/2}/E_{si}), \tag{2}$$

where E_{si} is the electric field in the silicon, E_g (= 1.12 eV) is the silicon energy band-gap, and A_{BB} and B_{BB} are two parameters to be determined. Based on two-dimensional device simulations, the parameter values of $A_{BB} = 3.5 \times 10^{15}$ eV$^{1/2}$/cm-s-V^2 and $B_{BB} = 17$ MV/cm-eV$^{3/2}$ have been obtained after successfully reproducing the measured gate current at $+V_G$. The corresponding simulated gate currents as function of gate voltage for both $+V_G$ and $-V_G$ are shown in Fig. 1. From Fig. 1 we can observe that such simulation results agree closely with the experimental data not only for the positive gate voltage case but also for the negative gate voltage case. Note that the parameter value of $B_{BB} = 17$ MV/cm-eV$^{3/2}$ in our work agrees reasonably with the associated parameter values reported in [1–3]. Therefore, we can conclude that the measured gate current is dominated by the thermal generation-limited F–N tunneling mechanism over the range of 12 V < V_G < 17 V while for $V_G > 17$ V the mechanism of F–N tunneling limited band-to-band tunneling (FNBB) as proposed above dominates. This can further be identified by performing one additional simulation work by not including the band-to-band tunneling generation rate (2). The corresponding simulation results for $+V_G$ are shown in Fig. 1, which have yielded the gate current dominated by only the thermal generation-limited mechanism.

To determine the region where the FNBB mechanism occurs, it is necessary to observe the current density distribution along the oxide-silicon interface. The simulated surface current density distribution for 1.0 μm gate length with gate voltage as a parameter is shown in Fig. 3. From Fig. 3 we can observe that a peak in the current density appears locally in the gate-to-drain overlap region. It can also be noted from Fig. 3 that irrespective of the gate voltage applied, such region has the same range of about 0.2 μm for the significant FNBB mechanism occuring. Moreover, we have found that not only

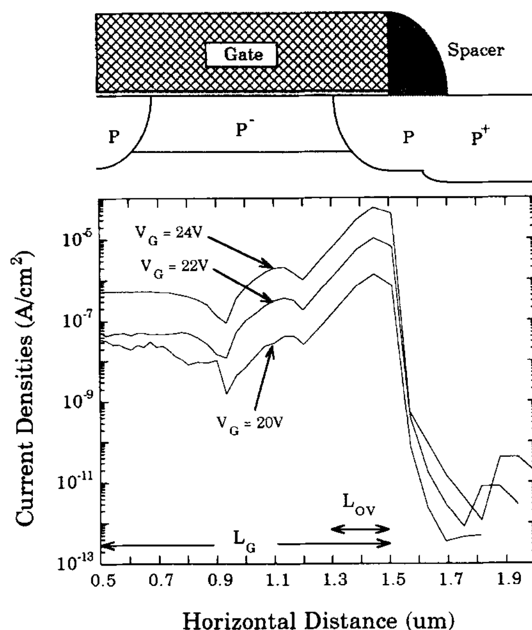

Fig. 3. The simulated current density distributions along the oxide–silicon interface for positive gate voltages of 20, 22 and 24 V. The label L_{OV} represents the estimated range of the gate-to-drain overlap region where the FNBB mechanism occurs dominantly.

this range of about 0.2 μm but also the simulated gate current almost do not change as the gate length increases. This simulation work can thus explain satisfactorily the observed weak dependence of gate current on gate length at $+V_G$ as shown in Fig. 1.

4. CONCLUSION

For the gate currents measured from p-MOSFETs with the bulk (n-well) and the source both floated, a new mechanism of F–N tunneling limited band-to-band tunneling (FNBB) has been judged to be responsible for the observed results at high positive gate voltage. The proposed mechanism has been confirmed by the 2D device simulations. Also the gate-to-drain overlap region in which this mechanism occurs has been determined.

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