A Low Quiescent Current Asynchronous Digital-LDO With PLL-Modulated Fast-DVS Power Management in 40 nm SoC for MIPS Performance Improvement

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***Abstract*—A low quiescent current asynchronous digital-LDO (D-LDO) regulator integrated with a phase-locked loop (PLL)-modulated switching regulator (SWR) that achieves the near-optimum power management supply for core processor in system-on-chip (SoC). The parallel connection of the asynchronous D-LDO regulator and the ripple-based control SWR can accomplish fast-DVS (F-DVS) operation as well as high power conversion efficiency. The asynchronous D-LDO regulator controlled by bidirectional asynchronous wave pipeline realizes the F-DVS operation, which guarantees high million instructions per second (MIPS) performance of the core processor under distinct tasks. The use of a ripple-based control SWR operating with a leading phase amplifier ensures fast response and stable operation without the need for large equivalent-series-resistance, thus reducing the output voltage ripple for the enhancement of supply quality. The fabricated chip occupies 1.04 mm^2 in 40 nm CMOS technology. Experimental results show that a 94% peak efficiency with a voltage tracking speed of 7.5 $\mathrm{V}/\mu\mathrm{s}$ as well as the improved MIPS performance by 5.6 times was achieved.**

***Index Terms*—Asynchronous digital-LDO regulator, bidirectional asynchronous wave pipeline, dynamic voltage scaling, hybrid operation, million instructions per second performance, power conversion efficiency, power module, ripple-based control, switching regulator.**

I. Introduction

SYSTEM-ON-A-CHIP (SoC) is the design trend in currently available integrated circuits. Multiple operation functions, which are achieved by using both analog and digital circuits, can be combined into a single chip to minimize the printed circuit board area as well as the total volume of portable devices. Power modules, which are demanded to provide high-quality supply voltages and to have high power conversion efficiency, are integrated to properly manage the supply voltages for sub-circuits, thus strengthening SoC performance [1]–[4]. As shown in Fig. 1, the system core processor is supplied by an integrated power module, which might be realized by using inductor-based switching regulators (SWRs) and/or low-dropout (LDO) regulators. To reduce power consumption and to improve core processor performance with distinct tasks, the function of a phase-locked loop (PLL) is implemented to adjust the supply voltage V_{SUP} dynamically and to provide the appropriate operation frequencies F_{CK} as requested by the core processor [5]. Frequency F_{CK} is indicated by the dynamic voltage scaling (DVS) commander, which sends the signal N_{DV} and the reference frequency F_{REF} to the PLL. The F_{CK} is rapidly changed to achieve the dynamic frequency scaling (DFS) operation so that the requirement of distinct tasks in the core processor would be met [6]–[8]. The DVS operation is activated by the indicative voltage V_{FLY} which helps obtain a near-optimum V_{SUP} voltage level [9]–[11]. Moreover, the PLL helps smoothly adjust the V_{SUP} with a determined F_{CK} for the core processor to minimize the effect of process, voltage, and temperature (PVT) variations.

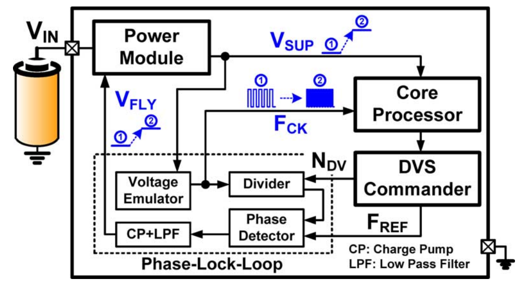

Fig. 1. Integrated power module with a PLL-modulated closed-loop operation for both DVS and DFS operations in SoC.

Million instructions per second (MIPS) is an appropriate indicator or evaluator for core processor performance [12], [13]. Operation frequency, which determines the execution speed of instructions, is the key factor in MIPS performance. Thus, DFS operation is utilized to meet the expected MIPS with distinct tasks in core processor. However, DVS operation should also be activated for the proper adjustment of supply voltage. The

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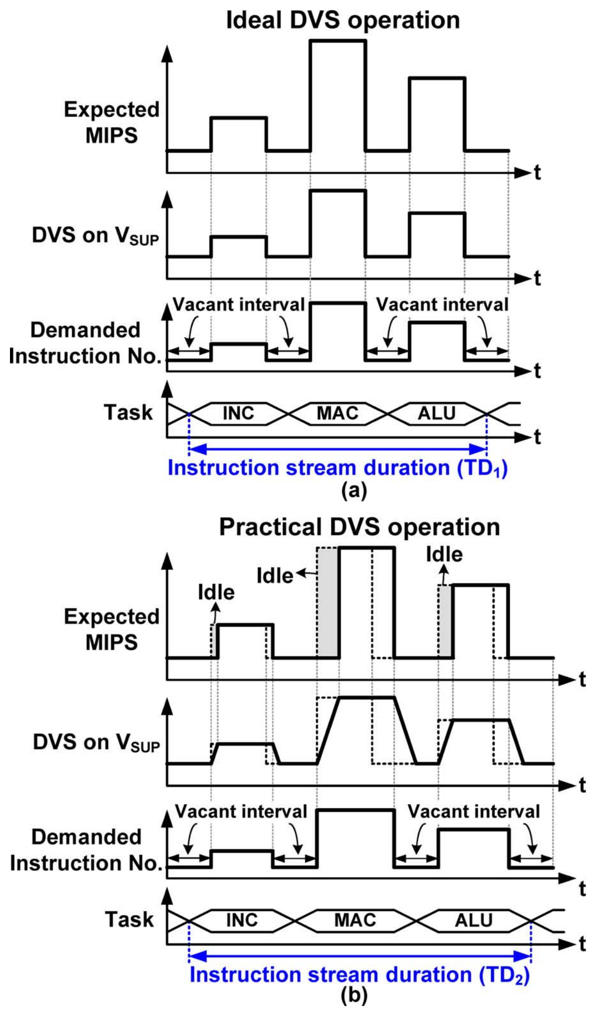

Fig. 2. MIPS illustration of different tasks in core processor under (a) ideal DVS operation and (b) practical DVS operation.

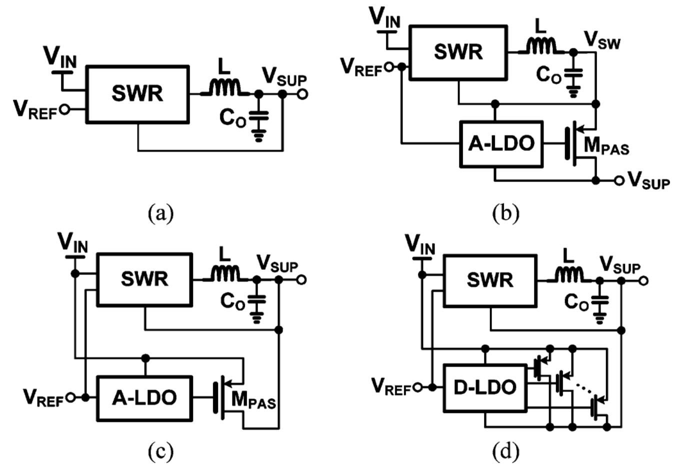

Fig. 3. Topologies of integrated power modules. (a) Simple SWR. (b) SWR in series with an A-LDO regulator. (c) SWR in parallel with an A-LDO regulator. (d) SWR in parallel with a D-LDO regulator.

near-optimum supply voltage helps minimize the propagation delay to guarantee fast operation frequency in high MIPS conditions and reduce needless power loss to realize power-efficient operation in low MIPS conditions. As shown in Fig. 2(a), which illustrates an ideal DVS operation, supply voltage V_{SUP} can be immediately changed to the different voltage levels. The number of demanded instructions varies according to the distinct tasks executing in core processor. Vacant intervals are observed between each peak instructions, which can be considered the operated buffer stage. Satisfactory supply voltages ensure that the varying MIPS performances will correctly correspond to the demanded numbers of instructions. Therefore, the V_{SUP} has to be rapidly adjusted to guarantee proper task operations.

The voltage tracking period is derived in practical DVS operation as shown in Fig. 2(b). The expected MIPS performance can be achieved by using adequate supply voltage V_{SUP}. An idle stage, which is utilized to block the execution in core processor, is inserted until the V_{SUP} reaches its target value in the voltage tracking period. The insertion of an idle stage prevents the operations with incorrect tasks but delays the instruction stream duration of sequential tacks. Thus, practical DVS operation derives longer instruction stream duration, T_{D2}, compared with that of T_{D1} which is performed with the ideal DVS operation. Voltage tracking speed on the V_{SUP} has a significant effect on both the MIPS performance and the instruction stream duration when core processor sequentially executes distinct tasks. As a result, the fast-DVS (F-DVS) operation needs to be achieved in an integrated power module to guarantee the performance of core processor as well as that of the SoC system.

Topologies of integrated power modules are shown in Fig. 3. Fig. 3(a)–(c) show the commonly used power modules. The SWR with a step-down function [14]–[16] shown in Fig. 3(a) has high power conversion efficiency but has limited voltage tracking speed due to its utilization of an inductor. The tracking speed is generally near tens of mV per micro-second, which is far from the demanded DVS performance in an integrated power module. Fig. 3(b) shows the power module achieved by the SWR with a cascaded analog-LDO (A-LDO) regulator [17]. The A-LDO regulator helps filter the switching noise from the SWR to generate a ripple-free output supply voltage for the noise-sensitive analog circuits in SoC. The A-LDO regulator has fast response because the bandwidth of LDO regulator is larger than that of the SWR. Nevertheless, the voltage tracking speed of this cascade structure is affected by the dropout voltage between V_{SW} and V_{SUP}. If a large dropout voltage exists at the cascaded A-LDO regulator, a fast response is achieved at the expense of efficiency. Trade-off exists between power efficiency and voltage tracking speed. The tracking speed of the cascade topology can reach up to hundreds of mV per micro-second, which is still below the demand of F-DVS operation. In addition, the SWR can operate in parallel with an A-LDO regulator [18], [19] as illustrated in Fig. 3(c). The parallel combination aims to realize hybrid operation for both high efficiency and F-DVS operation. The SWR operates with an inductor-based structure to provide energy for high efficiency operation, whereas A-LDO regulator achieves fast voltage tracking because of its large bandwidth. During the transient period, the A-LDO regulator can rapidly generate the supplementary current for F-DVS operations. In steady-state, all the supply currents are delivered by the SWR with a shutdown function to the A-LDO regulator to reduce power consumption. However, the

TABLE I
PERFORMANCE COMPARISONS OF POWER MODULES

Topology (Fig. 3)	(a) SWR	(b) SWR+A-LDO (Cascade)		(c) SWR+A-LDO (Parallel)	(d) SWR+D-LDO (Parallel)
Control Methodology	Linear loop	Linear loop		Linear loop	Linear loop, digital control shift register
Output Ripple	Medium	Small		Medium	Medium
Loading Capability	Large	Medium		Large	Large
DVS Speed	Slow	Slow	Medium	Medium	Fast
Efficiency	High	Medium	Low	High	High

tracking speed is still limited by the bandwidth of the A-LDO regulator, which has a tracking rate of hundreds of mV per micro-second. This value is far from the expected rate of thousands of mV per micro-second.

To enhance the voltage tracking speed significantly, digital-LDO (D-LDO) regulator is a suitable candidate for the integrated power module. Fig. 3(d) shows the hybrid operation achieved by the SWR in parallel with a D-LDO regulator [20]. Given that a D-LDO regulator has fast voltage tracking speed, the F-DVS operation is properly realized. The integrated power module proposed in this paper adopts this parallel structure to achieve both high efficiency and F-DVS operation. This proposed integrated power module contains a ripple-based control SWR and an asynchronous D-LDO regulator. Moreover, the asynchronous D-LDO regulator is controlled by the bidirectional asynchronous wave pipeline (BAWP), which can further improve tracking speed and can achieve a minimized static current consumption of 50 nA. Performance comparisons of these different integrated power modules are listed in Table I.

This paper is organized as follows. The PLL-modulated power module with an asynchronous D-LDO regulator and a ripple-based control SWR for hybrid operation is presented in Section II. An asynchronous D-LDO regulator structure with BAWP control is described in Section III. The ripple-based control SWR is illustrated in Section IV. Experimental results are shown in Section V. Finally, conclusions are made in Section VI.

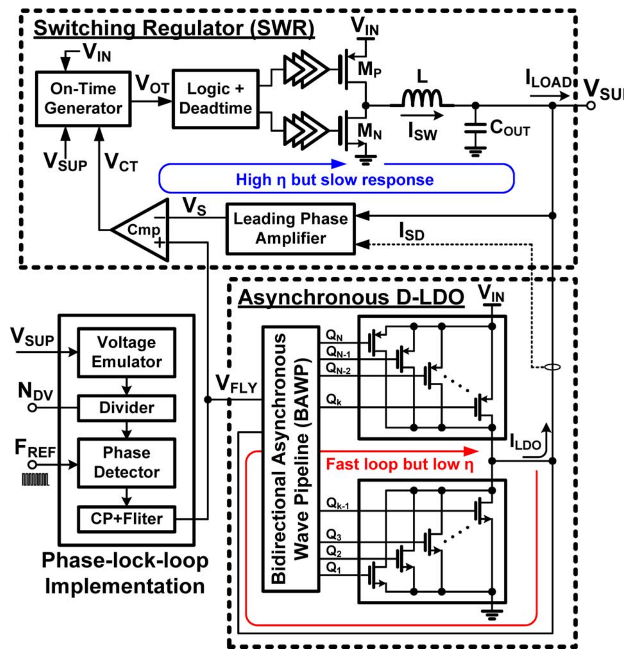

Fig. 4. Structure of the proposed PLL-modulated power module for the hybrid operation.

II. PLL-MODULATED POWER MODULE WITH THE HYBRID OPERATION

Structure of the proposed PLL-modulated power module is shown in Fig. 4. The PLL implementation helps activate the F-DVS operation to obtain a near-optimum voltage level at V_{SUP} for the core processor [5]. The proposed power module achieves hybrid operation through a parallel connection of the ripple-based control SWR and the asynchronous D-LDO regulator. The PLL implementation generates the indicative voltage V_{FLY}, which is the reference voltage for both SWR and D-LDO regulator.

The proposed SWR is operated with ripple-based control [21]–[24]. The output voltage is sent to the leading phase amplifier (LPA) to generate the sensing signal V_S. The V_S is then compared with the V_{FLY} in terms of enabling the on-time generator to produce the control duty cycles for power switches, M_P and M_N. This comparator-controlled feedback methodology achieves a simple control structure which does not require a system compensation network. In addition, the inductor-based SWR has the capability to provide a large supplying current and high efficiency despite its slow response. To achieve F-DVS operation for the core processor, the asynchronous D-LDO regulator is used for fast voltage tracking at the V_{SUP}. The power switch arrays comprising P-MOSFETs and N-MOSFETs are implemented to achieve fast up-tracking and fast down-tracking, respectively. However, the fated power consumption and the unwilling output voltage ripple, which degrade the performance of the power module, stem from synchronous D-LDO regulators [25]–[28] that utilize a clock. In the proposed asynchronous D-LDO regulator, the BAWP controls the driving capability of power switches without the need of clock signals, and thereby minimizing current consumption considerably. A fast loop is exhibited in the proposed power module for the rapid regulation of the V_{SUP} because the asynchronous D-LDO regulator can achieve F-DVS operation without the bandwidth limitation derived from conventional A-LDO regulators. Moreover, a freeze mode is also utilized in BAWP to stop the wave pipeline operation, such that the ultra-low current consumption of 50 nA can be obtained in the steady-state.

To guarantee the high efficiency operation of the proposed power module, the asynchronous D-LDO regulator must be shut down due to the existence of dropout voltages on power

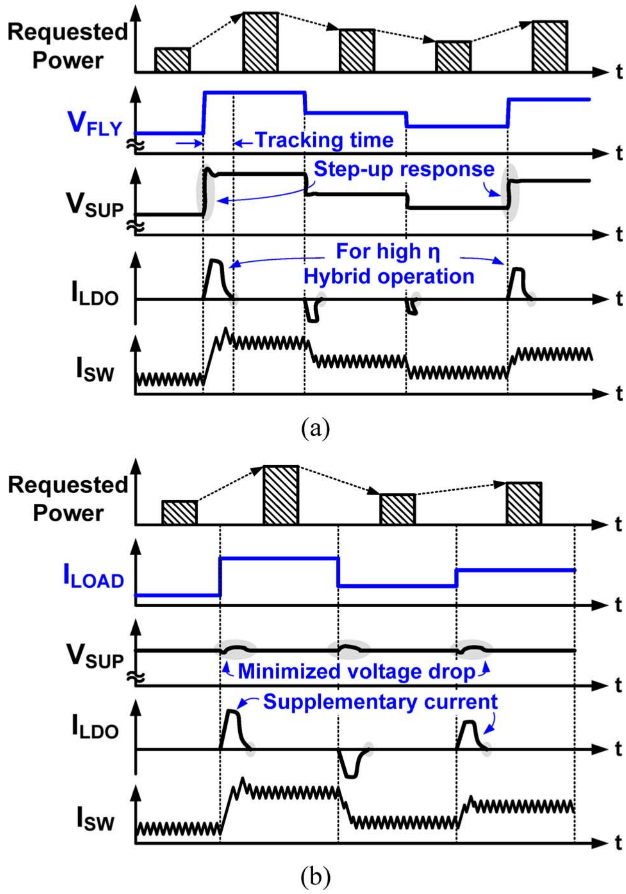

Fig. 5. Hybrid operation. (a) F-DVS operation with distinct power request in core processor. (b) Load transient response with different load variations at the output.

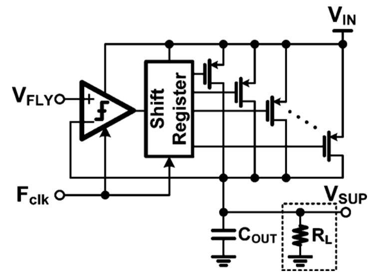

Fig. 6. Structure of synchronous D-LDO regulator.

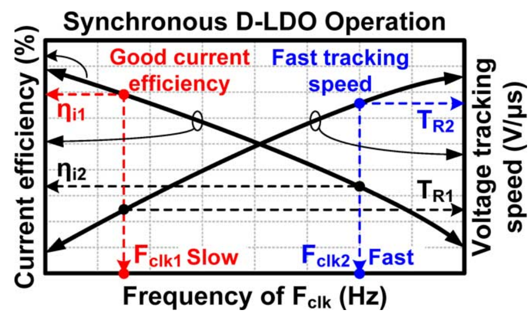

Fig. 7. Illustration of the synchronous D-LDO regulator operation.

switches. That is, the sensing current I_{SD}, which is proportional to the current of I_{LDO}, helps the SWR take over the full current driving function in steady-state. I_{SD}, which can also be regard as the auxiliary current, is obtained through the current sensing implementation [29]. That is, once the power switches conduct the driving current for the V_{SUP}, the I_{SD} can be carried out so as to increase the driving capability of the SWR. As a result, the driving current will be supplied by the SWR while the current flowing through the power switches in D-LDO regulator will be eliminated to get high efficiency. High power conversion efficiency and F-DVS operation can be simultaneously achieved in the integrated power module for SoC.

The proposed hybrid operations are illustrated in Fig. 5. The F-DVS operation is described in Fig. 5(a). With different requested power from the core processor, the indicative voltage V_{FLY} can be modulated to distinct voltage levels for the activation of F-DVS operation at the V_{SUP}. The asynchronous D-LDO regulator can provide the supplementary current I_{LDO} to help rapidly adjust the output voltage level of V_{SUP} for F-DVS operation. In addition, when the V_{SUP} reaches its target value, the current I_{LDO} can be set to zero to ensure high efficiency operation. The load transient response depicted in Fig. 5(b) has a response similar to that of the proposed hybrid operation. When the I_{LOAD} increases to provide a large amount of power to the core processor, the I_{LDO} helps minimize the voltage variation at the V_{SUP} and also ensures high power conversion efficiency in steady-state. Therefore, the hybrid operation simultaneously guarantees smooth supply voltage and high power conversion efficiency operation at both F-DVS operation and load transient response.

III. Asynchronous Digital-LDO Regulator

A D-LDO regulator is the characteristic of fast transient response by increasing operation frequency. With the implementation of a power switch array, the dropout voltage is rapidly adjusted through the digital control circuit. D-LDO is suitable for operation with low supply voltage because no analog circuit is presented in its control loop. In addition, the system bandwidth limitation, which is derived from the A-LDO regulator structure, is effectively released. Therefore, fast transient response can be guaranteed with the utilization of a D-LDO regulator.

A. Synchronous D-LDO Regulator

A Conventional D-LDO regulator usually adopts the synchronous control scheme [25]–[28] as shown in Fig. 6, where a clock signal is utilized to realize the operation. The comparator is used to monitor the output voltage V_{SUP} with the reference voltage V_{FLY}. In this work, a shift register is employed to activate the power switches. When large output power is requested to the D-LDO regulator, the comparator would detect the occurrence of insufficient energy at the V_{SUP} so that more power switches are turned on to provide the supplementary current. On the other hand, the power switches would be turned off if the V_{SUP} exceeds the V_{FLY}.

Synchronous D-LDO regulator performance is significantly affected by the operation clock frequency, F_{clk}. Given that the comparator has nearly infinite bandwidth, the shift register

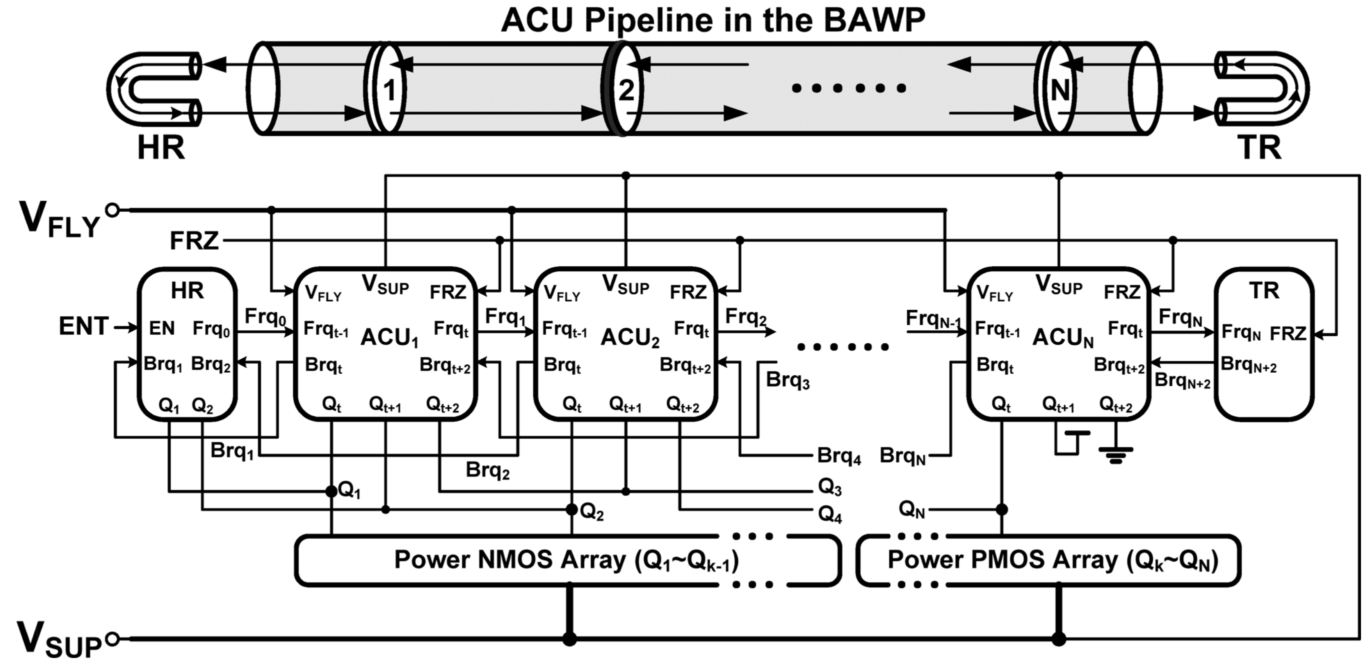

Fig. 8. Implementation of asynchronous D-LDO regulator with the bidirectional asynchronous wave pipeline (BAWP).

can be immediately informed to either increase or decrease the driving capability of power switches when the output loading is changed. However, the transient speed is mainly determined by F_{clk} because the shift register allows only one power switch to be turned on or off within per clock cycle in the synchronous D-LDO regulator. Illustration of the synchronous D-LDO regulator operation is shown in Fig. 7. If the synchronous D-LDO regulator operates with a slow frequency clock F_{clk1}, small power consumption realizes the better current efficiency η_{i1}, compared with that of η_{i2}, which is derived with the fast frequency clock F_{clk2}, thus resulting in larger current dissipation. However, fast tracking speed T_{R2} can be achieved by adopting the high frequency clock F_{clk2} in a synchronous D-LDO regulator but results in the worse current efficiency compared with that when operating with a slow frequency clock F_{clk1}. That is, higher frequency of F_{clk} leads to faster voltage tracking speed at the V_{SUP}. Moreover, the current efficiency of the D-LDO regulator is inversely proportional to the frequency of F_{clk}. Fast voltage tracking speed can be ensured; however, current efficiency will be deteriorated in the synchronous D-LDO regulator with a high frequency clock. A trade-off between voltage tracking speed and current efficiency exists in the clock-triggered synchronous D-LDO regulator design.

B. Bidirectional Asynchronous Wave Pipeline (BAWP) Controlled Asynchronous D-LDO Regulator

The proposed BAWP controlled asynchronous D-LDO regulator depicted in Fig. 4 achieves the F-DVS operation with the minimized current consumption. Fig. 8 shows the implementation of BAWP controlled asynchronous D-LDO regulator. Operation of the BAWP is similar to a clock-free shift register for determining the activation of power switches. That is, no constant clock signal triggers the asynchronous control units (ACUs) in BAWP. There are 32 ACU stages in this current design. The signal *ENT* will be enabled by the processor in SoC when the hybrid operation is activated. The D-LDO regulator with ACUs can then operate to provide the supplementary energy in order to obtain the requested power. With the activation of the enabling signal *ENT*, the ACUs control the power switches to modulate the output voltage V_{SUP} in the D-LDO regulator. As the result of asynchronous control scheme, only one ACU is activated at one time to minimize power dissipation. If the V_{SUP} is smaller than the V_{FLY}, the ACU pipeline executes the shift-right operation to turn on more power switches for V_{SUP} regulation. Contrarily, the shift-left operation occurs when the V_{SUP} is larger than the V_{FLY} to decrease the energy delivered to the V_{SUP}. In addition, the heading reflector (HR) and the terminal reflector (TR) are utilized as boundaries of BAWP owing to the removal of constant clock in asynchronous control. Unlike synchronous control, which requires a clock signal to activate all the control stages simultaneously, asynchronous control realizes the hand-shaking operation so that the problem of clock skew never occurs. The BAWP ensures that the ACU can be triggered by itself according to the energy demand of V_{SUP}. Moreover, the freeze mode can be enabled by signal *FRZ*, so as to freeze the convergent stage of ACUs. Therefore, the output voltage ripple in the proposed asynchronous D-LDO regulator can be eliminated, and the current consumption can be further minimized.

Implementations of ACU, latch-type comparator, HR, and TR are shown in Fig. 9. Each ACU in Fig. 9(a) contains a latch-type comparator, a multiplexer, and the control logics to control one power switch for the V_{SUP} modulation. The comparator is enabled by its prior ACU stage. That is, the ACU is motionless until the requested signal, Frq_{t-1}, is sent from its prior stage. The comparator compares the V_{SUP} with the reference voltage V_{FLY} and generates the signal Q_t to control

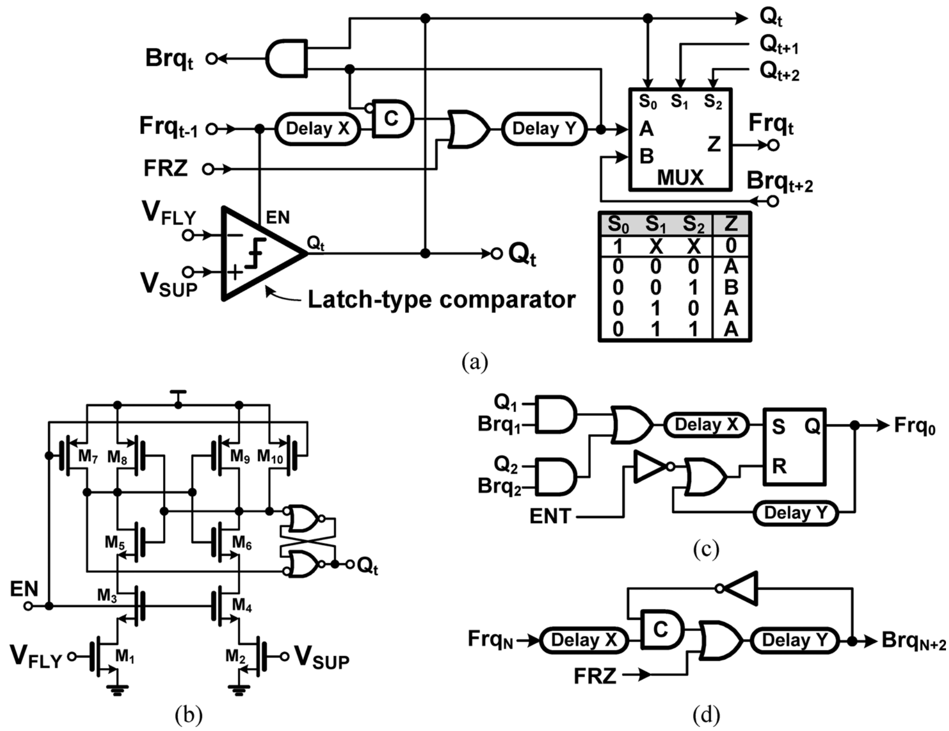

Fig. 9. Implementations of (a) ACU, (b) latch-type comparator, (c) heading reflector (HR), and (d) terminal reflector (TR).

the corresponding power switch. The multiplexer determines the forward request signal Frq_t from either the prior stage of Frq_{t-1} or the later stage Brq_{t+2} according to the control signals Q_t to Q_{t+2}. The operation principle of ACU in the BAWP is shown in the table attached in Fig. 9(a). The latch-type comparator is shown in Fig. 9(b). With the activation of enabling signal *EN* that is sent from the prior ACU stage, the output Q_t decides on state of corresponding power switch as well as on the forward request signal Frq_t. Both HR and TR, as respectively shown in Fig. 9(c) and (d), help guarantee the request signal Frq_t in the asynchronous BAWP at the first and last ACU stages, respectively. If the utilization of HR is missing, the request signal underflows in the BAWP when the V_{SUP} derives an overcharge at the first ACU stage. Similarly, TR helps prevent the request signal from overflowing in the BAWP while the V_{SUP} has insufficient energy at the last ACU stage.

Fig. 10(a) and (b) show the timing diagram of the single ACU operation at different conditions. If the V_{SUP} is smaller than the V_{FLY} in an ACU stage activated by signal Frq_{t-1}, the control signal Q_t is pulled low to turn on the p-type power switch or to turn off the n-type power switch in the proposed asynchronous D-LDO regulator. Thus, the energy supply for the V_{SUP} can be increased to raise the V_{SUP}. The forward request signal Frq_t is also set after a determined delay period, *Delay* X, to facilitate the shift-right operation in the BAWP to increase load driving. On the other hand, the back request signal Brq_t will be triggered if the V_{SUP} is larger than the V_{FLY}, so as to realize the shift-left operation in the BAWP to decrease the driving capability. Moreover, the periods, *Delay* X and *Delay* Y, are utilized to guarantee correct logic functions in ACUs.

Fig. 10(c) shows the BAWP control for F-DVS operation. The V_{SUP} needs to be raised to track the reference voltage V_{FLY}. Once the F-DVS operation is requested, the core processor sends a de-freeze signal, such that the operation of proposed asynchronous D-LDO regulator can be changed from the freeze mode to the tracking mode. In this work, the BAWP behaves the shift-right operation with the forward request signals, Frq_{t-1}, Frq_t, Frq_{t+1}, and so on. When the V_{SUP} reaches its target value of V_{FLY}, the back request signals are issued to stop the delivery of supplementary energy to the V_{SUP}. When the BAWP operation is converged to the two nearby ACU stages, the signal *FRZ* will be set by the processor to change the operation from the tracking mode back to the freeze mode. The F-DVS operation is ended through the indication of signal *FRZ*. Moreover, since all the ACUs are disabled in freeze mode, the current consumption of the proposed asynchronous D-LDO regulator only requires approximately 50 nA, which is nearly equal to the leakage current derived by 40 nm core devices. As a result, fast response and ultra-low static current consumption are simultaneously achieved by using the proposed asynchronous D-LDO regulator.

IV. Ripple-Based Control SWR

To quickly take over the power supplying authority from the asynchronous D-LDO regulator at the end of hybrid operation for high efficiency, the SWR also needs to behave the advantage of fast response. Transient speed of SWR is theoretically restricted because the inductor current level cannot be instantaneously raised within a finite charging period of time. Furthermore, system compensation limits the bandwidth, and thus worsens the transient response although it can guarantee the stable operation in pulse width modulation (PWM) control. Several fast transient techniques have been reported to enhance

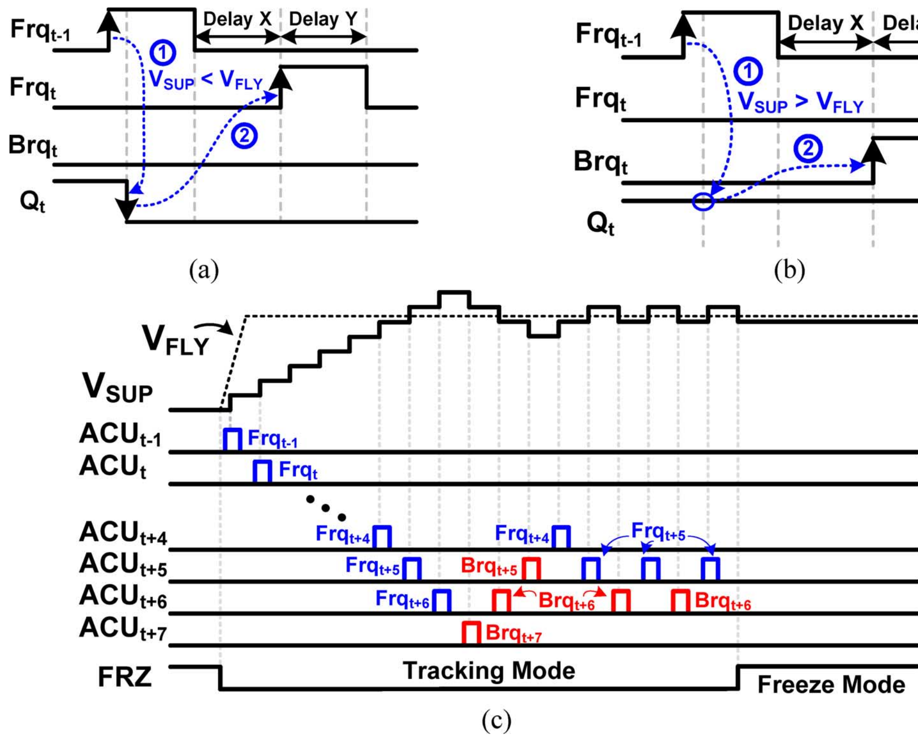

Fig. 10. Timing diagrams. (a) Single ACU operation when the V_{SUP} is smaller than the V_{FLY}. (b) Single ACU operation when the V_{SUP} is larger than the V_{FLY}. (c) BAWP operation when the F-DVS is activated.

the transient response of SWR [30]–[32]; however, the complex circuit implementations would be unacceptable. Utilization of a ripple-based control in SWR is characterized by fast response because its reduced-complexity structure achieved by the comparator-controlled feedback scheme realizes a near-infinite system bandwidth in control loop. That is, the power stage immediately extends the inductor charging or discharging periods for the rapid modulation of inductor current when the demand for supply power is changed.

A. Operation of Ripple-Based Control SWR

Circuit structure of the proposed ripple-based control SWR is shown in Fig. 4. Conventional ripple-based control design uses a large equivalent-series-resistance (ESR) on output capacitor to ensure stable operation [21]–[24]. Stability criterion of the ripple-based control step-down converter is given in [21] and is shown in (1).

$$R_{ESR} \times C_{OUT} \geq \frac{T_{ON}}{2} \qquad (1)$$

where R_{ESR} represents the ESR value on output capacitor C_{OUT}. T_{ON} is the period that the high-side power MOSFET of buck converter is turned on. Utilization of a large ESR causes the large output voltage ripple, and thus deteriorating the quality of supply voltage for the core processor. To strengthen the supply quality of SWR with a ripple-based control, ESR on the output capacitor has to be as small as possible. The LPA shown in Fig. 4 is used to guarantee stable operation when a small ESR is adopted in the ripple-based control SWR, so as to achieve low output voltage ripple. The operations of the ripple-based control SWR with LPA are described in Fig. 11.

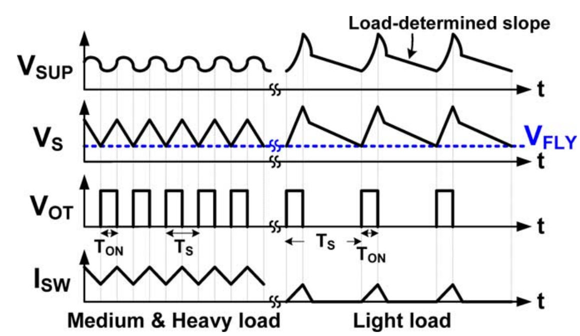

Fig. 11. Operations of the ripple-based control SWR with LPA circuit.

An LPA circuit serves as the differentiator that generates a sensing signal, V_S, which is proportional to the differentiation of voltage ripple on V_{SUP} and is similar to the current ripple of the inductor in SWR. In case of medium or heavy load conditions, the continuous-conduction-mode (CCM) operation is activated to provide high driving capability. When the V_S touches the reference voltage V_{FLY}, the on-time generator shown in Fig. 4 is activated to generate a constant on-time pulse, V_{OT}, with the on-time period, T_{ON}, so that the high-side power MOSFET M_P can be turned on to activate the inductor charging period. On the other hand, the low-side power MOSFET M_N is turned on to release the energy from the inductor at the end of the on-time period. Nevertheless, the electromagnetic interference (EMI) problem becomes a tough issue when the ripple-based control SWR is integrated in SoC. Since no constant frequency clock

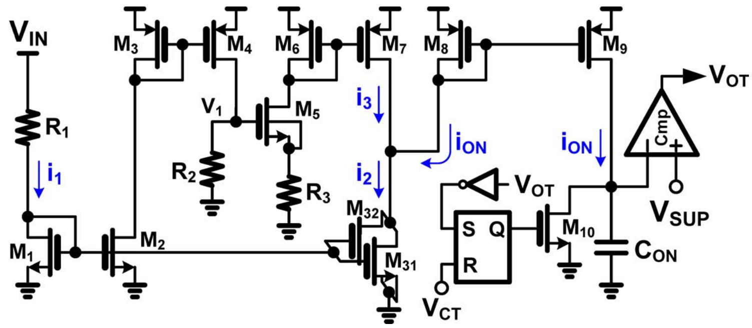

Fig. 12. Schematic of the on-time generator.

exists in ripple-based control, the varied switching frequency, which results in a noisy frequency spectrum, affects the functions of other integrated circuits in SoC. In other words, if the switching frequency is nearly constant in CCM operation, the EMI problem will be alleviated by an external EMI filter.

Duty cycle of the ripple-based control buck converter can be expressed by (2).

$$\frac{V_{SUP}}{V_{IN}} = D = \frac{T_{ON}}{T_S} \tag{2}$$

where T_S is the switching period. Thus, the switching frequency of SWR, f_S, can be described in (3).

$$f_S = \frac{1}{T_S} = \frac{V_{SUP}}{V_{IN}T_{ON}} = \text{Constant}, \text{ if } T_{ON} \propto \frac{V_{SUP}}{V_{IN}} \tag{3}$$

where f_S will be a constant value if only the T_{ON} is proportional and inversely proportional to V_{SUP} and V_{IN}, respectively. That is, the adjustment of T_{ON} with the distinct input and output voltages results in a nearly constant switching frequency in the ripple-based control SWR.

The ripple-based control SWR can also operate with a reduced switching frequency at light loads as shown in Fig. 11. Unlike the PWM control that operates with a constant frequency clock to trigger the switching cycle, the ripple-based control reduces the switching frequency at light loads to minimize power loss and obtain high efficiency. The discontinuous-conduction-mode (DCM) operation is automatically achieved by using the comparator-triggered on-time generator and the zero current detection mechanism at the low-side power MOSFET [33], [34]. As a result, the switching frequency in DCM operation varies according to the load-determined slope at V_{SUP} caused by distinct output load conditions, such that the power conversion efficiency can be guaranteed at the light load conditions.

B. On-Time Generator

Fig. 12 shows the circuit of on-time generator. The on-time period, T_{ON}, of the on-time signal, V_{OT}, is determined by both V_{IN} and V_{SUP}. The current i_1 is generated by V_{IN} as shown in (4) that the large V_{IN} will indicate the large i_1.

$$i_1 = \frac{V_{IN} - V_{GS,M1}}{R_1} = \frac{1}{2}i_2. \tag{4}$$

To enhance the linearity of voltage-to-current conversion of (4), the $V_{GS,M1}$, which is the non-ideal factor caused by the gate-to-source voltage of M_1, needs to be eliminated. The MOSFET M_5 also forms another voltage-to-current conversion to generate the current i_3 described in (5), which is also affected by the gate-to-source voltage $V_{GS,M5}$. By removing the body effect on M_5, both the process-dependent gate-to-source voltages, $V_{GS,M1}$ and $V_{GS,M5}$, become nearly equivalent only if M_1 and M_5 are implemented with the same aspect ratio.

$$\begin{aligned} i_3 &= \frac{V_1 - V_{GS,M5}}{R_3} = \frac{i_1 R_2 - V_{GS,M5}}{R_3} \\ &= \frac{R_2 V_{IN} - (R_1 + R_2)V_{GS,M1}}{R_1 R_3}, \text{ if } V_{GS,M1} \approx V_{GS,M5}. \end{aligned} \tag{5}$$

As a result, the T_{ON}, which denotes duration that voltage crossed on the capacitor C_{ON} is charged to the V_{SUP} by the current i_{ON}, can be obtained as shown in (6). Finally, once the resistors, R_1, R_2, and R_3, are chosen properly, the T_{ON} shown in (7) becomes proportional and inversely proportional to the output voltage V_{SUP} and to the input voltage V_{IN}, respectively. This condition helps achieve a nearly constant switching frequency in the ripple-based control SWR.

$$\begin{aligned} T_{ON} &= \frac{C_{ON}V_{SUP}}{i_{ON}} = \frac{C_{ON}V_{SUP}}{i_2 - i_3} \\ &= \frac{C_{ON} \times V_{SUP}}{(2R_3 - R_2)V_{IN} + \frac{(R_1 + R_2 - 2R_3)V_{GS,M1}}{R_1 R_3}} \end{aligned} \tag{6}$$

$$T_{ON} = (C_{ON}R_1)\frac{V_{SUP}}{V_{IN}} \propto \frac{V_{SUP}}{V_{IN}}, \text{ if } R_1 = R_2 = R_3. \tag{7}$$

C. Leading Phase Amplifier (LPA)

Fig. 13 shows the proposed LPA circuit, which is used to guarantee the stable operation of the ripple-based control SWR without the use of a large ESR. Fig. 13(a) depicts the circuit schematic. A negative feedback loop formed by the OP_1 transmits the voltage ripple at the V_{SUP} into the LPA. A voltage-control-current-source (VCCS) structure is implemented by using M_1, M_2, M_5, and the capacitor C_{DIF} to achieve the phase lead operation. The structure can also be regarded as the high-pass filter that enables the ripple voltage of V_{SUP} to be converted to the current i_d through the C_{DIF}. The voltage ripple at the V_{SUP} of the buck converter is illustrated in (8).

$$\begin{aligned} v_{SUP}(t) &= v_{ESR}(t) + v_{C_{OUT}}(t) \\ &= R_{ESR}i_{SW}(t) + \frac{1}{C_{OUT}}\int i_{SW}(t)dt \end{aligned} \tag{8}$$

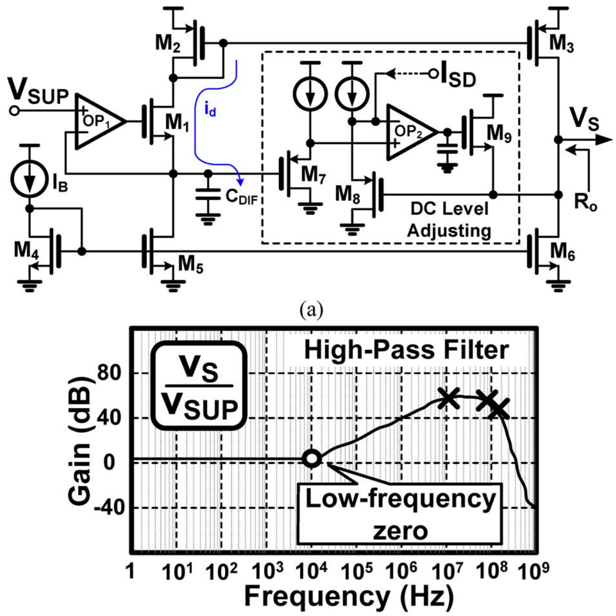

Fig. 13. LPA circuit in the proposed SWR. (a) Schematic. (b) Frequency response.

where the i_{SW} is the inductor current ripple.

The VCCS circuit acts as the differentiator. Thus, the i_d is generated through the C_{DIF} shown in (9) with the s-domain description.

$$i_d(s) = \frac{v_{SUP}(s)}{\frac{1}{sC_{DIF}}} = sC_{DIF}v_{SUP}(s). \tag{9}$$

The i_d can be seemed as the small signal current which is mirrored to M_3 for generating the sensing signal V_S. Therefore, the V_S, which can be regarded as the differential result of V_{SUP}, is then obtained by means of the output resistance R_o as shown in (10).

$$\begin{aligned} v_s(t) &= C_{DIF}R_o\left(R_{ESR}\frac{di_{SW}(t)}{dt} + \frac{i_{SW}(t)}{C_{OUT}}\right) \\ &= R_{ESR}C_{DIF}R_o\frac{V_{IN}-V_{SUP}}{L} + \frac{C_{DIF}R_o}{C_{OUT}}i_{SW}(t). \end{aligned} \tag{10}$$

Here, the V_S can be further simplified as expressed in (11) if a small R_{ESR} is used.

$$v_S(t) \approx \frac{C_{DIF}R_o}{C_{OUT}}i_{SW}(t), \text{ if } R_{ESR} \text{ is small.} \tag{11}$$

Consequently, the ac signal on V_S replicates the inductor current ripple i_{SW}. That is to say, the inductor current ripple information is obtained without the need for a large ESR through the proposed LPA. Moreover, the DC level adjusting is used to accomplish the dc voltage tracking between the V_{SUP} and the V_S. A compensated feedback loop achieved by the OP_2 ensures the V_S to track the dc voltage value of V_{SUP}. Therefore, the V_{SUP} can be regulated to its target value because of the comparator-controlled structure in the ripple-based control SWR.

Frequency response of the proposed LPA circuit is shown in Fig. 13(b). A low-frequency zero, which is generated by the capacitor C_{DIF}, ensures the phase lead operation as well as the differentiate function. By adopting the differentiate function, the V_S becomes proportional to the inductor current ripple without adopting a large ESR on the output capacitor. Thus, output voltage ripple in the ripple-based control SWR can be surely minimized. In the meanwhile, stability can also be guaranteed as well as high power conversion efficiency and fast response in ripple-based control SWR. Fig. 14 shows the simulated result that demonstrates the utilization of LPA circuit in the ripple-based control SWR.

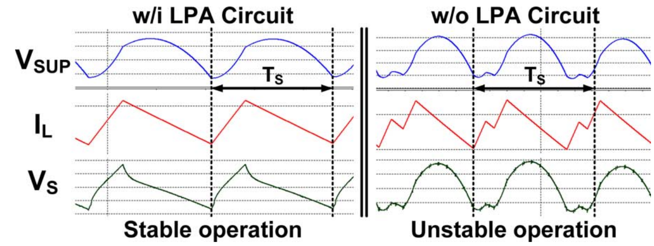

Fig. 14. Simulated result of the LPA circuit in ripple-based control SWR.

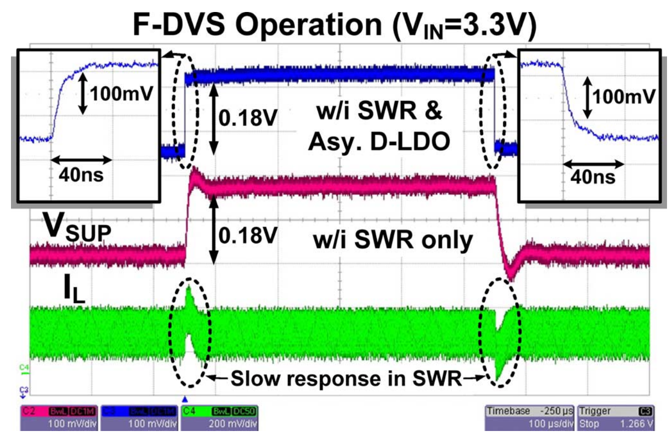

Fig. 15. Measured waveform of F-DVS operation with both up-tracking and down-tracking operations.

V. Experimental Results

The proposed integrated power module with asynchronous D-LDO regulator and SWR for hybrid operation was fabricated by 40 nm CMOS technology. Nominal output voltage of the proposed power module is 1 V. Off-chip inductor is 1 μH with the output capacitor of 0.1 μF in SWR. Measure F-DVS operation is shown in Fig. 15. If V_{SUP} is requested with a 0.18 V voltage step with the V_{IN} of 3.3 V, the asynchronous D-LDO regulator helps guarantee the F-DVS operation within 20 ns. When the up-tracking is enabled with hybrid operation, the BAWP in asynchronous D-LDO regulator activates the shift-right operation to turn on the p-type power switches to increase the supplementary current. Therefore, the tracking speed can be achieved about 9 V/μs. The freeze mode also helps eliminate the output voltage ripple to derive the high-quality supply. Compared the hybrid operation to that of SWR regulator only, the voltage tracking speed in SWR is obviously restricted due to the determined system bandwidth and the inductor.

Besides, the SWR will provide all load current to shut down the asynchronous D-LDO regulator for achieving high power

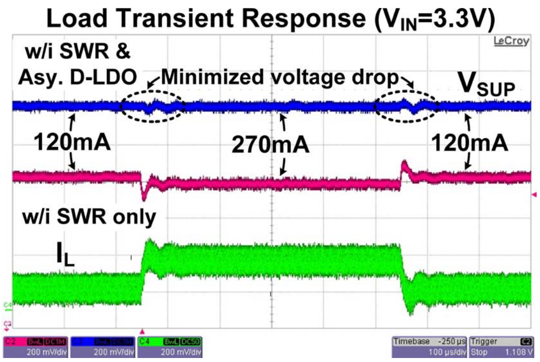

Fig. 16. Measure load transient response with and without the hybrid operation.

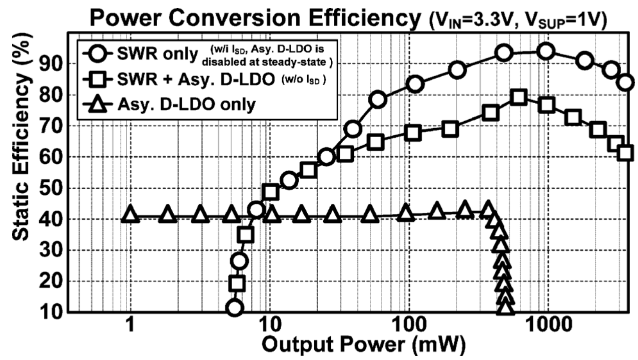

Fig. 18. Measure steady-state power conversion efficiency.

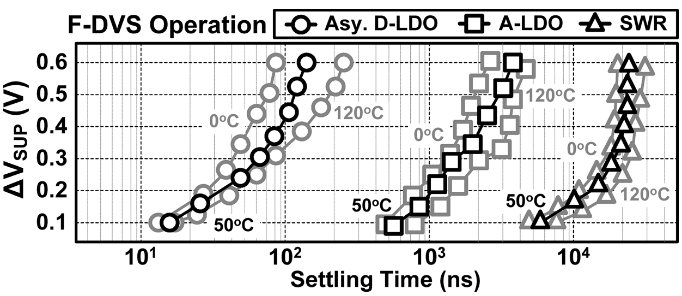

Fig. 17. Measure F-DVS operation with distinct power modules.

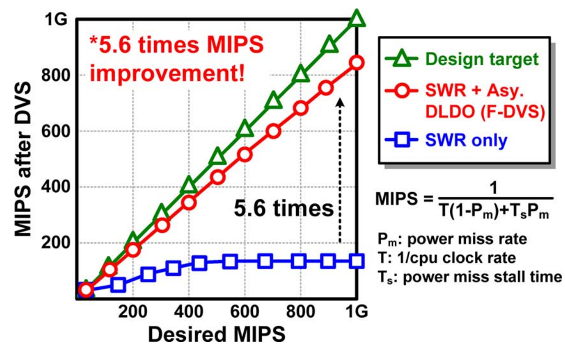

Fig. 19. Measured MIPS performance in core processor with distinct power modules.

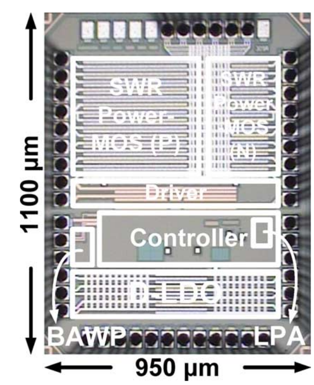

Fig. 20. Chip micrograph.

conversion efficiency. The similar operation is derived in the down-tracking operation. The BAWP in asynchronous D-LDO regulator can operate with the shift-right operation to fast modulate the V_{SUP}, so that the improved voltage tracking operation is obtained. Fig. 16 shows the load transient response with the V_{IN} of 3.3 V. The hybrid operation can also be activated that the asynchronous D-LDO regulator will rapidly provide the compensated current if the demanded supply current is increased. Thus, the voltage drop at the V_{SUP} can be minimized when the hybrid operation is activated.

Fig. 17 shows the measured F-DVS operation with distinct power modules with the V_{IN} of 3.3 V. Voltage tracking speed can be improved to thousands of mV per micro-second due to the utilization of asynchronous D-LDO regulator. The BAWP ensures fast response for voltage tracking and achieves power-efficient operation by using asynchronous control scheme. A-LDO performance is limited by the finite bandwidth. The tracking speed in SWR is restricted by both bandwidth and inductor. Here, fast response of the proposed asynchronous D-LDO regulator is demonstrated. Fig. 18 shows the power conversion efficiency. Since the measured efficiency is obtained in steady-state, the hybrid operation in the proposed power management was ended so that the proposed asynchronous D-LDO regulator can be operated with freeze mode in steady-state. If the operation contains the auxiliary current I_{SD}, all driving current will be supplied by the SWR and the asynchronous D-LDO regulator remains only a 50 nA current consumption in steady-state to get high efficiency. That is, the SWR only operation helps obtain the peak efficiency of 94%. Once the hybrid operation is activated without the auxiliary current I_{SD}, the asynchronous D-LDO regulator will not be shut down in steady-state. Therefore, efficiency of the proposed power management will be deteriorated since partial of the load current is provided by the D-LDO regulator. Fig. 19 shows the improvement of MIPS performance in the realistic core processor. It demonstrates the MIPS can be improved by 5.6 times with the proposed F-DVS operation compared to that of the SWR only. Since the asynchronous D-LDO regulator can help rapidly modulate the supply voltage, the idle period in the practical DVS operation can be minimized. This improvement helps the MIPS performance in the core processor match up with the design target, so as to shorten the total instruction steam duration with the serious tasks for guarantee the operated efficiency in core processor. Fig. 20 shows the chip micrograph with 1.04 mm^2 active area. The test chip integrates both SWR and asynchronous D-LDO regulator to achieve the hybrid operation. The detailed design specifications are listed in Table II, while the comparisons of the prior LDO designs are shown in Table III. Despite of fast response in the proposed asynchronous

TABLE II
DESIGN SPECIFICATIONS OF PROPOSED POWER MODULE

Topology	Asynchronous D-LDO regulator	Ripple-based control SWR
Fabricated process	40 nm CMOS	40 nm CMOS
Input voltage	0.9 V – 3.6 V	2.2 V – 3.6 V
Output voltage	0.8 V – 3.5 V (1 V nominal)	0.6 V – 3 V
Current consumption	50 nA (Freeze mode)	30 µA (no switching)
Inductor	N/A	1 µH
Output capacitor	N/A	0.1 µF
Maximum output power	0.4 W	1.2 W
Voltage tracking capability	9 V/µs	0.1 V/µs
Current efficiency / Power efficiency	99.9 %	Peak 94%
Active area	0.08 mm^2	0.96 mm^2

TABLE III
COMPARISONS OF PRIOR LDO REGULATORS

	This work	[25]	[26]	[27]	[29]	[35]
Type	LDO	1/2 V_{DD} Generator	LDO	LDO	LDO	LDO
Control methodology	Digital	Digital	Digital	Digital	Analog	Analog
Technology	40nm	90nm	65nm	40nm	0.35µm	0.35µm
Minimum input voltage (V)	0.9	2.4	0.5	1.34	1.05	2
Nominal output voltage (V)	1	1.2	0.45	1.2	0.9	1.8
Maximum load current (mA)	200	1000	0.2	250	50	200
Output capacitor	Cap-free	Cap-free	Cap-free	Cap-free	1 µF	1 µF
Line regulation (mV/V)	1.8	N/A	3.1	N/A	1.1	2
Load regulation (mV/mA)	0.05	N/A	0.65	0.44	0.06	0.17
Current consumption in steady-state (µA)	0.05	25700	2.7	0.13-10	4.04-164	20-320
Active area (mm^2)	0.08	0.03	0.042	0.057	0.053	0.264
Current efficiency (%)	99.97	97.5	98.7	96-99.95	99.67	99.8

D-LDO regulator, the minimized 50 nA current consumption also helps achieve the current efficiency of 99.97%.

VI. CONCLUSION

A power module of the asynchronous D-LDO regulator and the ripple-based control SWR is proposed to achieve the integration in SoC. PLL-modulate control loop provides the indicative reference voltage to guarantee the near-optimum supply voltage according to the demand from system core processor. Parallel connection of both D-LDO regulator and SWR forms the hybrid operation to realize F-DVS operation and high power conversion efficiency. The asynchronous D-LDO regulator ensures the F-DVS operation with the clock-free BAWP control, which can further minimize the current consumption to 50 nA by freeze mode operation, for power saving. The ripple-based control SWR operates with the simple structure while accomplishing the fast response. Utilization of the LPA helps guarantee the stale operation with the need of large ESR, so as to strengthen the supply quality. The proposed power module fabricated by 40 nm CMOS process occupies a 1.04 mm^2 silicon area, which achieves 94% peak efficiency with the voltage tracking speed of 7.5 $\mathrm{V}/\mu\mathrm{s}$ for the 5.6 times MIPS performance improvement.

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