# Electromigration study of eutectic SnPb flip-chip solder joints on ceramic substrates

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## Abstract

This study investigates electromigration study of eutectic SnPb flip-chip solder joints on ceramic substrates. The under bump metallization (UBM) structure consists of 5-μm Cu / 3-μm Ni under bump metallization (UBM). Under the current stressing by 0.9A at 150°C, we did not find void formation but a large amount of intermetallic compound (IMC) of $Cu_6(Sn,Ni)_5$ were formed when the bump resistance increased 10 mΩ. Three-dimensional electrical simulation by finite element analysis was carried out to simulate the current density distribution in solder joints with slit Cu traces. It is found that the current density was almost uniformly distributed in solder joint for this structure. It is found that the bump resistance only increases 0.07mΩ when half of the solder bump was transformed into $Cu_6Sn_5$ IMC. The reason for the low crowding effect in the solder joints will be discussed in the conference.

## Introduction

Under-bump metallization (UBM) is very important in the flip-chip technology because it acts as a solder wettable layer, diffusion barrier, and adhesion layer [1]. Currently, the most common choices for solder wettable layers are Cu and Au, and the diffusion barrier and adhesion layers are TiW, Ti, Cr, Al, NiV, and Ni. These choices depend not only on a solder bumping process, but also on a balancing of capabilities and costs, as well as the manufacturer's skill and experience. When a trilayer thin film of Cr/Cu/Au is applied as UBM, spalling of Cu–Sn compounds from the Cu–solder interface occurs and results in a weak mechanical solder joint, which is one of the most serious reliability problems because the Sn-based Pb-free solders react very fast with Cu and the amount of Cu is very limited in the thin-film metallization [2–4]. To overcome the spalling problem, a 5-μm-thick electroplated Cu UBM has been integrated into the UBM so that the chemical reaction will not consume all the Cu and no spalling may occur during aging[5]. However, when the joint is subjected to current stressing, current crowding leads to a rapid dissolution of the 5-μm-thick Cu UBM at the corner where electrons entered from Al interconnect to Cu UBM and the joint failed quickly [6]. Due to the demand for high performance and miniaturization in the electronics industry, the problem of electromigration must be overcome; a thicker Cu UBM has been designed to overcome the electromigration-induced failure[7]. Currently, the design rule requires that each flip-chip solder joint of 50 _m in diameter carries 0.2 A, which means that the average current density in such a joint is about $10^4$ A/cm$^2$ [7]. The International Technology Roadmap for Semiconductor (ITRS) projections indicated that electromigration is a near-term issue in high current density packages [8].

A lower processing temperature will prevent the malfunction of a temperature-sensitive device as well as minimize built-in stress after cooling. In this study, the eutectic tin–lead (63% Sn 37% Pb) was chosen due to its low melting temperatureof 183 C. The metallization layers used in this study are similar to the under bump metallurgy (UBM) used for flip chip technology. Because the process is compatible with the current manufacturing process in the IC industry, this bonding technology can be applied readily to the industry. Another advantage of the design is that it makes use of the solder's unique properties. First, solder is a metal. Metal has the lowest permeability to moisture compared with epoxy, glass, and other nonmetal materials. With a width of a few micrometers, metals can block moisture for over a decade. In addition, solders are known to possess self-alignment properties in flip chip technology. As a bonding material, solder provides good hermeticity. Most importantly, the process is cost effective. The design is useful for future applications in optoelectronic packaging.

## Experiment and Simulation

The ceramic substrate was used in this study. The test specimen was adopted the eutectic SnPb solder with the 5-μm Cu / 3-μm Ni under bump metallization (UBM). The daisy-chain with four bumps was adopted under electromigration test and four points test structure is shown in the figure. 1. The electron through the Cu lead under the Bump 2 and distribute Bump 2 、Bump 3 and Bump 4 and leave the Cu lead under the Bump 6. The resistance of measurement include two via, two bumps and one slit Cu trace. The dimension of the solder joint is shown schematically in the figure. 2(a) and figure.2(b). The 5-μm Cu was sputtered and then the 3-μm Ni layer was electroplated in the chip side. The 10-μm Ni was electroplated in the board side. The diameter of UBM opening and passivation opening were 80 μm and 40 μm separately. Eutectic SnPb solder was electroplated to joint on W via in the ceramic substrate. The bump height was about 60 μm. The pitch of each bump was 175 μm. There are special six slit Cu traces used in this layout. One of six Cu traces was 8 μm wide and 0.8 μm thick, and total Cu traces was 48 μm wide. The test condition applied 0.9 A through Cu line under bump 2 to Cu line under bump 6 on the 150°C hot plate. The resistance history was monitored under current stressing. We observed microstructrue after the bump resistance increasing 10mΩ, 30mΩ and open. The current was terminated by a computer program when the resistance of the stressing circuit exceeded 5000Ω. The infrared microscopy was utilized to examine whether there was any damage in the Cu trace, since Si is transparent to infrared. After checking the failure of the Cu trace, the samples were ground with SiC papers and polished with $Al_2O_3$ powder. Scanning electron microscopy (SEM) was adopted to inspect the microstructure of the solder joints.

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The intermetallic compound (IMC) formed between the UBM and the solder was also considered in the simulation models. 3 μm of electroplated Ni was assumed to react and form a layer of 1.0 μm $Ni_3Sn_4$ IMC in the chip side. Similarly, 10 μm of electroplated Ni is assumed to react and form 1.0 μm of $Ni_3Sn_4$ IMC in the board side. Be due to find the increasing of bump resistance after current stressing. We simulated two different conditions. First, the $Cu_6Sn_5$ IMC was formed a half of bump 5. Second, remove one slit Cu line between bump 4 and bump 5. The parameters of the materials used in the simulation can be found in our previous publication.[10] The model used in this study was based on SOLID69 eight-node hexahedral coupled-field elements using ANSYS simulation software developed by ANSYS Inc. USA. The simulation results focus on the maximum current in the solder joints, in order to analysis the current density part of lifetime.

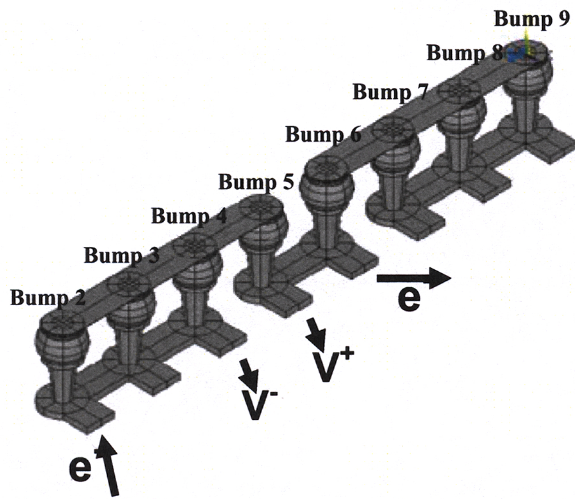


FIGURE 1. Four points test structure

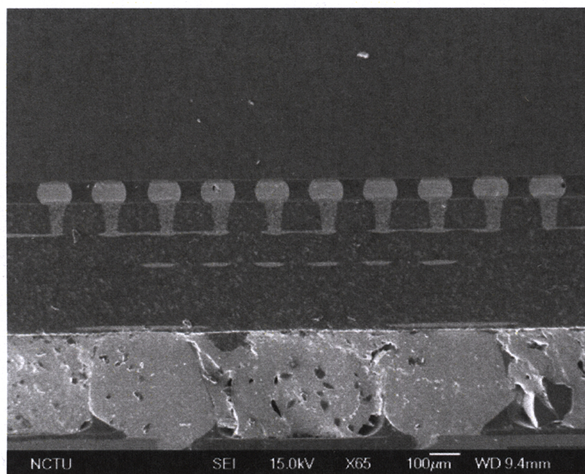


FIGURE 2(a). The SEM image of total eutectic bumps

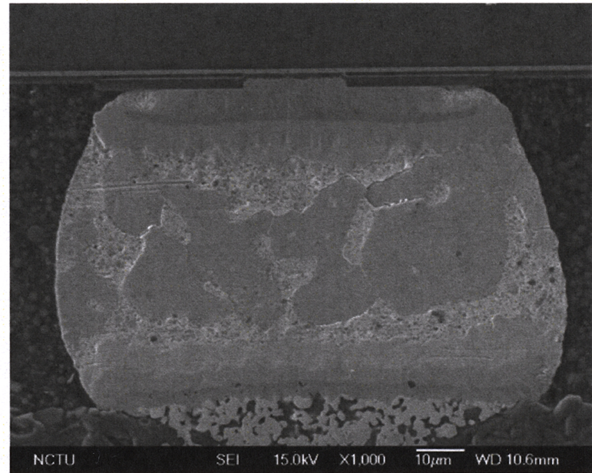


FIGURE 2(b). The SEM image of one eutectic bump

## Results

The failure time of the eutectic SnPb solder after 0.9 A current stressing on 150°C is about 379.5 hrs. The resistance profile was shown in figure. 3(a). The resistance slowly and almost linear increased during more than 95% of stressing time. At remaining stressing time, the resistance suddenly increase and went to the terminated resistance. Before investigating the microstructure of the solder bumps, the radiance mode of IR technology detected the damage of the each Cu trace is divided into six individual lines. In figure 3(b), the electron flow for each Cu trace come form left hand side to right hand side. It found that the bump 5 and Cu trace upon the bump 4 was destroyed. The serious damage always occurs in bump 5, because there is the high current density in bump 5. Figure 3(c) shows the failure mode in bump 5 after stressing downward. We observed the large damage in the chip side and lead phase accumulated in board side. Because this structure has very low crowding ratio, so there was a large damage in solder joint of center of chip side.

The bump resistance increased 10mΩ, figure 4 shows the cross-sectional SEM image for bump 5. We did not find void formation but a large amount of intermetallic compound (IMC) of $Cu_6(Sn,Ni)_5$ were formed when the bump resistance increased 10 mΩ. The IR image of Cu trace in the chip side was shown in figure 5. There were not large damage in the Cu trace on the grounds that this IR image.

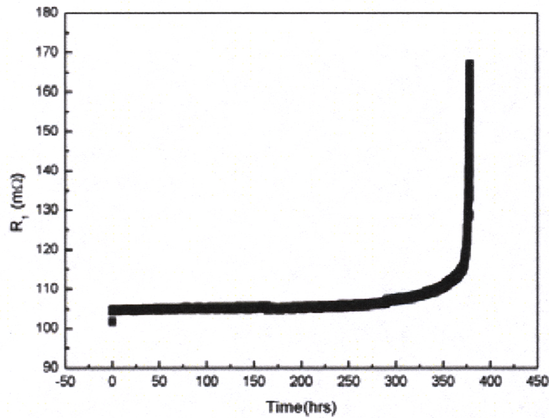


FIGURE 3(a). The bump resistance profile

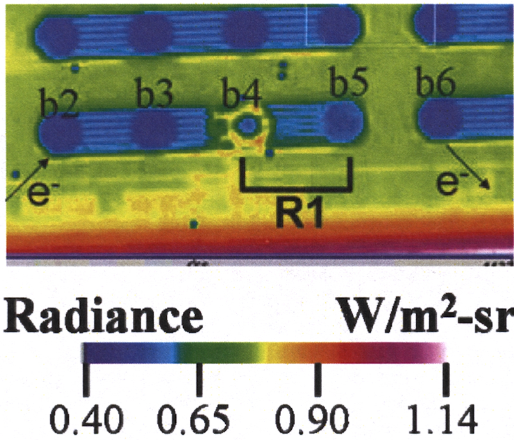


FIGURE 3(b). The bump resistance profile

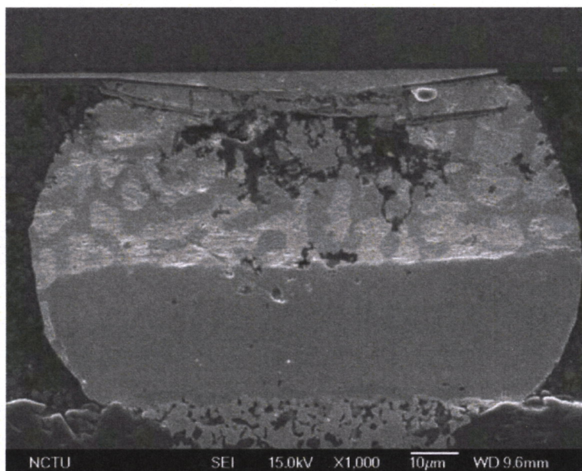


FIGURE 3(c). The failure mode of bump 5

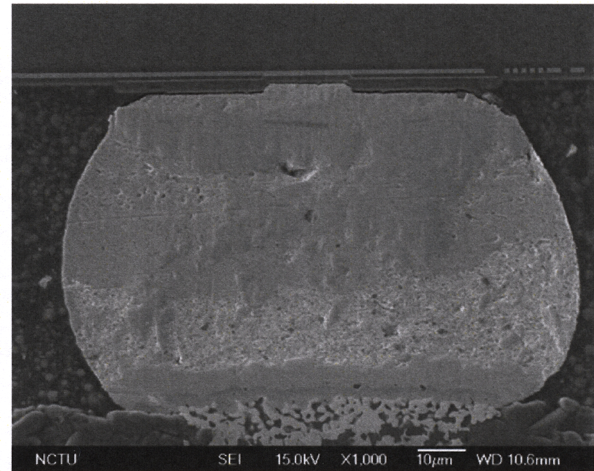


FIGURE 4. The SEM image of bump 5

## Discussion

In order to obtain the information of current crowding in the solders, we simulate this structure with two bumps. Figures 6(a) and 6(b) show the current density distribution in two bumps and one solder separately. It knows that there is low current crowding in solder joint. Because the good passivation opening size and via made the current density to distribute uniformly in solder.

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