New design techniques for a complementary metal-oxide semiconductor current readout integrated circuit for infrared detector arrays

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Abstract. A new share-buffered direct-injection (SBDI) current readout circuit with high injection efficiency, low noise, high dynamic range, and good threshold control is proposed. The circuit is superior to the traditional direct-injection (DI) current readout circuit. Using the SBDI readout circuit, the same excellent performance of the buffered direct-injection (BDI) current readout can be achieved, but only half the chip area and power consumption are required. Thus the SBDI is more suitable for infrared (IR) readout applications, especially for 2-D focal plane arrays under strict power and area limitations. A dynamic discharge source follower (DDSF) output stage is also proposed and analyzed. It can improve the speed performance of the conventional source-follower output buffer and requires very little power dissipation. Both simulation and experimental results have verified the functions and the advantageous features of the proposed readout structure.

Subject terms: IR focal plane arrays; detectors; IR imaging; readouts; integrated circuits; injection efficiency.

Optical Engineering 34(1), 160–168 (January 1995).

1 Introduction

The photovoltaic (PV) infrared (IR) detector is potentially suitable for the applications in low-power, large-area second-generation multispectral IR imagers because it has a much larger sensor resistance than the photoconductive IR detector. In the readout operation of the PV IR detector, voltage readout and current readout are the two popular approaches. Usually, the current readout is chosen because of the noise, bias point, and the power dissipation consideration.

Because the PV IR detector device is reverse biased, both surface generation-recombination current and surface tunneling current are increased, which causes the $1/f$ noise to increase proportionally.[1,2] Moreover, the device bias also leads to the bias-induced dc currents. Clearly, maintaining a low detector bias is important for the current readout circuit to minimize the noise and the excess dc current of IR detectors.

Generally, the total input referred noise current of an IR detection channel is made up of four components: background optically generated shot noise, detector noise, input stage noise, and signal processing stage noise. The goal of a current readout structure is to make the other three noise components less than the background shot noise, so that only the inevitable background shot noise dominates. According to this requirement, the current readout input stage needs to have a very small input impedance to achieve a high injection efficiency. Otherwise, less signal and background shot noise from the detector are injected, and hence the noise of the readout structure becomes more significant to degrade the system noise performance [noise-equivalent difference in temperature (NEΔT) sensitivity].

So far, several current readout schemes and structures such as the source follower per detector[3–5] (SFD), the capacitive transimpedance amplifier[3,5] (CTIA), the direct injection[1,6,7] (DI), and the buffered direct injection[1,3,6–8] (BDI), have been proposed. Among them, both SFD and DI schemes have the problems of poor injection efficiency and nonuniform detector bias. In the CTIA, the reset operation induces a certain amount of clock feedthrough on the detector node and limits the output swing. In the BDI, the additional chip size and power dissipation of the buffer often become intolerable, especially in large and high-performance focal plane arrays (FPAs).

In this paper, a new current readout scheme called the share-buffered direct injection (SBDI) is proposed to solve the mentioned problems and improve the readout performance. It has been shown from both simulation and experimental results that the proposed SBDI has the same high injection efficiency and good zero-bias stability as the BDI. But the SBDI has less chip area and power dissipation than the BDI. Thus the SBDI is suitable for the large and high performance 2-D IR detector array.

In Sec. 2, the circuit structure of the new SBDI readout input stage is described and comparisons with DI and BDI

Paper 17014 received Jan. 17, 1994; revised manuscript received Apr. 29, 1994; accepted for publication July 13, 1994.
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in injection efficiency, noise performance, power requirement, area consumption, threshold control, and 2-D application possibility are also discussed. In Sec. 3, a dynamic discharge source-follower output stage, including correlated double sampling (CDS) and autoclamping, is described. The speed performance, output range, and power dissipation of this output stage are also analyzed. In Sec. 4, both simulation results and experimental results of the fabricated SBDI readout chip are presented. Finally, a conclusion is given.

2 SBDI Current Readout

In the proposed new SBDI structure, a differential-input-to-single-ended-output amplifier with one commonly shared half circuit and several independent output half circuits are used. Figure 1 shows the circuit structure of the differential amplifier with common half circuit in the left and two independent half circuits with v_{o1} and v_{o2} outputs in the right. This amplifier is used to describe the operating principle.

In the circuit of Fig. 1, I_0 is the ideal bias current source; $v_{\text{in}1}$ and $v_{\text{in}2}$ are the two input signals; V_{com} is the reference input voltage in the common half circuit; v_{o1} and v_{o2} are the two output voltages; and i_{d0}, i_{d1}, and i_{d2} are incremental drain currents of MP0, MP1, and MP2, respectively. Because I_0 is a constant current source, we have

$$i_{d0}+i_{d1}+i_{d2}=0 \ . \tag{1}$$

Because all MP0, MP1, and MP2 are in saturation, the incremental drain currents can be written as

$$i_{d0}\simeq g_{mi}(v_{\text{in}0}-v_1) \ , \tag{2a}$$

$$i_{d1}\simeq g_{mi}(v_{\text{in}1}-v_1) \ , \tag{2b}$$

$$i_{d2}\simeq g_{mi}(v_{\text{in}2}-v_1) \ , \tag{2c}$$

where g_{mi} is the input transconductance of the amplifier. From Eqs. (1) and (2), we have

$$v_1=\frac{v_{\text{in}0}+v_{\text{in}1}+v_{\text{in}2}}{3} \ , \tag{3}$$

$$i_{d0}\simeq g_{mi}\left[v_{\text{in}0}-\left(\frac{v_{\text{in}0}+v_{\text{in}1}+v_{\text{in}2}}{3}\right)\right]$$

$$=g_{mi}\left(\frac{2v_{\text{in}0}-v_{\text{in}1}-v_{\text{in}2}}{3}\right) \ , \tag{4a}$$

$$i_{d1}\simeq g_{mi}\left(\frac{2v_{\text{in}1}-v_{\text{in}0}-v_{\text{in}2}}{3}\right) \ , \tag{4b}$$

$$i_{d2}\simeq g_{mi}\left(\frac{2v_{\text{in}2}-v_{\text{in}0}-v_{\text{in}1}}{3}\right) \ . \tag{4c}$$

Because transistors MN0, MN1, and MN2 form a current mirror and hence the currents through MN1 and MN2 satisfy the relation $i_{d\text{MN}1}=i_{d\text{MN}2}=i_{d\text{MN}0}=i_{d0}$. Thus the total currents sent to the output nodes v_{o1} and v_{o2} are $i_{d1}-i_{d0}=2i_{d1}+i_{d2}$ and $i_{d2}-i_{d0}=2i_{d2}+i_{d1}$, respectively. Because the output node v_{o1} (v_{o2}) is loaded by the drain resistance of the input gates MP1 (MP2) and the load gates MN1 (MN2),

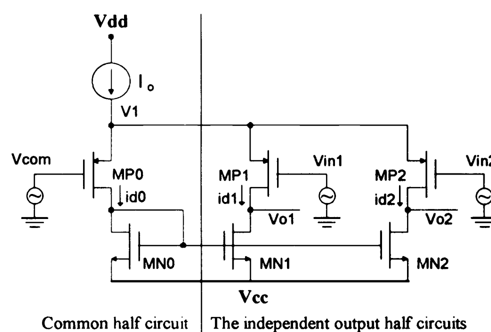

Fig. 1 Differential-input-to-single-ended-output amplifier with one shared half circuit and two individual output half circuits.

respectively, the output node voltages v_{o1} and v_{o2} can be expressed as

$$v_{o1}=g_{mi}\frac{2i_{d1}+i_{d2}}{g_{di}+g_{dl}} \ , \tag{5a}$$

$$v_{o2}=g_{mi}\frac{2i_{d2}+i_{d1}}{g_{di}+g_{dl}} \ , \tag{5b}$$

where $g_{di}(g_{dl})$ is the output conductance of the input (load) transistors MP1 and MP2 (MN1 and MN2). From Eqs. (4a) and (4b), Eqs. (5a) and (5b) can be rewritten as

$$v_{o1}=-g_{mi}\left(\frac{4v_{i1}-2v_{i0}-2v_{i2}}{3}+\frac{2v_{i2}-v_{i0}-v_{i1}}{3}\right)$$

$$=-g_{mi}\frac{v_{i1}-v_{i0}}{g_{di}+g_{dl}} \ , \tag{6a}$$

$$v_{o2}=-g_{mi}\left(\frac{4v_{i2}-2v_{i0}-2v_{i1}}{3}+\frac{2v_{i1}-v_{i0}-v_{i2}}{3}\right)$$

$$=-g_{mi}\frac{v_{i2}-v_{i0}}{g_{di}+g_{dl}} \ . \tag{6b}$$

Then the differential gains A_{dm1} and A_{dm2} are

$$A_{dm1}=\frac{v_{o1}}{v_{i1}-v_{i0}}=-\frac{g_{mi}}{g_{di}+g_{dl}}=\frac{v_{o2}}{v_{i2}-v_{i0}}=A_{dm2} \ . \tag{7}$$

It can be seen from Eqs. (6a) and (6b) that the output v_{o1} of the first half circuit is independent of the input $v_{\text{in}2}$ of the second half circuit, and similarly v_{o2} is independent of $v_{\text{in}1}$. Through the analysis, it is proved that the common half circuit of the differential amplifier can be shared by several output half circuits and the gain characteristics can be kept the same as those of a single differential amplifier, without cross-interference among several input voltages.

The input stage of the SBDI current readout scheme is shown in Fig. 2 where the original BDI circuit is separated into two parts: one is the common half circuit of the differential amplifier shared by all the detector cells and the other is the remaining circuit of the BDI, which must be included in each cell. To connect the shared half circuit with each cell,

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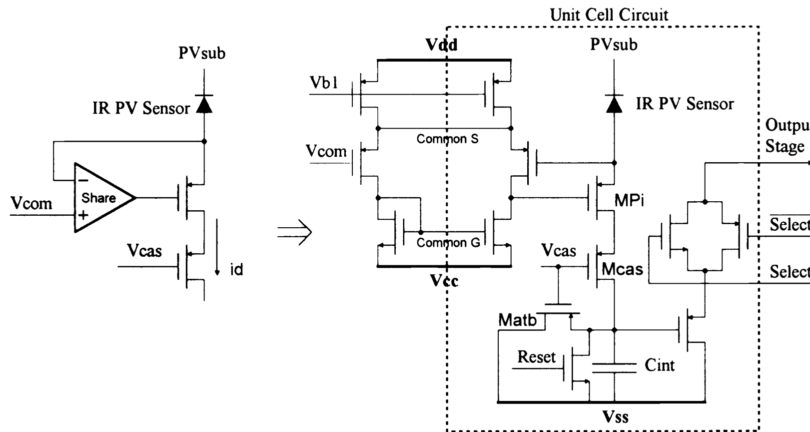

Fig. 2 Functional block diagram and complementary metal-oxide semiconductor (CMOS) circuit of the SBDI input stage.

three global lines Vb1, common S, and common G are used, as shown in Fig. 2. An extra current-source metal-oxide semiconductor (MOS) device is also used in each cell to obtain a stable source-coupled current source I_0. This device can minimize the mismatch effect and the route loading effect on the current source I_0. Totally, there are three MOS devices instead of a complete buffer amplifier in each cell to achieve the SBDI function.

In the SBDI circuit of Fig. 2, a cascade structure consisting of Mcas and MPi is used to minimize the clock feedthrough and reset signal coupling. The Matb device is an antiblooming gate to avoid the saturation condition. When the input signal current is large and the integrated voltage on the capacitor Cint approaches to $V_{\text{cas}}+|V_T|$, the MOS device Mcas would be driven into the linear region and the effect of the cascade structure would be greatly degraded. In this undesirable saturation case, Matb is turned on to bypass the input signal current and then the integrated voltage is held constant independent of the input signal current. The two complementary clock phases *Select* and $\overline{\textit{Select}}$ are applied to the transmission gate to sample the integrated voltage on C_{int} after the integration time interval T_{int}. After sampling, the *Reset* clock signal resets the capacitor immediately.

In the following, the injection efficiency, noise performance, chip area, bias stability, and threshold uniformity control of the proposed BDI structure are described in detail.

2.1 *Input Impedance and Injection Efficiency*

The main design goal of the current readout input stage of IR detectors is to achieve a high injection efficiency and low noise. The injection efficiency $\eta(s)$ and the bandwidth f_{BW} of a Di structure can be expressed as[1,6–8]

$$\eta(s)=\frac{g_m R_D}{1+g_m R_D}\left(\frac{2}{1+s/2\pi f_{\text{BW}}}\right) , \tag{8a}$$

$$f_{\text{BW}}=\frac{1+g_m R_D}{2\pi R_D C_T} . \tag{8b}$$

The injection efficiency and the bandwidth of a BDI are

$$\eta(s)=\frac{(1+A)g_m R_D}{1+(1+A)g_m R_D}\left(\frac{1}{1+s/2\pi f_{\text{BW}}}\right) , \tag{9a}$$

$$f_{\text{BW}}=\frac{1+(1+A)g_m R_D}{2\pi R_D C_T} . \tag{9b}$$

In the preceding equations, A is the gain of the buffer, g_m is the transconductance of the input gate, and $R_D(C_T)$ is the total input shunt resistance (shunt capacitance) of the IR detector. From Eqs. (8a), (8b), (9a), and (9b) it can be clearly seen that the injection efficiency $\eta(s)$ and the bandwidth f_{BW} are much improved in the BDI structure because the input impedance of the input gate MPi is reduced from $1/g_m$ to $1/(1+A)g_m$ by using an actively compensated input structure. This good injection efficiency and wide input bandwidth performance are also kept the same in the SBDI of Fig. 2 with the gain $|A_{dm}|$ in Eq. (7) substituted into the gain A in Eqs. (9a) and (9b). Typically, the gain amplitude $|A_{dm}|$ of the share-half circuit differential amplifier can be designed as 100, then the injection efficiency will be closed to 1 and the bandwidth will be almost 100-fold wider than that of the DI scheme if R_D is large enough such that $g_m R_D > 1$.

2.2 *Noise Performance*

The noise of the readout input stage should be significantly smaller than the noise produced by the IR detector and the radiation shot noise. The noise model of DI and BDI input stages can be represented by the models shown in Figs. 3 and 4, respectively. In the DI input stage, the noise generated by the input gate MOS is represented symbolically by an equivalent voltage source e_n^2 connected to its gate, as shown in Fig. 3. An IR PV sensor can be modeled as a current source I_s with the shunt capacitor C_D and the shunt resistance R_D. Then the input referred noise current of the input stage can be expressed as[9]

$$i_d^2=g_{mi}^2 e_n^2 , \tag{10}$$

$$i_{n,DI}^2=g_{mi}^2 e_n^2\left(\frac{1/g_{mi}}{R_D+1/g_{mi}}\right)^2=\frac{e_n^2}{(R_D+1/g_{mi})^2}$$

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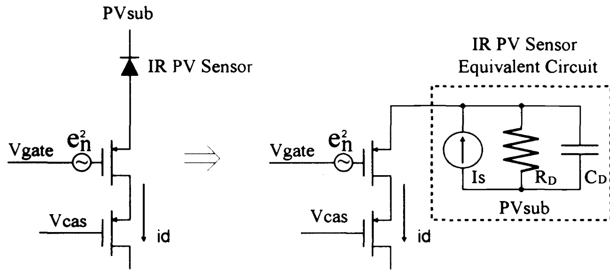

Fig. 3 Noise model and equivalent circuit of the DI input stage.

$$i_{n,DI}^2 = \frac{e_n^2}{R_D^2}\ , \quad \text{if } R_D \gg 1/g_{mi}\ , \tag{11}$$

where i_d is the drain noise current flows in the input gate generated by e_n and i_n is the input referred noise current. For low R_D detectors, the stages have a high input referred noise current, as shown in Eq. (11).

On the other hand, the input referred noise of the BDI input stage, as shown in Fig. 4, is given by the superposition of the OP input gate referred noise voltages e_{n1}^2 and the noise voltages of the input MOS devices e_{n2}^2. The input referred noise current generated by e_{n1}^2 is

$$i_{n1}^2 = \frac{e_{n1}^2}{R_D^2}\ . \tag{12}$$

The input referred noise current generated by e_{n2}^2 is

$$i_{n2}^2 = g_{mi}^2 e_{n2}^2 \left[\frac{1/(1+A)g_{mi}}{R_D + 1/(1+A)\,g_{mi}}\right]^2 \simeq \frac{e_{n2}^2/(1+A)^2}{R_D^2} = \frac{e_{n2}^2}{(1+A)^2 R_D^2}\ . \tag{13}$$

Because $R_D \gg 1/(1+A)g_{mi}$, the total input referred noise current of the BDI input stage is given by summing Eqs. (12) and (13) as

$$i_{n,\mathrm{BDI}}^2 = i_{n1}^2 + i_{n2}^2 = \frac{e_{n1}^2}{R_D^2} + \frac{e_{n2}^2}{(1+A)^2 R_D^2} \simeq \frac{e_{n1}^2}{R_D^2}\ . \tag{14}$$

The gate referred noise voltage source of a MOS field effect transistor (MOSFET) can be represented as[10]

$$e_n^2 \cong \frac{8\,kT}{3\,\mathbf{g}_m}\Delta \mathbf{f}\ . \tag{15}$$

Thus $i_{n,\mathrm{BDI}}^2$ is inversely proportional to the gate transconductance g_m. Comparing Eqs. (11) and (14), the noise reduction ratio is e_n^2(input MOS)/e_{n1}^2(OP input gate), that is, the transconductance ratio $g_{mi,\mathrm{OP}}/g_{mi,\mathrm{CG}}$ of the OP input gate and the common-gate (CG) input as applying Eq. (15) to it. The transcondutance of the MOSFET is proportional to its operating current i_d. Thus, it is apparent that a noise reduction ratio equal to the ratio of OP bias current over detector photocurrent can be obtained. Because the background photocurrent is very small, a quite small bias current of OP is enough to obtain a good noise performance.

The input referred noise current of the SBDI input stage is generally similar to that of the BDI in Eq. (14). It is apparent from Eq. (14) that the input gate-referred noise e_{n1}^2 of the OP gain stage dominated the noise performance. Thus only the input gate-referred noise e_{ni}^2 of the shared half-circuit differential pair in the SBDI scheme is analyzed. The corresponding noise model is shown in Fig. 5. To consider the noise contribution in each half circuit without confusion, the noise models of some MOS devices are expressed by the equivalent noise current source i_{nx}^2 in parallel with the drain-to-source channel, instead of the gate-referred noise voltage e_{nx}^2. The value of equivalent noise current source i_{nx}^2 is $g_{mx}^2 e_{nx}^2$, with e_{nx}^2 given by Eq. (15).

From Fig. 5 and Eq. (6a), it is seen that the output noise voltage v_{o1} is independent of the noise sources e_{n3}^2 and i_{n6}^2 of the other half circuit. Thus the noise contribution of the other half circuit stage is zero. In this case, the noise contribution of each MOS device to the output noise voltage v_{o1} in Fig. 5 can be expressed as

$$v_{o1}(e_{n1}) = A_{dm1} e_{n1}\ , \tag{16a}$$

$$v_{o1}(e_{n2}) = A_{dm1} e_{n2}\ , \tag{16b}$$

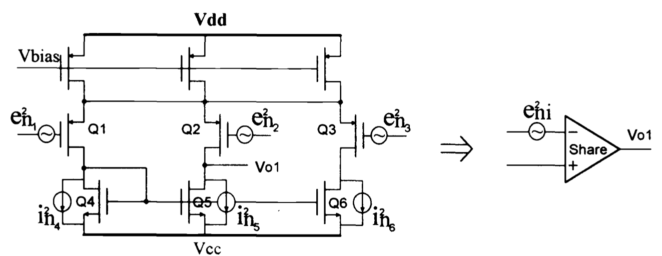

Fig. 5 Noise model and equivalent circuit of the differential pair with one shared half circuit and two individual output half circuits.

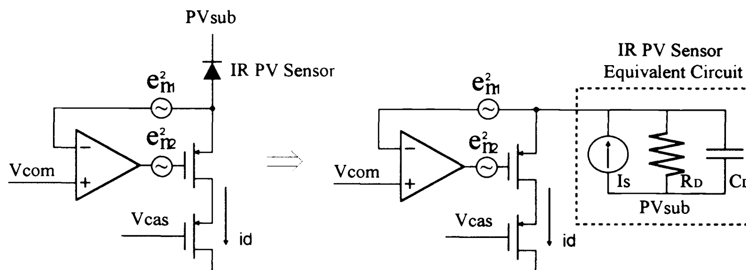

Fig. 4 Noise model and equivalent circuit of the BDI input stage.

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$$v_{o1}(i_{n4})=\frac{i_{n4}}{g_{di}+g_{dl}}=\frac{i_{n4}}{g_{d2}+g_{d5}} , \quad (16c)$$

$$v_{o1}(i_{n5})=\frac{i_{n5}}{g_{di}+g_{dl}}=\frac{i_{n5}}{g_{d2}+g_{d5}} , \quad (16d)$$

where A_{dm1} is the differential gain calculated in Eq. (7) with $g_{di}=g_{d2}$ and $g_{dl}=g_{d5}$. Because these sources are all uncorrelated, the overall mean-square output voltage v_{o1}^2 can be expressed as

$$v_{o1}^2=v_{o1}^2(e_{n1})+v_{o1}^2(e_{n2})+v_{o1}^2(i_{n4})+v_{o1}^2(i_{n5})$$

$$=A_{dm1}^2(e_{n1}^2+e_{n2}^2)+\frac{(i_{n4}+i_{n5})^2}{(g_{d2}+g_{d5})^2} . \quad (17)$$

Hence, the equivalent input noise voltage $e_{ni}=v_{o1}/A_{dm}$ has the mean-square value

$$e_{ni}^2=e_{n1}^2+e_{n2}^2+\frac{i_{n4}^2+i_{n5}^2}{g_{m2}^2}$$

$$=e_{n1}^2+e_{n2}^2+(g_{m5}/g_{m2})^2(e_{n4}^2+e_{n5}^2) , \quad (18)$$

where $g_{m4}=g_{m5}$. Hence, to minimize e_{ni}^2 and the contribution of i_{n4}^2 and i_{n5}^2, clearly g_{m2} should be much larger than g_{m5}, and this is the normal design guide for the differential input stage. Through the analysis, it is shown that the SBDI input stage can achieve a better noise performance over the DI, just as for the BDI structure.

2.3 *Power Consumption and Chip Area*

The total power consumption and unit-cell area for large FPAs are limited by practical considerations of cryogenic capability and package integrity of the IR detector systems. The conventional DI structure uses a single MOS device as the input stage and results in a low injection efficiency and low performance, although it has less power consumption and smaller chip area as compared with other readout schemes. In the BDI structure, better performance can be achieved, but the input stage of each cell requires an additional buffer. Normally, the buffer is designed as a differential pair, which requires at least five MOSFETs and an additional power dissipation $2I_d(V_{dd}-V_{cc})$, with I_d being the bias current in each half circuit. In the new SBDI structure, the input stage of each cell requires only three MOSFETs and its power dissipation is $I_d(V_{dd}-V_{cc})$. Both power dissipation and chip area of the input stage buffer of the SBDI are only half of those in the input stage of BDI. As compared with the commonly used DI readout structure, there are only three extra MOSFETs of the buffer required in each cell. This increasing chip area is still tolerable in a high-density 2-D FPA with 0.8-μm CMOS process. Thus this new SBDI readout structure offers an effective trade-off between the readout performance and the chip area consumption.

The total devices count of the SBDI unit cell is 10 MOS, as shown in Fig. 2. But it can be reduced to seven MOS devices by eliminating the cascade gate Mcas, the antiblooming gate Matb, and replacing the transmission gate by a single *p*–channel MOS (PMOS) device. Without these performance options, the basic readout circuit operation remains unchanged. With the same basic operation, the DI structure requires four MOS devices in total, whereas the BDI structure nine MOS devices. In applying the SBDI to the 2-D FPA, the chip area can be further reduced by using a high-density capacitor process or the shared capacitor design technique.

In a hybrid focal plane, the detector elements and the readout signal processor are fabricated on separate semiconductor substrates and then joined together using the array-bonding technique. The cell chip area of the current readout CMOS circuit in such a hybrid focal plane is limited to that of one single detector with a bonding pad. Thus, the complex buffer circuit used in the BDI is not allowed in such a 2-D application with strict size limitation. Because the new SBDI input stage has low power dissipation and small chip area, it can be used in the hybrid FPA.

In addition to high injection efficiency, good noise performance, small area size, and low power dissipation, good bias stability and threshold control are inherent in the SBDI structure as well as in the BDI structure. The detectors should be kept near zero bias to prevent the generation of $1/f$ noise and maintain linear and uniform response. The virtual short-circuit property between the two differential-pair OP input nodes in the SBDI structure makes the detectors biased at near zero bias.

Usually, strict threshold uniformity is required for an IR FPA sensor. Because the threshold voltage variation in the DI input gate is directly coupled to the detector bias point, control of the FPA's readout uniformity is difficult under the process variations. This problem can be solved by the SBDI feedback amplifier structure. The threshold variation range of the feedback amplifier is equal to the random offset level of the OP amp. This is enough to satisfy the operational requirements dictated by IR detectors.

3 Dynamic Discharge Source-Follower Output Stage

The output stage of a current readout circuit is also used as an unit-gain buffer and is usually implemented by source followers. As shown in Fig. 6, the signal voltage from each cell is sampled through the source follower by clocking the appropriate switches. The cascaded two stages of the source followers constructed by MP2 ~ MP5 are used to drive the output load under high readout frequency. Because large charging and discharging currents through the output load are required to satisfy the requirements of frame rate and readout speed, the power dissipation of the output stage dominates that of the whole IR current readout circuit.

The function of this conventional source-follower output stage is described in the following. After the cell $(n-1)$ readout operation is completed, node B is reset to a low level, which is usually $(V_{SS}+V_{gs(\mathrm{MP2})})$ and V_{out} is reset to $(V_{SS}+V_{gs(\mathrm{MP2})}+V_{gs(\mathrm{MP4})})$. Then, before the sample-to-output operation of the cell (n), the voltage at node A is the integrated signal voltage, which is usually a high level because of the integration of the input background current. In the sampling phase, *Select* is high and the transmission gate is on. At this time, MP2 is off because $V(A)>V(B)$. But node B is gradually charged toward $V(\mathrm{signal})+V_{gs(\mathrm{MP2})}$ by the constant current through MP3. In the reset phase, *Reset* is high and $V(A)$ is discharged to V_{SS} immediately. Thus, there is a large drop between nodes A and B, which causes

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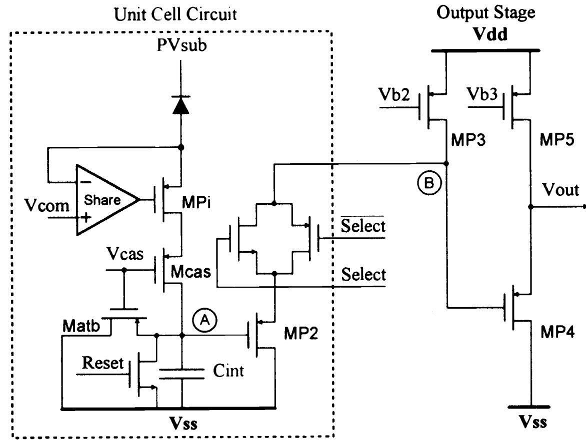

Fig. 6 Conventional PMOS cascaded source-follower output stage.

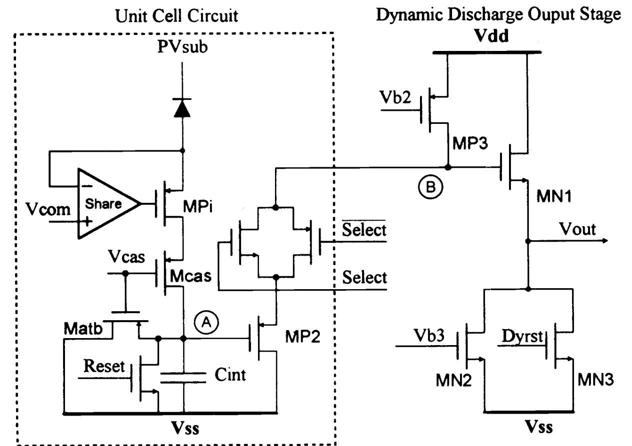

Fig. 7 Dynamic discharge output stage with the level shifter.

MP2 and then MP4 to sink a large current and discharge the output node quickly. In this output stage, the speed is limited by the constant charging current generated by V_{b3} and MP5, whereas the standby power dissipation is also determined by the constant charge current. A trade-off exists between power dissipation and readout frequency. The mentioned speed limit can be overcome by using a dynamic discharge source-follower output stage with only dynamic power dissipation.

The dynamic discharge output stage, which is composed of a PMOS level shifter and an *N*-type MOS (NMOS) source follower with the dynamic discharge gate MN3 is illustrated in Fig. 7. The function of the dynamic output stage in the charging and reset phases is shown. In the charging phase, node *B* of the output stage is preset to a low level in the last cell reset phase. At this time, node *A* has a signal level of $V(A)$. When the control signal *Select* is high, signal *A* is sampled to the output stage and node *B* is charged to $V(A)+V_{gs(\mathrm{MP2})}$ quickly because it is only loaded by the switch transistors and the gate capacitance of MN1. The high voltage at node *B* leads to a low V_{out} in the sample moment. Then there is a large voltage drop between gate and source nodes of MN1, which generates a large charging current to charge the output load to $V(B)-V_{gs(\mathrm{MN1})}$ quickly. In the reset phase, node *A* is discharged to V_{SS} through the reset switch and node *B* is discharged to $V_{SS}+V_{gs(\mathrm{MP2})}$ immediately. At this time, V_{out} is pulled to a low voltage of $V_{SS}+V_{gs(\mathrm{MP2})}-V_{gs(\mathrm{MN1})}$ by the constant current of MN2 and the extra dynamic discharge gate MN3 controlled by the clock $D_{y\mathrm{rst}}$. Because $D_{y\mathrm{rst}}$ is high when *Reset* is high, the output voltage is discharged to low through MN3 in every reset phase. This achieves a high readout speed without any extra static power dissipation. The dynamic discharge NMOS source follower can be applied to both *n*-on-*p* and *p*-on-*n* types of detectors that have the reset-to-low operation and the high signal output level in the output stage.

The maximum integrated voltage on C_{int} in each cell is constricted to V_{int} in the conventional PMOS cascaded source followers output stage in Fig. 6. To cause all the MOS transistors to work in the saturation region, the maximum output voltage should obey

$$V_{\mathrm{out}}\leq V_{dd}-|V_{d\mathrm{sat(MP5)}}| \ , \tag{19}$$

where $V_{d\mathrm{sat(MP5)}}$ is the saturation voltage of MP5. Thus, the maximum integrated signal level V_{int} is consticted to

$$V_{\mathrm{int}}\leq V_{dd}-|V_{d\mathrm{sat(MP5)}}|-|V_{gs(\mathrm{MP4})}|-|V_{gs(\mathrm{MP2})}| \ , \tag{20}$$

because

$$v_{\mathrm{out}}=V_{\mathrm{int}}+|V_{gs(\mathrm{MP2})}|+|V_{gs(\mathrm{MP4})}| \ . \tag{21}$$

Because the dc drain current of MP4 is equal to that of MP5, which must be large enough to charge/discharge the output load, the voltage $V_{gs(\mathrm{MP4})}$ is large. As can be seen from Eq. (20), the maximum signal integrated voltage is seriously degraded and results in a low dynamic range. The case is even worse under cryogenic operation with a larger threshold voltage than that under room-temperature operation.

In the dynamic discharge output stage, as shown in Fig. 7, a large integration capacity can be achieved by using a complementary type of cascaded source followers. The maximum output voltage V_{out} and the integrated signal voltage V_{int} are

$$V_{\mathrm{out}}=V_{\mathrm{int}}+|V_{gs(\mathrm{MP2})}|-V_{gs(\mathrm{MN1})}\leq V_{dd}-V_{d\mathrm{sat(MN1)}} \ , \tag{22}$$

$$V_{\mathrm{int}}\leq V_{dd}-V_{d\mathrm{sat(MN1)}}-|V_{gs(\mathrm{MP2})}|+V_{gs(\mathrm{MN1})} \ . \tag{23}$$

Equation (23) shows that the maximum input signal integrated range is increased without the degradation by the output stage. This structure can also achieve an almost zero dc offset by properly tuning the voltages $|V_{gs(\mathrm{MP2})}|$ and $V_{gs(\mathrm{MN1})}$. Note that the smallest voltage V_{out} must obey the condition

$$V_{\mathrm{out}}\geq V_{d\mathrm{sat(MN2)}} \ , \tag{24}$$

where $V_{d\mathrm{sat(MN2)}}$ is the saturation voltage of MN2. To achieve the minimum V_{out}, one can choose

$$|V_{gs(\mathrm{MP2})}|=V_{gs(\mathrm{MN1})}+V_{d\mathrm{sat(MN2)}} \ , \tag{25}$$

In this case, V_{out} is minimum without losing the low-background signal. Through the analysis, it is seen that the dynamic discharge output stage with complementary cascaded source followers can improve the dynamic range and overcome the speed limit of the conventional output stage at the small cost of increasing the dynamic power dissipation.

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The additional clock control can be shared with the CDS stage, as shown in Fig. 8, which can eliminate the $1/f$ noise of multiplexer and output stage.[8,11–13]

4 Simulation and Experimental Results

Figure 9 is a block diagram of a $N\times 1$ scanning array readout circuit using SBDI technology. It is composed of an analog signal processing unit and a digital clock control unit. The PV sensors are connected to the readout chip through bonding pads. The bias circuit can be implemented on chip or off chip. The difference between common voltage V_{com} and photodetector substrate bias PV_{sub} deference determines the bias condition of detector. These can be connected together to achieve a zero bias. There is an optimum voltage V_{com} to achieve the largest integrated capacity while keeping the amplifier operating properly. Those voltages marked with * are optional, depending on different applications.

Because this readout chip is of mixed-mode circuits, some design techniques are used to offer good shielding between digital part and analog part. First, the whole n-substrate is biased by the analog power supply AV_{dd} to avoid the noise coupling effect from the digital power supply to the substrate. In addition to this, analog and digital power supplies should be separated to avoid the digital noise resulting from the dynamic switching current of logic gates from being coupled to the analog part.

SPICE simulation results of the SGDI current readout with input signals 5, 50, and 100 nA and the maximum input background capacity 130 nA, are shown in Fig. 10. The output voltage waveforms at the node V_{out} of Fig. 7 is shown in Fig. 10(a). The static current in the PMOS level shifter is shown in Fig. 10(b), where less 20 μA is needed and the static power dissipation is small. The dynamic charging and discharging waveforms of the NMOS source follower are shown in Fig. 10(c). It is clearly seen that this output stage consumes only dynamic power and the total average power dissipation is small. As shown in the simulation results, 1-MHz readout frequency can be achieved with a power dissipation below 10 mW at a 25-pF output loading and 10-V supply. Evidently, the summation of the output charging time and reset time in Fig. 10(a) is less than 500 ns, that is, the readout speed performance could be as high as 2 MHz.

Several experimental circuits were designed and fabricated to verify this new CMOS readout circuit. Photographs of 8×1 and 64×1 SBDI experimental readout chips that were fabricated in 3-μm double-poly single-metal p-well CMOS process are shown in Figs. 11(a) and 11(b), respectively. An off-chip test current source is used to simulate the photocurrent of the IR detector and the experimental results are shown in Fig. 12 with different input currents in the first four cells and the same input current in the last four cells. The measured readout speed is 500 kHz, which is smaller than the simulated speed of 2 MHz. The charging speed decrease is caused by the inevitable extra load capacitance of the test environment, which is much larger than the normal load capacitance of the designed readout chip.

The measured current voltage (I-V) relationship results with the input current range from 50 to 120 nA by a 5-nA step are shown in Fig. 13. It is seen that the linearity performance of this chip can be larger than 98%. The voltage

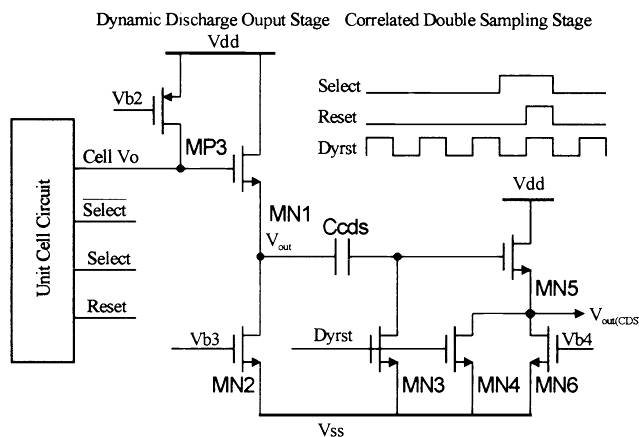


Fig. 8 CDS output stage with the control clock D_{yrst}.

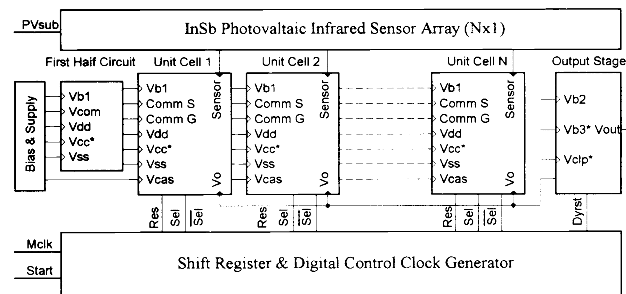
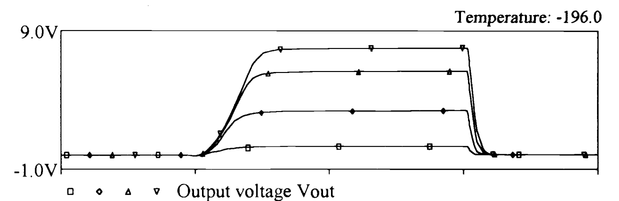
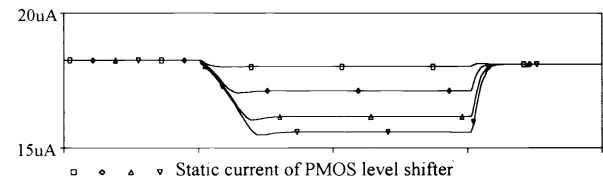


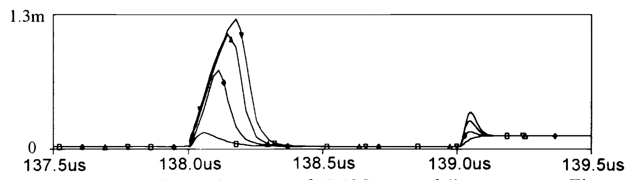
Fig. 9 Complete block diagram of a $N\times 1$ SBDI readout circuit.



(a)



(b)



(c)

Fig. 10 SPICE transition simulation results of the SBDI readout circuit with input signal currents 5, 50, 100, and 130 nA (saturation): (a) waveforms of the output voltage V_{out}, (b) current flows in the NMOS source follower, and (c) current flows in the PMOS level shifter.

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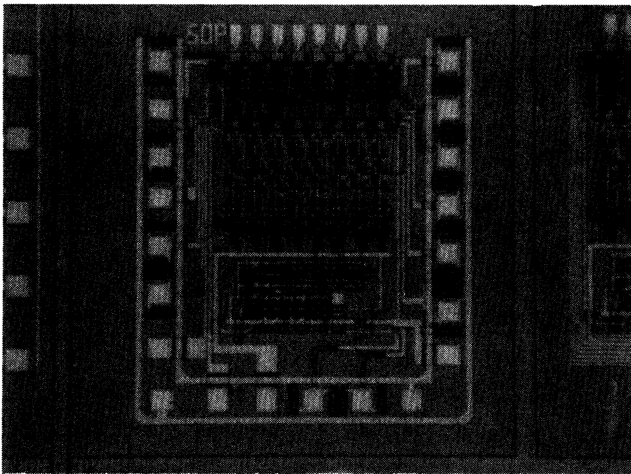
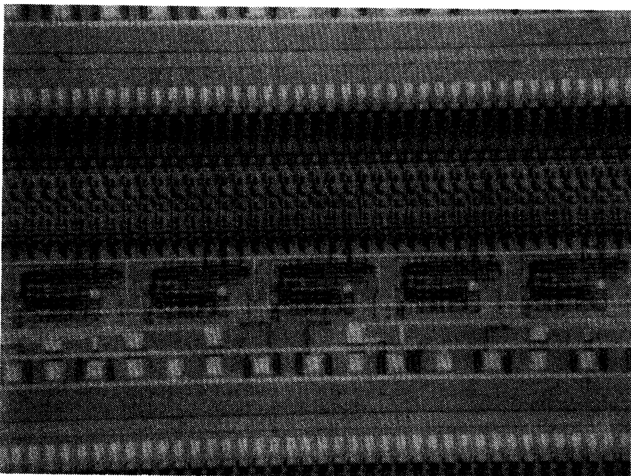


(a)



(b)

Fig. 11 Chip photographs of (a) 8×1 and (b) 64×1 SBDI IR readout chips.

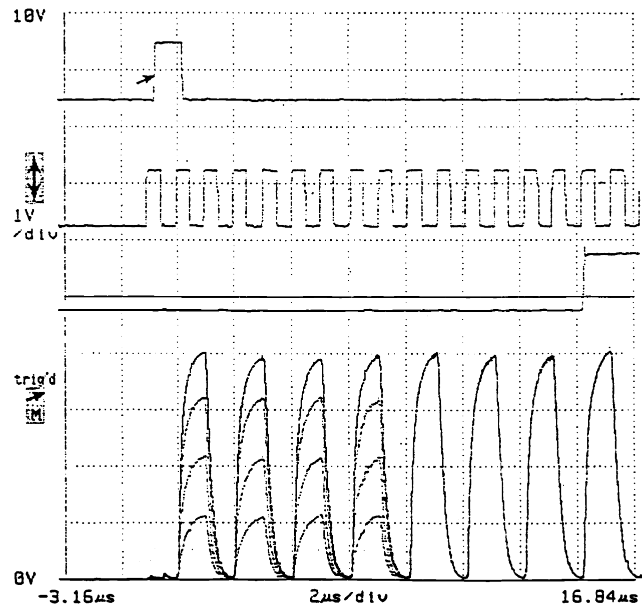


Fig. 12 Measured output waveforms of the 8×1 SBDI readout chip with off-chip input current sources supplying the first four cells with four different input currents and the last four cells with constant input currents.

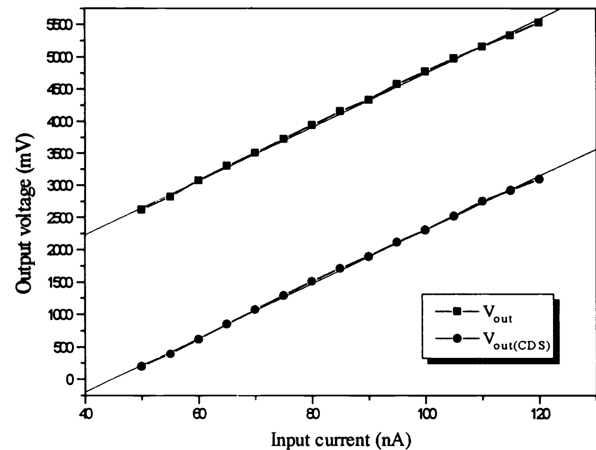


Fig. 13 Output voltage V_{out} and CDS output voltage $V_{out(CDS)}$ versus different input currents from 50 to 120 nA in 5-nA steps.

between V_{out} and $V_{out(CDS)}$ is the sum of the voltage on capacitor C_{cds} and the gate-to-source voltage drop V_{gs} of the unit gain buffer in Fig. 8, which is implemented by MN5 and MN6, an on-chip NMOS source follower. The uniformity of an 8×1 readout test chip with off-chip current input is shown in Fig. 14. The uniformity performance, although limited by the off-chip current source data resolution, is expected to be better than 99%. The total test performance of the SBDI readout chip is summarized in Table 1. The readout speed is dependent on the integration interval and the frame rate. A higher readout frequency is not necessarily for the 1-D scanning array but is useful for the 2-D application. Three (0-, 5-, and 10-V) or two (0- and 10-V) power supplies are optional, depending on the power dissipation and chip area considerations. An additional power supply (5 V) used by the shared half-circuit differential pair can decrease the power dissipation and the chip size of the buffer in every cell. The power dissipation in Table 1 is calculated without considering the static power dissipation of the bias circuits.

5 Summary

In this paper, a new SBDI current readout input stage and a dynamic discharge complementary cascaded source-follower output stage for IR detectors are proposed and analyzed. This new CMOS current readout structure uses a share half-circuit differential pair technique to implement a buffer with only half power dissipation and chip size as compared with the conventional BDI structure. It has been shown that the new current readout circuit has high injection efficiency, low noise, small chip size, low power dissipation, good threshold uniformity, high readout speed, and stable cryogenic temperature operations. Moreover, this new readout technology can be applied to FPA design and a high-performance 2-D

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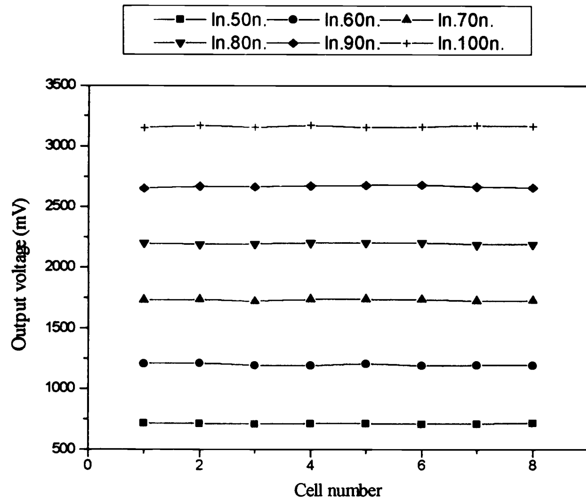

Fig. 14 Uniformity of the 8×1 SBDI readout chip with different input currents from 50 to 100 nA.

Table 1 Test results and operation conditions for the SBDI current readout structure.

Parameter	Results
Power supply	0-5-10V or 0-10V
Max. Photo-current	130 nA
Max. Readout speed	500k Hz
Integration capacitance	> 2 pF
Storage capacity	$> 1.0 \times 10^8 e^-$
Transimpedance	> 40 MΩ
Power dissipation	< 10 mW
Linearity	>98%
Anti blooming control	yes
Operation temperature	77° k

readout is achievable. The function and performance of this new SBDI readout structure are partly verified by experimental chips.

Acknowledgments

We would like to acknowledge the support and help of Sheng-Jen Yang, Tai-Ping Sun and Far-Wen Jih. This research was supported under the contract with the Chung Shang Institute of Science and Technology.

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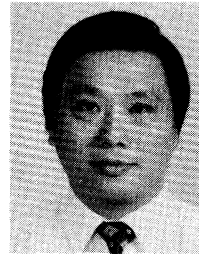

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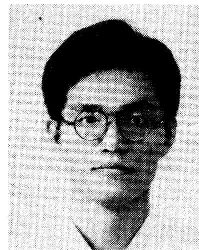

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