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Evaluation of Temperature Stability of Trilayer Resistive Memories Using Work-Function Tuning

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A trilayer resistive memory with a low picojoule switching energy shows highly uniform current distribution, fast switching speed of 10 ns, and robust endurance cycling of 10^6 cycles under high-temperature (343 K) operation. Such good performance is related to high-temperature stable Ni electrode, fast electron hopping via nanocrystallized anatase TiO_2, and nonuniform electric-field distribution to dilute cycling stress. The evaluation of thermal stability is mandatory for the application of reliable high-density three-dimensional nonvolatile memory.
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The resistive random access memory (RRAM) provides a potential solution for down-scaling beyond charge-trapping flash nonvolatile memory at sub-20 nm nodes.[1–11] The RRAM also has a small cell size, large memory window for multiple-level cell operation, and three-dimensional (3D) integration capability. To realize resistive bistability, non-stoichiometric transition metal oxides have been used for RRAM, but these devices usually suffer from the high set/reset currents and present unstable resistance switching at high-temperature operation. To address these issues, we previously reported ultra low-power RRAM using a covalent bond oxide/metal oxide of $GeO_x/SrTiO_3$,[10,12] where the performance improvement is related to the low vacancy control in dielectric using O_2/Ar. Although a low set current ($<5\,\mu$A) has been reported in bilayer $GeO_x/SrTiO_3$ RRAM,[10] further improving the switching uniformity close to existing flash memory and high-temperature endurance cycling are still required for reliable 3D memories. In this work, we further improve the temperature instability on switching uniformity and endurance characteristics of RRAM using trilayer-structured dielectrics and high-work-function electrodes. The nanocrystallized TiO_2 (nc-TiO_2) with anatase phase has been used for high-density DRAM capacitor, where the anatase TiO_2 has the merit of lowering the thermal budget to <400 °C for VLSI backend integration.[13] Such defect-rich and narrow-bandgap TiO_2 dielectric is important to reach fast switching and robust endurance at high-temperature operation.

The RRAM devices were integrated into a VLSI backend for an embedded memory application. First, a 200-nm-thick backend SiO_2 was formed on the Si substrates. Then, 100 nm TaN was deposited by sputtering. After patterning the bottom TaN electrode, the 25-nm-thick TaON film was deposited by sputtering in a gas mixture with 10% O_2 and 5% N_2 in Ar ambient. After film deposition, the amorphous TaON was followed by oxygen annealing at 400 °C for 10 min. Subsequently, the 17-nm-thick TiO_2 film was deposited by sputtering in a gas mixture with 5% O_2 in Ar ambient on the TaON/TaN. Then, the TiO_2 film was annealed at 400 °C for 5 min to form crystallized TiO_2, where the crystallinity of TiO_2 (nanocrystallized anatase TiO_2) was confirmed by transmission electron microscopy (TEM) and X-ray diffraction (XRD). Following that, a 6-nm-thick GeO_x was deposited by e-gun evaporation to finish the trilayer dielectrics of the GeO_x/TiO_2/TaON. Finally, a 50-nm-thick Ni was deposited and patterned to form the top electrode. The fabricated devices were characterized by current–voltage (I–V), switching distribution, switching speed, and endurance measurements using an Agilent 4156 semiconductor parameter analyzer and 81110 pulse generator.

The high-temperature leakage improvement has been demonstrated by high-work-function metals in DRAM capacitors.[13,14] To understand the effect of metal work-function tuning in RRAM, we fabricated two trilayer RRAM devices with different top electrodes (TEs) of Pt (work function ~5.63 eV) and Ni (work function ~5.1 eV) for a resistance switching comparison. Figure 1(a) shows the swept I–V characteristics of trilayer GeO_x/nc-TiO_2/TaON RRAM devices with different TEs. The trilayer RRAM with Ni TE can be set or reset to low- or high-resistance state (LRS or HRS) by 4.6 µA at 5 V or 0.3 µA at −6 V, respectively. Two-orders-of-magnitude HRS/LRS is measured at a read voltage of 0.5 V. However, the lower set/reset voltages conditions (2.2 µA at 3 V for set; 46 nA at −2 V for reset) are reached in RRAM with a high-work-function Pt TE. The result clearly explains that the reset voltage and current can be further lowered by using a Pt electrode with a high-work-function tuning, which leads to a large band bending for fast reverse-biased reset. Besides, the low-self-compliance LRS current can only be reached by the trilayer GeO_x/nc-TiO_2/TaON dielectric, not a single-layer nc-TiO_2. This is because the nonuniform electric-field distribution within our designed MIM structure provides a large internal resistance for hopping conduction in LRS.[10–12] The uniform switching characteristic is required for robust endurance. Because of the different switching margins in HRS/LRS for two RRAM devices, the coefficient of variation (CV) was used to evaluate the distribution. The CV is a normalized measure of dispersion of a probability distribution that is defined as the ratio of the standard deviation to the mean value. The RRAM devices were examined via a dc pulse of 60 µs using a 4156 analyzer for the in situ observation of current distribution. Figure 1(b) shows the measured current distribution of RRAM devices with different electrodes under 60 µs set/reset, which performs very wide current distributions for LRS (CV = 131%) and HRS (CV = 43%) in the RRAM device with Pt TE. In sharp contrast, very tight distributions for LRS (CV = 36%) and HRS (CV = 13%) are found in the RRAM device with Ni TE. It is suggested that the interface roughness effect in Pt/GeO_x affects the

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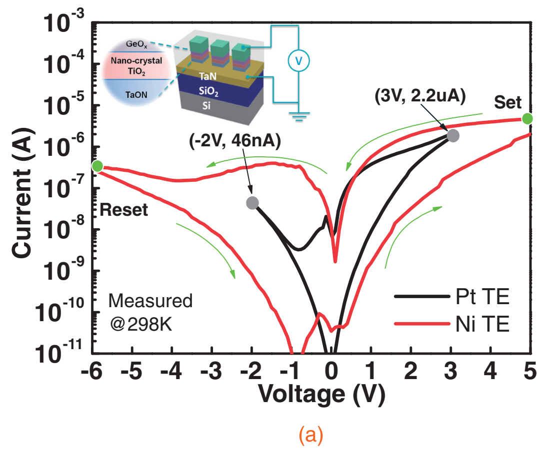

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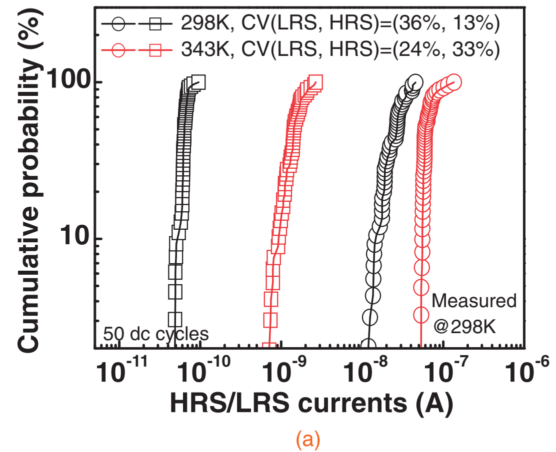

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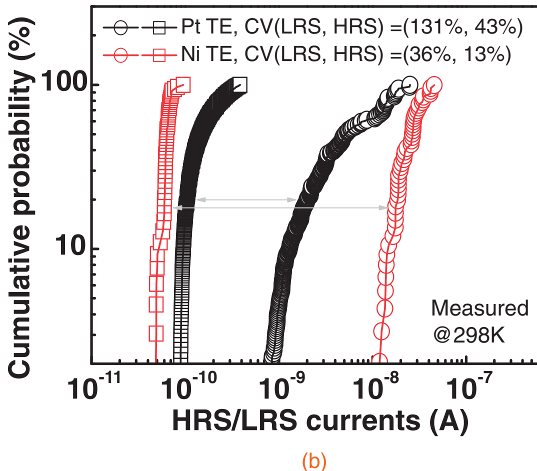

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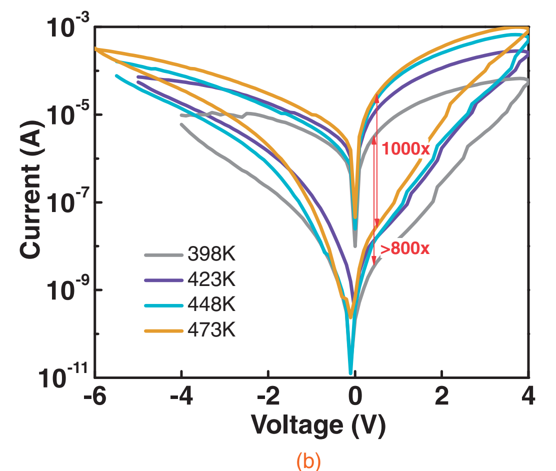

(b)

Fig. 1. (a) Measured swept I–V curves and (b) current distribution of trilayer RRAM with Pt and Ni top electrodes. The inset shows the schematic illustration of the formed [Pt or Ni]/GeO_x/nc-TiO_2/TaON/TaN RRAM. The arrows indicate the bias sweeping directions.

Fig. 2. (a) Current distribution and (b) swept I–V curves measured from 398 to 473 K in trilayer RRAM with Ni top electrode.

draft of atomic-scale oxygen vacancy and thereby results in an unstable LRS switching since the rms roughness of Pt (0.84 nm) is much higher than that of Ni (0.44 nm). Furthermore, the excellent switching uniformity is directly linked to the low-power operation with low-self-compliance set/reset currents since a high forming voltage and a large set current in conventional unipolar RRAM can result in an additional defect increase to widen the HRS/LRS distributions.[15–18)]

Figure 2(a) shows the high-temperature current distribution of the trilayer RRAM with Ni TE. Although the HRS distribution at 343 K (CV = 33%) is slightly poorer than that at 298 K, better uniformity (CV = 24%) in LRS at 343 K indicates a stable set process at high-temperature operation. It is worth noticing that the Ni/GeO_x/TiO_2/TaON/TaN RRAM exhibits resistive switching characteristics at very high temperature, from 398 to 473 K, as shown in Fig. 2(b). The increased HRS/LRS currents with elevated temperature still can maintain a large HRS/LRS ratio of 1000 at 473 K. It is well known that the vacancy concentration is further increased with elevated temperature, especially for narrow-band-gap nc-TiO_2,[19,20)] which may be responsible for the high-temperature HRS/LRS currents.

The switching speed is a key factor for RRAM. In Fig. 3(a), the set pulse width dependence of HRS/LRS ratio was examined using various set pulse widths. The input and output voltages can be extracted and inspected via a simple circuit consisting of a pulse generator, an oscilloscope, and RRAM with a fixed external resistor, as shown in the inset. To optimize the HRS/LRS ratio, the reset pulse width was fixed at 100 ns to ensure that the LRS could be recovered to HRS with an overdrive reset voltage. The change in the HRS/LRS ratio with varied pulse widths indicates that this RRAM device can be triggered by even ultra short pulse width (5 ns) for resistance-state change. Figures 3(b) and 3(c) plot schematic illustrations of pulse-triggered set and reset processes. The schematic band gaps of GeO_x, TiO_2, and TaON are 5.8, 3.05, and 4.4 eV, respectively.[21,22)] The width of the space charge region (W_{sc}) shown here denotes that a change in the charge density can induce a corresponding change in the width. Apparently, the large-band-gap GeO_x and TaON can provide a larger conduction band offset corresponding to nc-TiO_2 and a higher potential barrier in contact with top and bottom electrodes, which effectively reduce leakage paths originated from narrow-band-gap nc-TiO_2 and thus lower HRS current. In Fig. 3(d), the activation energies (E_a) obtained from the Arrhenius plot for HRS and LRS are estimated to be 0.51 and 0.37 eV, respectively. The resistance switching can be attributed to the change of activation energy between HRS and LRS. The high E_a in HRS is expected to be determined by the nature

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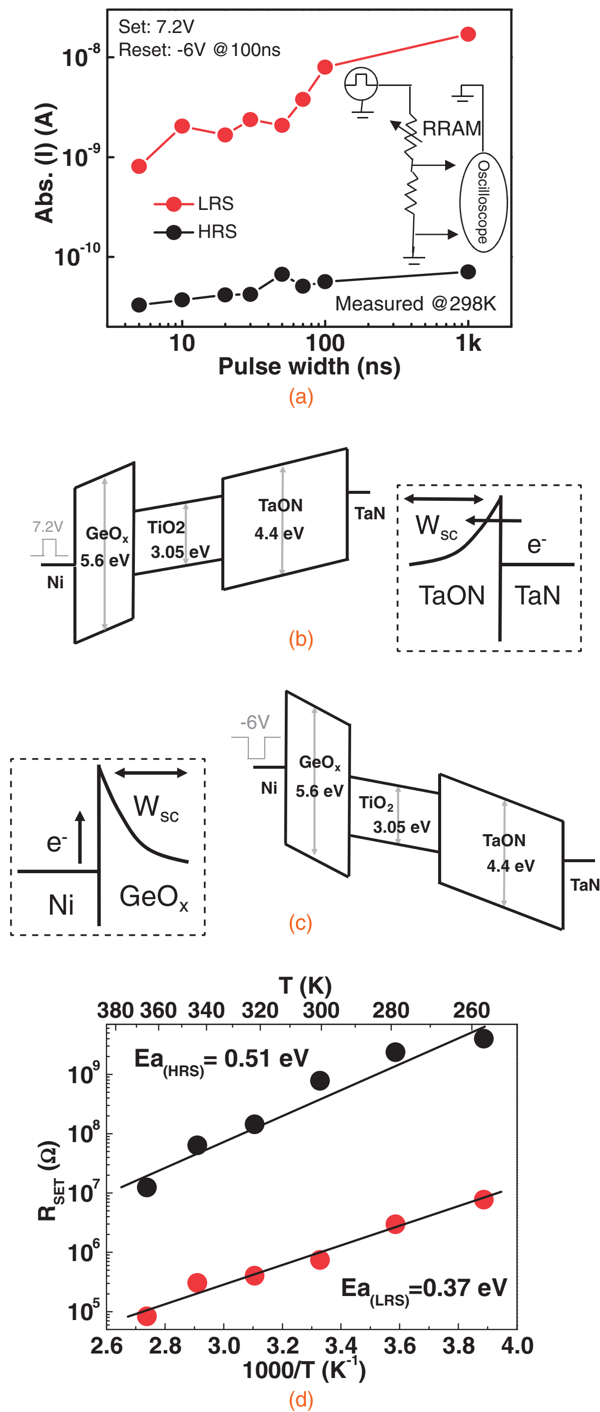
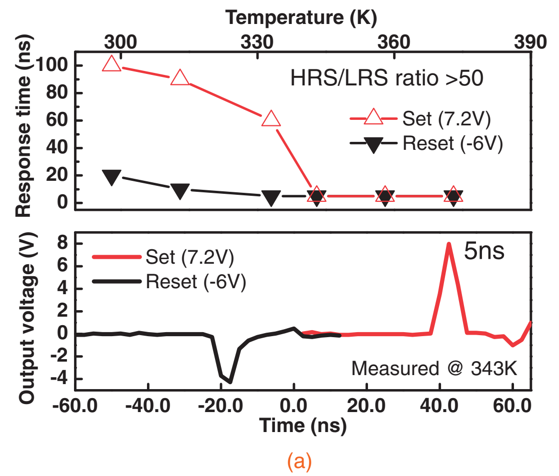


Fig. 3. (a) Pulse width dependence of HRS/LRS ratio and schematic schemes for resistive switching under (b) set and (c) reset operations of trilayer RRAM. (d) The extracted activation energies in HRS and LRS. The inset of (a) is the RRAM circuit for pulse response measurement.

of bulk defects distributed across the stacked dielectric. The low E_a of 0.37 eV in LRS is close to that of defective silicon ruled by hopping conduction.[12] Furthermore, a similar resistance 10^6–10^8 Ω cm resistivity and a negative temperature coefficient were also reported in the defective silicon,[12] suggesting that the switching behavior in LRS is related to electron hopping via defects. The hopping conduction has been proposed for resistive switching and also demonstrated in reported RRAMs using defective dielectrics including AlO_x,[23] ZnO,[24] WO_x,[25] TiO_x,[26,27]



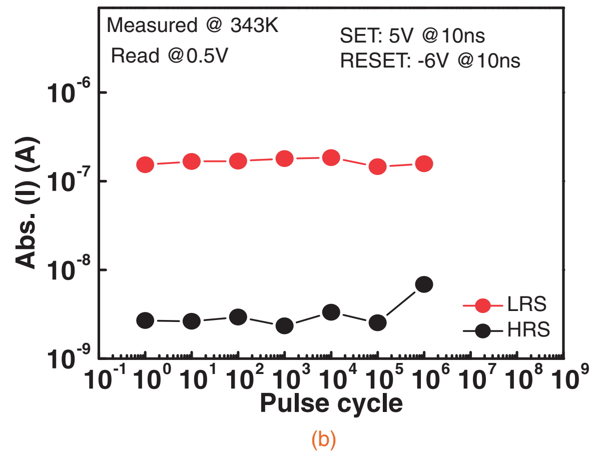


Fig. 4. (a) Temperature-dependent response time (top) and response waveforms to 5 ns pulse (bottom) and (b) 10-ns-pulsed endurance characteristics measured at 343 K.

TaO_x,[28] ion-doped ZrO_2,[29] and stacked HfO_x/AlO_x.[30] The switching mechanism can be explained as follows. The energetic electron hops through the potential barrier at the TaN/TaON interface to form a low-self-compliance LRS current as a positive set pulse is applied. In contrast, the injected electrons from the top Ni can break the hopping conduction pass and recover to HRS due to the large potential barrier across the high-work-function Ni and large band gap GeO_x after giving a reverse pulse. Therefore, the hopping behavior should be determined by total dielectric stack. However, the change in space charges (space charge capacitance) near electrodes with biasing field can contribute to hopping resistance, which may influence the magnitude of the self-compliance LRS current.

We also measured the temperature dependence on response time as shown in Fig. 4(a). Considering fixed set (7.2 V) and reset (−6 V) pulsed voltages, switching times of 100 and 20 ns are required for the set and reset to reach a large resistance ratio >50, respectively. However, the switching speed is faster at higher temperatures, where only the 5 ns set and reset times can be reached at a temperature of 343 K. This may be due to the higher thermal energy at higher temperatures for easier hopping conduction. The bottom figure in Fig. 4(a) shows the output voltage response of RRAM. A fast response time of 5 ns is measured at applied over stressed set/reset pulses of 7.2 and −6 V, where

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the distorted output waveform is due to the parasitic capacitance and resistance from wire bonding. Such fast switching capability is only measured in the Ni/GeO_x/TiO_2/TaON/TaN RRAM with nc-TiO_2 but not amorphous TiO_2 devices, where the anatase TiO_2 with native shallow-level defects may contribute to superior electron transport for this fast resistive switching.

Figure 4(b) shows the measured endurance characteristics at a high temperature of 343 K under a set pulse of 5 V and a reset pulse of −6 V at a switching speed of 10 ns. The robust endurance of 10^6 cycles for 10 ns pulse is obtained and also can maintain a resistance window of >10 after 10^6 cycles at picojoule switching energy. Since high-temperature leakage is strongly related to the presence of bulk vacancies in the RRAM device, good high-temperature uniformity $\geq 10^5$ cycles obtained at 10 ns switching is also a strong merit of this trilayer RRAM device. Such robust high-temperature endurance is ascribed to the high-work-function electrode to lower the high-temperature leakage, fast switching speed of 10 ns caused by easy hopping via grain boundaries, and high-κ nc-TiO_2 to reduce the electric field stress over GeO_x and TaON under a low picojoule switching energy. The grain boundaries have high grain boundary defects that in turn allows the hopping conduction pass to form via grain boundaries at a lower set power.

In conclusion, using a high-work-function electrode and a trilayer resistive switching dielectric, the low-power trilayer RRAM shows highly uniform switching, fast 10 ns speed, and robust endurance of 10^6 cycles at a high temperature of 343 K.

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