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Achieving low sub-0.6-nm EOT in gate-first *n*-MOSFET with TiLaO/CeO_2 gate stack

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ABSTRACT

We report a gate-first TiLaO/CeO_2 *n*-MOSFET with an equivalent oxide thickness (EOT) of only 0.56 nm and threshold voltage (V_t) of 0.31 V. This small EOT MOSFET was achieved by employing high-κ CeO_2 interfacial layer with high bond enthalpy (795 kJ/mol) to replace low-κ SiO_2 with close bond enthalpy (800 kJ/mol). The cerium silicate can aggressively scale EOT down to sub-0.6-nm EOT region without increasing gate leakage, which is urgently needed for 16 nm technology node.

1. Introduction

Recently, a major challenge for metal-gate/high-κ CMOS [1–13] is to trade off equivalent oxide thickness (EOT) and flat-band voltage (V_{fb}) roll-off at a CMOS-compatible gate first process, since the large V_{fb} roll-off [7,8] at smaller equivalent oxide thickness (EOT) is undesirable, which can result in an unwanted high threshold voltage (V_t). Previously we have shown that the V_{fb} roll-off and the high V_t are related to charged-oxygen vacancies in the non-stoichiometric oxides (HfO_{2-x} and SiO_x) [7,8]. The vacancy-rich interfacial layer not only leads to V_{fb} roll-off and high V_t, but also largely increase gate leakage current at a sub-nm EOT region. Although an ultra-thin SiO_2 layer can be used as interface layer between high-κ dielectric and Si to reach a 1 nm EOT [9] in the 45 nm node technology, this may not work as the gate-stack technology is highly scaled down to sub-0.6-nm EOT for 16 nm technology node. To solve these issues, we proposed a stacked gate dielectric using higher-κ TiLaO [14] and large-bandgap cerium oxide (CeO_2) interface layer with bond enthalpy (795 kJ/mol) close to that of the SiO_2 (800 kJ/mol) [3] for aggressive EOT scaling. Since the TiO_2-based dielectrics in direct contact with Si substrate always accompany common shortcoming of poor interface quality, the robust cerium-based silicate to improve the interface thermal stability become more urgent.

In this paper, TiLaO/CeO_2 *n*-MOSFET using silicate interface modification to obtain a small 0.56 nm EOT and a low V_t of 0.31 V have been demonstrated. The *n*-MOSFET with highly scaled EOT can be attributed to the combined results of an increased capacitance density using higher-κ TiLaO gate dielectric, low gate leakage and robust cerium-based silicate interface.

2. Experimental procedure

Standard p-type Si wafers were used in this study. The simple, self-aligned, gate-first TaN/TiLaO/CeO_2 *n*-MOSFETs were made by depositing TiO_2-doped La_2O_3 (~25% TiO concentration) on Si substrate using electron beam (e-beam) evaporation, followed by a post-deposition anneal (PDA) of 400 °C. The low-temperature physical-vapor disposition [3–8,13,14] have less interface reaction compared to sputtering with plasma damage or high-temperature chemical-vapor disposition. The adding TiO_2 in TiLaO increases the dielectric constant (κ value), which allows using a thicker layer to decrease the gate leakage without scarifying gate capacitance density to reach small EOT. Then 150-nm-thick TaN were subsequently deposited on these gate stacks and RTA annealed at 550–900 °C to form the MOS capacitors. For comparison, the same MOS process was also used to fabricate other TaN/TiLaO/Al_2O_3/p-Si *n*-MOS capacitors. After patterning, self-aligned As^+ implantation with an acceleration voltage of 25 KeV and a dosage of 5×10^{15} cm^{-2} for source-drain doping was applied and activated at 900 °C RTA. After etching non-reacted metal, Al contact metal was added on source-drain to form the *n*-MOSFETs with 10-μm (100-μm size. The

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interface reaction was investigated by Transmission Electron microscopy (TEM). The fabricated *n*-MOSFETs were characterized by capacitance–voltage (*C–V*) and current–voltage (*J–V*) measurements. The EOT extractions of experimental *C–V* curves were well fitted by CVC simulators.

3. Results and discussion

Fig. 1a and b shows the *C–V* and *J–V* curves of TaN/TiLaO *n*-MOS devices at various RTA temperatures. High capacitance density of 3.3 μF/cm^2, leakage current of 6.7 × 10^{-2} A/cm^2 at −1 V and proper V_{fb} of −0.6 V are obtained after 800 °C RTA. This gives an EOT of 0.72 nm by CVC Quantum-Mechanical *C–V* simulation. The large negative V_{fb} with thickness dependence is unique property of La_2O_3 dielectric [6]. Both the increased capacitance density for a reduced EOT and negative V_{fb} shift are observed with increasing thermal budget from 400 °C PDA to 800 °C RTA. It is demonstrated that the gate dielectric was densified but thicker interfacial layer were also formed after 800 °C RTA. The TEM images of MOS sample with 800 °C RTA was inserted in Fig. 1a, where the 1.2-nm-thick interfacial layer was clearly observed. Such interfacial layer formation is unavoidable because of the strong bond enthalpy of Si–O (800 kJ/mol) close to La–O (799 kJ/mol) but higher than Ti–O (672 kJ/mol) [3]. Furthermore, the titanium-based silicate interface with higher interface states is unstable. The severe V_{fb} roll-off to positive bias direction and degraded capacitance density were found when increasing RTA temperature up to 900 °C (not shown here).

To prevent from V_{fb} roll-off and unstable interface formation at a gate first process, the high-κ CeO_2 was used to improve interface thermal stability of higher-κ TiLaO dielectric. Fig. 2a and b shows the *C–V* and *J–V* curves of TiLaO/CeO_2 *n*-MOS devices with different RTA conditions. The capacitance density of 2.3 μF/cm^2 and gate leakage current of 1.1 × 10^{-2} A/cm^2 at −1 V were measured at a low 550 °C RTA. However, a very high capacitance density of 4.2 μF/cm^2 and low leakage current of 1.2 A/cm^2 at −1 V were further reached after a high thermal budget of 900 °C. The high-density gate capacitance provides a small EOT of 0.56 nm, which can be used for 16 nm technology node with 10 nm gate length according to ITRS. As shown in TEM image of Fig. 2c, a cerium–silicate (checked by EDX) with sharp interface was found within the 3.6-nm-thick TiLaO/CeO_2 gate dielectric stack, giving a high-κ value of 25. Thus, the well-behaved *C–V* curves and the increased capacitance density by 82% from 500 °C to 900 °C RTA explain that

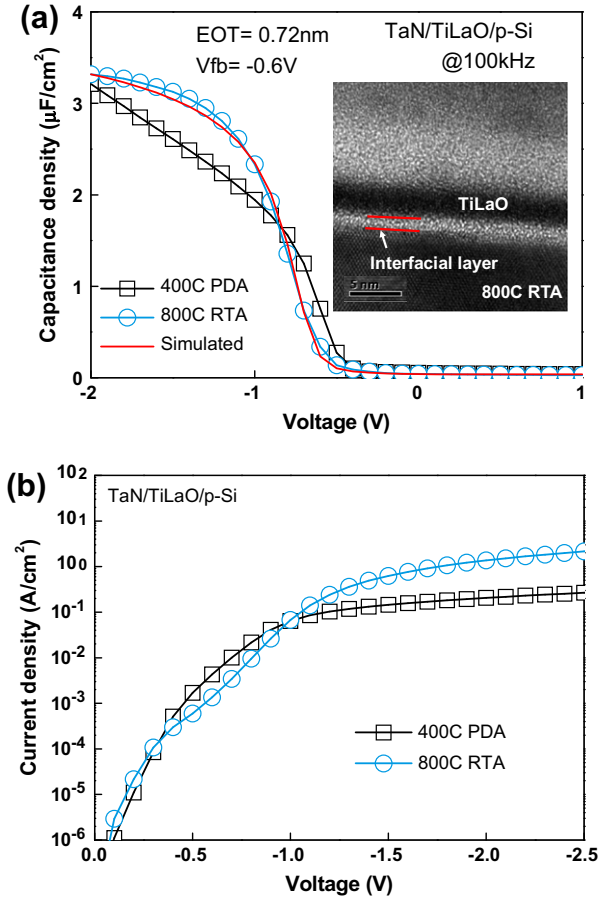

Fig. 1. (a) *C–V* and (b) *J–V* characteristics of TiLaO *n*-MOS capacitors with 400 °C PDA and 800 °C RTA. The inset figure is cross-sectional TEM picture of TiLaO *n*-MOS capacitors after 800 °C RTA.

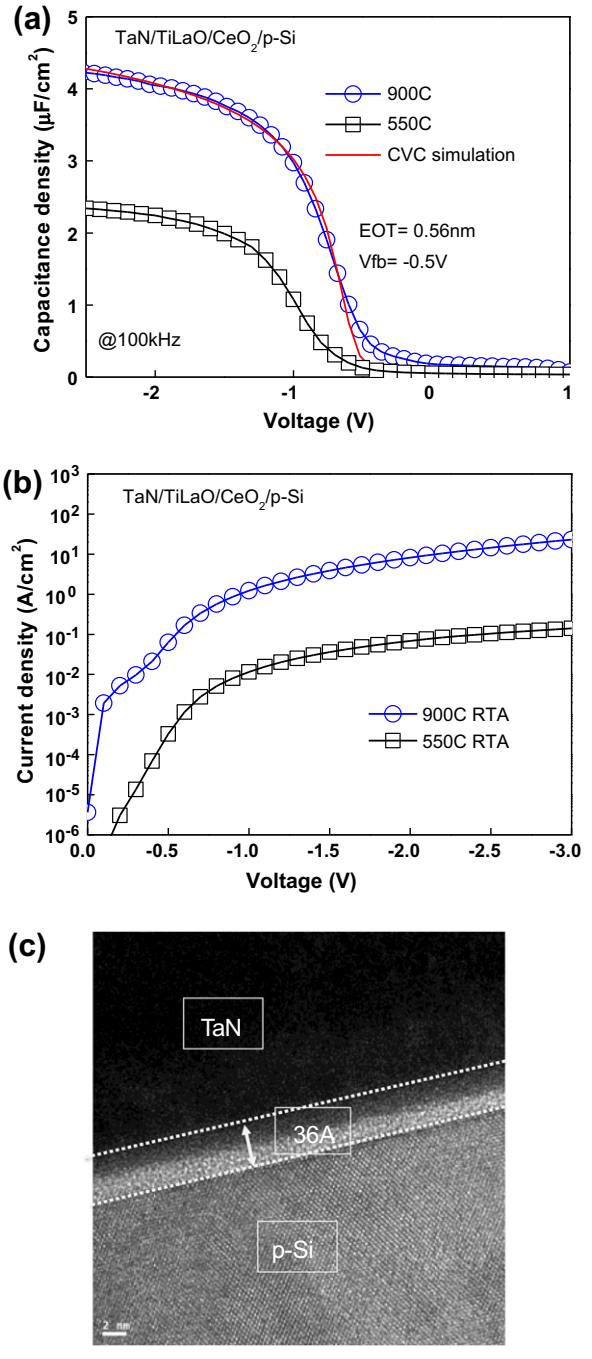

Fig. 2. (a) *C–V*, (b) *J–V* characteristics and (c) cross-sectional TEM picture of TiLaO/CeO_2 *n*-MOS capacitors.

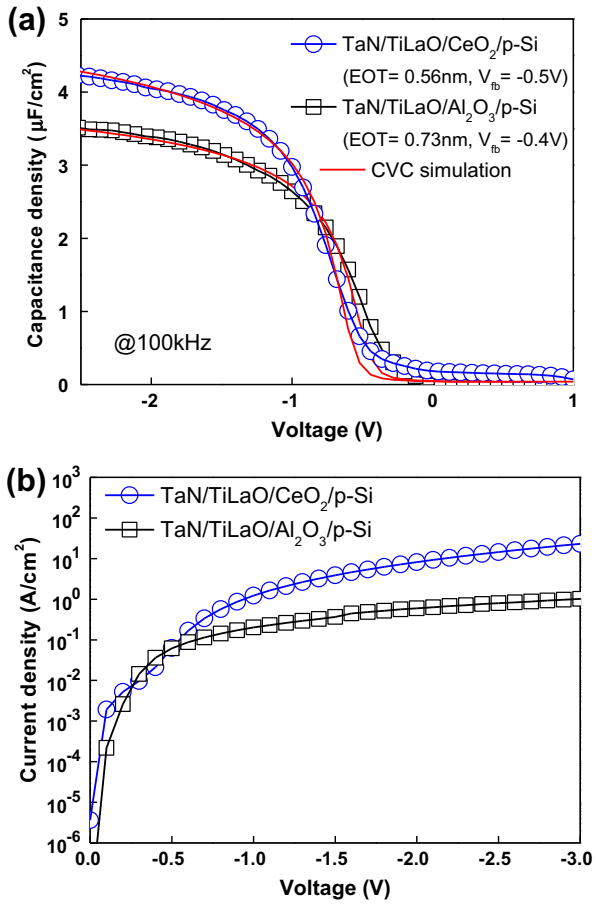

Fig. 3. (a) *C–V* and (b) *J–V* characteristics TiLaO/[CeO_2 or Al_2O_3] *n*-MOS capacitors.

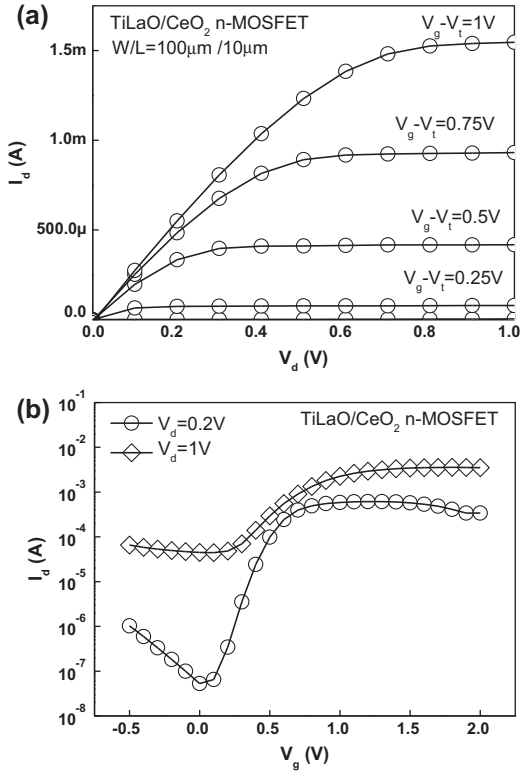

Fig. 4. (a) I_d–V_d and (b) I_d–V_g characteristics of TiLaO/CeO_2 *n*-MOSFETs.

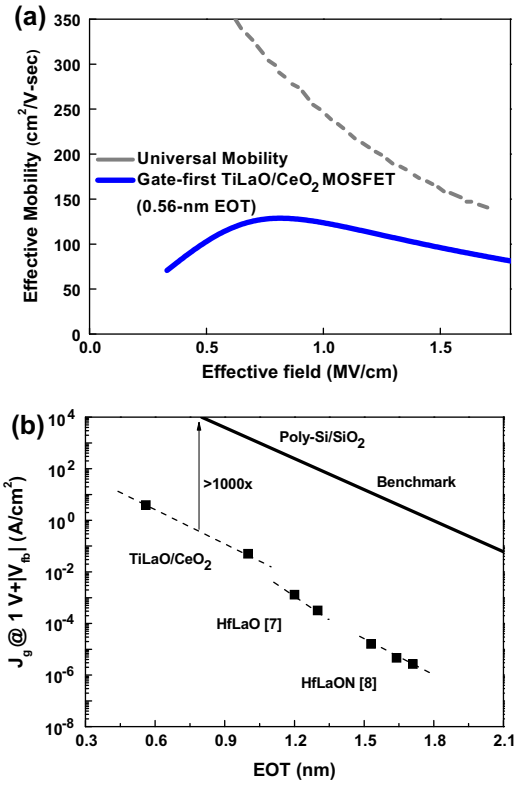

Fig. 5. (a) Electron mobility and (b) EOT verse gate leakage (EOT-Jg) characteristics of TiLaO/CeO_2 *n*-MOSFETs.

the observed interfacial layer is robust cerium silicate rather than low-κ defective SiO_2.

From the viewpoint of EOT scaling, the Al_2O_3 dielectric with large bandgap and good thermal stability is suitable as buffered layer to resist the formation of defective interfacial layer. Thus, we also fabricated a TiLaO/Al_2O_3 *n*-MOS device as a control sample for comparison. Fig. 3a and b shows the *C–V* and *J–V* curves of TaN/TiLaO/[CeO_2 or Al_2O_3] *n*-MOS capacitors after 900 °C RTA. Compared to TiLaO/CeO_2 *n*-MOS, TiLaO/Al_2O_3 one has a lower capacitance density of 3.5 μF/cm^2 and larger 0.73-nm EOT, which cannot meet the requirement of sub-0.6-nm EOT at 16 nm technology node. The negative V_{fb} (−0.4 V) with slightly positive shift is believed to be related to the intrinsic dipole effect near Al-based interfacial layer that it is favorable for V_t tuning in *p*-MOSFET.

Fig. 4a and b shows the I_d–V_d and I_d–V_g characteristics of TiLaO/CeO_2 *n*-MOSFET. In addition to output transistor characteristics, the low V_t of 0.31 V was measured at this 0.56-nm-EOT transistor. Fig. 5a shows the effective mobility extracted by split CV measurement based on linear I_d–V_g characteristic in TiLaO/CeO_2 *n*-MOSFETs. The universal mobility of conventional MOSFET was plotted for comparison. A mobility of 126 cm^2/V s at 0.8 MV/cm was obtained in TiLaO/CeO_2 *n*-MOSFET with a 0.56 nm EOT. It has been clarified that such low V_t and EOT can be attributed to the unique negative V_{fb} of La_2O_3 in bulk TiLaO and robust cerium silicate interface with high bond enthalpy. However, the device mobility is significantly smaller than the TiN/HfO_2 *n*-MOSFET with a 1 nm EOT [11]. The mobility degradation at small sub-0.6-nm EOT is unavoidable due to charged vacancies in the dielectric or related remote phonon scattering. Although the interface state is high at this small-EOT MOSFET with gate first process, further improvement on mobility can be expected by inserting an ultrathin oxide [15] or low-temperature junction formation by solid-phase diffusion [13]. Besides, the gate leakage at 1 V above V_{fb} for TiLaO/CeO_2 *n*-MOSFET still can maintain ⩾3 orders of magnitude lower

than that of benchmark SiO_2 while EOT scaling from 1 nm to 0.56 nm, as shown in Fig. 5b.

4. Conclusions

We report a gate-first *n*-MOSFET with a low EOT of 0.56 nm using gate stack of $TiLaO/CeO_2$. The robust cerium silicate interfacial layer was used to prevent from additional EOT increase at a gate-first process, which enabled aggressive EOT scaling down to <0.6 nm target of 16 nm technology node. Thus, this self-aligned and gate-first *n*-MOSFET with a highly scaled EOT is compatible with CMOS process.

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