Impacts of Multiple Strain-Gate Engineering on a Zero-Temperature-Coefficient Point

Tien-Shun Chang, Tsung Yi Lu, and Tien-Sheng Chao

***Abstract*— The impacts of zero-temperature-coefficient (ZTC) points of various strained devices is presented in this letter. The current and mobility are reduced at high temperature by phonon scattering. The degree of mobility reduction becomes severe on devices with multiple strain-gate engineering. The reduction of mobility becomes severe as a result of impurity scattering, which results from gate implantation impurities. The ZTC point is decreased by multiple strain-gate engineering due to the decreased *V*th.**

***Index Terms*— Mobility, nMOSFETs, strain, temperature, zero-temperature-coefficient (ZTC) point.**

I. Introduction

TO MEET the demand of high-speed MOSFETs, strain technologies such as embedded SiGe source/drain [1], contact etch-stop layer (CESL) [2], and the stress memorization technique (SMT) [3] are mature and powerful techniques for improving the device performance. A combination of strain techniques can bring greater stress into the channel and provide better performance for MOSFETs. In our work, MOSFETs fabricated by multiple strain-gate engineering consisting of a strain-proximity-free technique (SPFT) and a preamorphous layer (PAL) gate structure have better electrical properties [4]. However, phonon scattering counteracts the effect of strain technology in mobility enhancement, especially at high temperature. Moreover, unstable temperature issues such as impact ionization efficiency [5], [6] and drain current mismatch [7] at elevated temperatures also have negative influences on the devices and cause reference circuit failure.

To eliminate these negative influences, an interesting parameter, the zero-temperature-coefficient (ZTC) point, can be introduced into the operation of the device. Biasing at the ZTC point can provide constant drain current, which is insensitive to temperature. Therefore, stable performance of the integrated circuit can be achieved [8]–[10]. However, the impact of strain effect on ZTC point has been little explored. In this letter, we extracted the ZTC point by I_d–V_g characteristics at various temperatures, 20 °C, 60 °C, and 120 °C, for devices fabricated by multiple strain-gate engineering. Multiple strain-gate engineering induced band gap narrowing, which decreases not only the threshold voltage but also the ZTC point.

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The authors are with the National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: tschao@mail.nctu.edu.tw).

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TABLE I
ELECTRICAL CHARACTERISTICS OF ALL SAMPLES

	Idsat (μA)	Ioff (pA)	Gmmax (μS/μm)	*V*th (V)
STD	1241	0.489	132.6	0.61
SPFT	1341	0.222	149.1	0.55
SPFT+PAL1	1499	0.102	187.4	0.55
SPFT+PAL2	1593	0.213	217.0	0.50
SPFT+PAL3	1697	0.203	237.6	0.40

II. Experimental Methods

nMOSFETs were fabricated on 6-in wafers with resistivity of 15–25 Ω-cm. 2.5 ± 0.1-nm gate oxide and 200-nm poly-Si were grown in a vertical furnace. Before patterning on the poly-Si gate, the SPFT process was introduced by high-tensile stressor deposition, rapid-thermal annealing (RTA) using spike annealing at 1050 °C, and stressor removal processes. The SPFT processing introduces stress into the channel region. The stressor used in the SPFT was a high-tensile thermal chemical vapor deposition (CVD)-SiN film of 100-nm thickness. The stress level of this film is near 1.3 GPa. Amorphourization of poly-Si is proposed by PAL in gate using an implantation process. It was inserted into the SPFT process after poly deposition [4]. The dosage splits of Arsenic are 40 keV, 1E15 cm^{-2}, and 40 keV, 5E15 cm^{-2} for PAL1 and PAL2, respectively. PAL3 is combination of PAL2 and two-step anneal inserting after stressor buffer-oxide deposition. Hence, PAL3 can generate greater stress into the channel [4].

After gate patterning, source/drain extension implantation, side-wall spacer and S/D formation were carried out. A 100-nm thermal CVD tensile SiN CESL was deposited on all transistors. After interlayer dielectric film deposition and contact patterning, a four-level metallization (Ti-TiN-Al-TiN) was carried out on the PVD system. The electrical characteristics were measured by a Keithly-4200 and are shown in Table I. Significant improvements in drain current in SPFT, SPFT with PAL1, SPFT with PAL2, and SPFT with PAL3 are found. It appears that SPFT with PAL1, SPFT with PAL2, and SPFT with PAL3 can further improve the drain current, by 21%, 28%, and 38%, $V_g - V_{th} = 1$ V and $V_{ds} = 2$ V respectively.

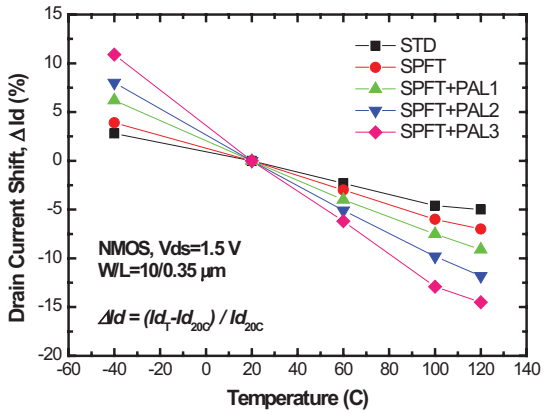

Fig. 1. Drain current shift for STD, SPFT, SPFT with PAL1, SPFT with PAL2, and SPFT with PAL3 at various temperatures.

III. Results and Discussion

The drain-current shift at various temperatures compared to that at 20 °C is defined as $(Id_T - Id_{20C})/Id_{20C}$ and is shown in Fig. 1. The shifts in the drain current of STD, SPFT, SPFT with PAL1, SPFT with PAL2, and SPFT with PAL3 are 2.8%, 3.9%, 6.2%, 8.0%, and 10.9% at −40 °C, respectively. Compared to the shift in the drain current at 120 °C (−5%, −7%, −9.1%, −11.8%, −14.5%, respectively.), the shift in the drain current decreases when temperature increases. The degradation of mobility results from phonon scattering, which is the dominant scattering mechanism at higher temperatures. Furthermore, the degree of degradation becomes more serious on devices fabricated by multiple strain-gate engineering. The reason the reduction in mobility becomes more serious is due to impurity scattering, a result of the poly-Si gate implantation [11]. Although the multiple strain-gate engineering improves the performance, it is accompanied by serious mobility degradation at high temperatures. Hence, devices fabricated by multiple strain-gate engineering reveal stronger temperature dependence [11]. It is important to minimize the variation in the current for applications where temperature varies. Thus, operation at the ZTC point could be a solution for circuit design.

The definition of the ZTC point is that the drain current reveals no temperature sensitivity at $V_g = V_g(\text{ZTC})$. The existence of the ZTC point is due to reciprocal compensation between the effective mobility and threshold voltage at the elevated operated temperature of MOSFETs. In general, lower ZTC point has benefits for low power consumption devices. The threshold voltages are 0.61, 0.55, 0.55, 0.5, and 0.4 V for STD, SPFT, SPFT with PAL1, SPFT with PAL2, and SPFT with PAL3, respectively. The threshold voltage decreases more seriously in SPFT with PAL gate structures than just SPFT. The decreased threshold voltage by strain effect is due to a band gap narrowing. Therefore, multiple strain-gate engineering leads to a larger threshold voltage shift.

We measured the $V_g(\text{ZTC})$ of all samples for operation at room temperature to military range (from 20 °C to 120 °C). Fig. 2 shows the I_d–V_g characteristics for all samples.

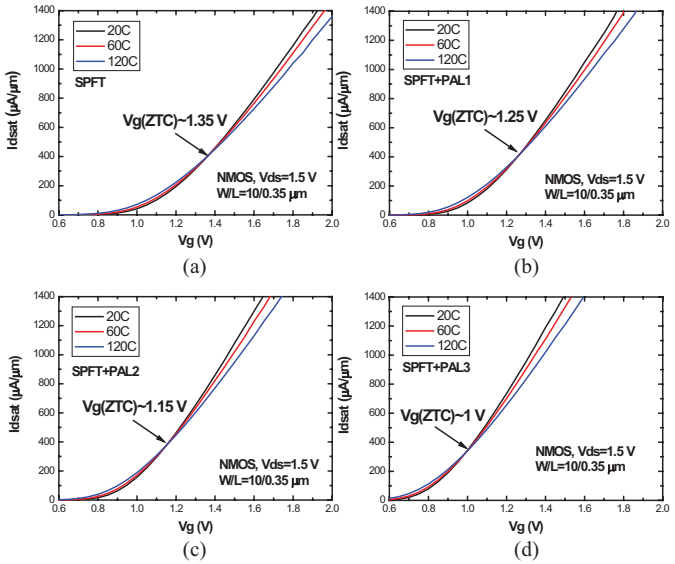

Fig. 2. ZTC point extraction by I_d–V_g characteristics at various temperatures of 20 °C, 60 °C, and 120 °C for (a) SPFT, (b) SPFT with PAL1, (c) SPFT with PAL2 and (d) SPFT with PAL3.

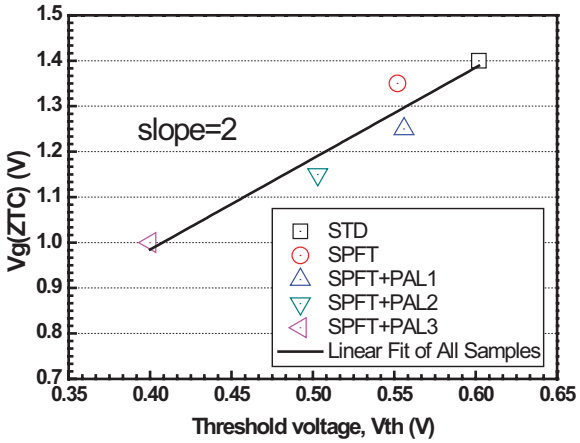

Fig. 3. Threshold voltage dependence of the ZTC point, It shows a strong correlation between V_g(ZTC) and the threshold voltage

The ZTC points of STD, SPFT, SPFT with PAL1, SPFT with PAL2, and SPFT with PAL3 are 1.4, 1.35, 1.25, 1.15, and 1 V, respectively. It is also found that the ZTC point decreases in the SPFT and that the decrease becomes more serious in SPFT with PAL gate structures. As shown in Fig. 3, V_g(ZTC) shows a strong dependence on the threshold voltage. Both V_g(ZTC) and threshold voltage have the same trend for multiple strain-gate engineering. The expression of threshold voltage shift and V_g(ZTC) shift can be derived as follows (1).

The drain current biasing at ZTC point in saturation region are given by

$$I_{ZTC1} = K(V_{ZTC} - V_{th})^2 \quad (1)$$

$$I_{ZTC2} = K[(V_{ZTC} + \Delta V_{ZTC}) - (V_{th} + \Delta V_{th})]^2 \quad (2)$$

where K is $1/2(W/L)\mu C_{ox}$, and ΔV_{ZTC} and ΔV_{th} are the ZTC point shift and threshold voltage shift caused by strain engineering, respectively. Assuming ΔV_{ZTC} and ΔV_{th} are

very small. Therefore, equation (2) can be rewritten as

$$I_{ZTC2} \approx I_{ZTC1} + 2K(V_{ZTC} - V_{th})(\Delta V_{ZTC} - \Delta V_{th}). \quad (3)$$

Thus, the drain current shift caused by strain engineering at ZTC point is given by

$$\Delta I_{ZTC} \equiv I_{ZTC2} - I_{ZTC1} \approx 2K(V_{ZTC} - V_{th})(\Delta V_{ZTC} - \Delta V_{th}). \quad (4)$$

The drain current shift caused by strain engineering can be described by a function of V_g as

$$I_{d1}(V_g) = K(V_g - V_{th})^2 \quad (5)$$

$$I_{d2}(V_g) = K[V_g - (V_{th} + \Delta V_{th})]^2. \quad (6)$$

Similarly, (6) can be rewritten as

$$I_{d2}(V_g) \approx I_{d1}(V_g) - 2K(V_g - V_{th})\Delta V_{th} \quad (7)$$

$$\Delta I_d \equiv I_{d1} - I_{d2} \approx 2K(V_g - V_{th})\Delta V_{th} \quad (8)$$

where ΔI_d is the drain current shift caused by strain engineering and is a function of V_g as well. Thus, the drain-current shifts at ZTC point also can be expressed by

$$\Delta I_{ZTC} \equiv \Delta I_d(V_g = V_{ZTC}) \approx 2K(V_{ZTC} - V_{th})\Delta V_{th}. \quad (9)$$

Compare (4) and (9), and the expression of threshold voltage shift and V_g(ZTC) shift is given by

$$\Delta V_{ZTC} - \Delta V_{th} = \Delta V_{th}; \text{ hence, } \Delta V_{ZTC} = 2\Delta V_{th}. \quad (10)$$

The shift in V_g (ZTC) doubles that of the threshold voltage, as confirmed by the slope of the fitting line in Fig. 3 (slope = 2). Consequently, the decreased threshold voltage of devices caused by multiple strain-gate engineering is the root cause of decreasing V_g(ZTC). The strong correlation between V_g(ZTC) and the threshold voltage (V_{th}) for SPFT and SPFT with PAL gate structure are expected to explain this phenomenon. Multiple strain-gate engineering brings not only an improvement in performance but also lower V_g(ZTC). Circuits operated at lower V_g(ZTC) offer great benefits in power consumption.

IV. Conclusion

Experimental results show stronger temperature dependence of the shift in the mobility, which results in larger current deviation for devices with multiple strain-gate engineering. Current insensitivity to temperature variation is important in the circuit design. Introducing a ZTC point could be a solution for circuit design. A strong correlation between V_g(ZTC) and threshold voltage is found. The shift of V_g (ZTC) doubles that of threshold voltage. The ZTC point decreased under multiple strain-gate engineering can be explained by the decreased V_{th}.

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