Charge Quantity Influence on Resistance Switching Characteristic During Forming Process

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***Abstract*—In this letter, we presented that the charge quantity is the critical factor for forming process. Forming is a pivotal process in resistance random access memory to activate the resistance switching behavior. However, overforming would lead to device damage. In general, the overshoot current has been considered as a degradation reason during the forming process. In this letter, the quantity of charge through the switching layer has been proven as the key element in the formation of the conduction path. Ultrafast pulse forming can form a discontinuous conduction path to reduce the operation power.**

***Index Terms*—Forming process, hafnium oxide ($\mathbf{HfO_2}$), nonvolatile memory, resistance switching.**

I. Introduction

CONVENTIONAL nonvolatile floating memory (NVM) is expected to reach certain technical and physical limits in the future. In order to overcome this problem, alternative memory technologies have been extensively investigated [1]–[5]. Among these NVMs, resistance random access memory (RRAM) has recently attracted great attention in next-generation NVM applications owing to the advantages of low operating power, fast operation speed, and high density integration [6]–[11]. The memory cells exhibit reversible electric field-induced resistance switching between the high-resistance state (HRS) and the low-resistance state (LRS). Heretofore, the resistance switching effect has been observed in various materials, including perovskite oxides [12], chalcogenide materials [13], and oxide materials [14]–[17]. In this letter, hafnium oxide (HfO_2) was taken as the resistance switching layer because HfO_2 is extremely compatible with the prevalent complementary metal–oxide–semiconductor process.

These devices have to go through a pivotal forming process to activate the resistance switching behavior. Nevertheless, overforming would lead to device damage and cause inferior resistance switching characteristic. Therefore, forming is a significant issue to research. In this letter, the charge quantity through the switching layer is the key factor in the formation of the conduction path.

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II. Experimental Setup

First, a titanium nitride (TiN) 200-nm bottom electrode was deposited by using RF sputter. Second, lithography process was taken to pattern the cell size via. After this, we start growing our dielectric layer 10 nm by using the atomic layer deposition process. Finally, we sputtered TiN/Ti layer 40 nm/10 nm as our top electrode and used acetone in etching the photo resistor. The cell size of RRAM devices in this experiment is 0.24 μm $*$ 0.24 μm.

III. Results and Discussion

All of the electric characteristics were measured by the Agilent B1500 semiconductor parameter analyzer and the Agilent B1530 fast I–V measurement system. The resolution of the fast I–V measurement system is 10 ns. The dc sweeping and pulse bias were applied to the bottom electrode (TiN), and the top electrode (Ti) was grounded during the electrical measurement.

Fig. 1(a) shows the typical bipolar resistance switching behavior with the Ti/HfO_2/TiN device, which is after the forming process with dc sweep mode and pulse mode. The irreversible forming process is required to activate the as-fabricated memory cells. In general, the dc voltage sweep mode is used for the forming process with a compliance current of 100 μA, as shown

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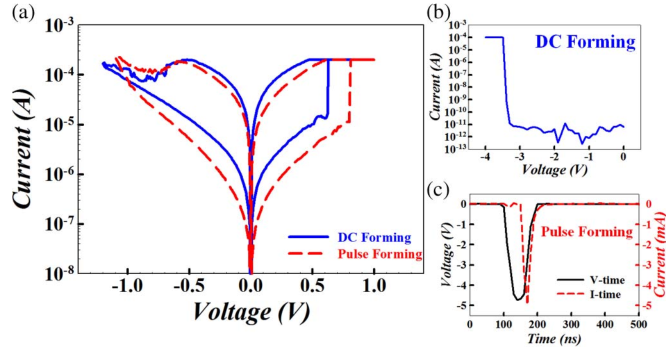

Fig. 1. (a) Typical bipolar resistance switching current–voltage curves of the Ti/HfO_2/TiN cells after dc forming and pulse forming. (b) Forming with dc voltage sweep mode. (c) Forming with ultrafast pulse I–V mode.

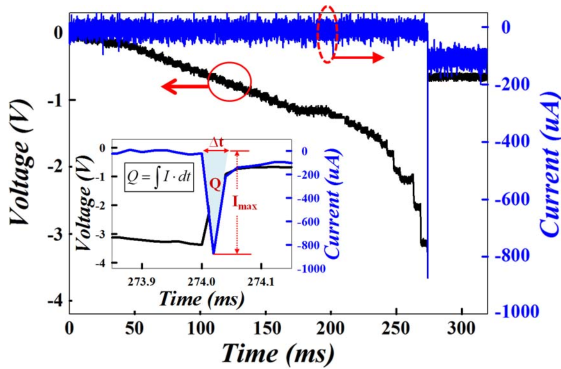

Fig. 2. Experimental result of forming process observed with the circuit designed by the semiconductor parameter analyzer and an oscilloscope.

in Fig. 1(b). During the forming process, a sudden increase in current occurs at a voltage of about -3.5 V, where the memory cell was transformed from HRS to LRS. In this letter, the ultrafast pulse I–V mode is used as the forming method with pulse forming condition -4.5 V (50 ns), as shown in Fig. 1(c). During the pulse forming process, a sudden increase in current occurs at 150 ns, where the pass current continually rises to 5 mA. Compared with the resistance switching property of dc forming, ultrafast pulse forming reduces the operation current.

In general, the forming process with dc voltage sweep cannot control the pass current effectively, causing large leakage current. In order to accurately observe the forming process, the semiconductor parameter analyzer and an oscilloscope were used [18]. The voltage (VRRAM) and current (IRRAM) on the RRAM device were obtained from the oscilloscope signal. The black and blue lines show VRRAM and IRRAM signals, respectively, as shown in Fig. 2. The initial IRRAM signal approaches zero. At the forming voltage, where the current suddenly spikes, the RRAM transforms from initial state to LRS. The path current shoots over the compliance current by nine times, although the compliance current is limited at 100 μA during the forming process. As shown in Table I, the maximum current $I_{\max}$ of pulse forming is greater than that of dc forming by over five times. In general, the overshoot current is considered as a degradation issue in RRAM devices. However, in this letter, the higher $I_{\max}$ results in lower damages for the RRAM devices. Forming is a pivotal process to create the conduction path. In chemical reaction, the extent of reaction

TABLE I

PARAMETER EXTRACTED DURING DC FORMING AND PULSE FORMING

	DC Forming	***Pulse*** Forming
I_{max}	~ 0.9 mA	~ 5 mA
Δt	40 μs	60 ns
Q	$1.6*10^{-8}$C	$1.5*10^{-10}$C

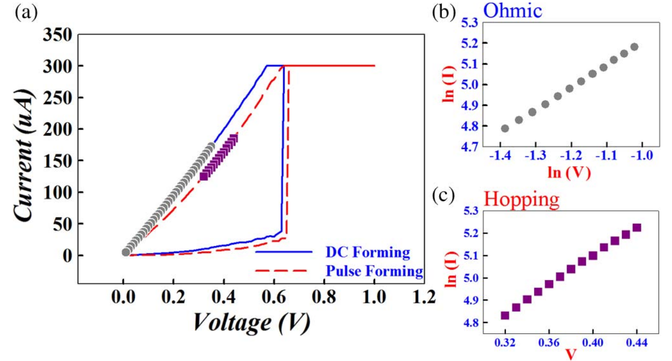

Fig. 3. (a) Carrier transport analysis with the I–V curves fitting at LRS. The fitting analysis of (b) dc forming and (c) pulse forming.

is related to the quantity of charge Q, where Q was calculated and shown in Table I. We proposed that the degradation issue in RRAM devices must take time into consideration. The total pass charge quantity can influence the size and shape of the formed conduction path.

In order to ascertain the switching mechanism, the I–V curves are fitted to analyze carrier transport of the switching layer [19], as shown in Fig. 3. A good linear relationship with a slope of 1, between Napierian logarithm leakage current $(\ln(I))$ and Napierian logarithm voltage $(\ln(V))$, indicates that the leakage current of the dc forming device in LRS is dominated by ohmic conduction, as shown in Fig. 3(b). According to the relationship of hopping conduction, $J = aN a\upsilon_0 e^{-q\phi_T/kT} e^{qaV/2dkT}$, where N, a, ϕ_T, υ_0, and d are the density of space charge, the mean of hopping distance, intrinsic vibration frequency, the barrier height of hopping, and film thickness, respectively, as shown in Fig. 3(c), displayed the fitting result of the pulse forming device in LRS, in which the relationship between $\ln(I)$ and applied voltage V is linear. Therefore, hopping conduction is considered as the main transport mechanism [20]. Such conduction requires the electrons to execute discrete jumps across an energy barrier and through space from one site to next. The density of defects will be small enough for hopping to occur between defect sites on account of their small physical separation. As the defects become close enough subsequently, the electrons can jump across a reduced small energy barrier with thermal excitation.

According to the above experiment result, the resistance switching properties are dominated by the forming process. For oxide materials, the oxygen vacancy V_O^{2+}-associated conducting path is usually regarded as the origin of filaments. During the forming process triggered by sufficient electric field, the oxygen ion (O^{2-}) is created accompanying V_O^{2+}. V_O^{2+} subsequently constituted the conduction filaments. The size and shape of the conduction path relate with the pass Q. The large quantity of charge formed the continuous conduction

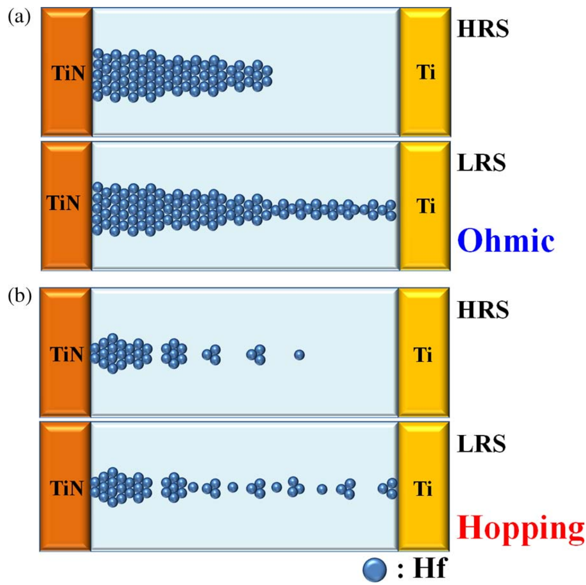

Fig. 4. Schematics of carrier transport behavior after (a) dc forming and (b) pulse forming.

filament. The carriers transported through the continuous filament, causing ohmic conduction in LRS, as shown in Fig. 4(a). On the contrary, the small quantity of charge can form the discontinuous conduction path to reduce pass leakage current, as shown in Fig. 4(b). Both states of pulse forming devices can reduce the operation current because the conduction path is fragmented and the carriers have to transport by thermal hopping conduction.

IV. Conclusion

In conclusion, the quantity of charge through the switching layer would influence the size and shape of the formed conduction filament during the forming process. In the pulse forming process, the discontinuous conduction path is formed. The operation current can be reduced, and the carriers have to transport by thermal happing conduction.

References

[1] T. C. Chang, F. Y. Jian, S. C. Chen, and Y. T. Tsai, "Developments in nanocrystal memory," *Mater. Today*, vol. 14, no. 12, pp. 608–615, Dec. 2011.

[2] F. M. Yang, T. C. Chang, P. T. Liu, P. H. Yeh, Y. C. Yu, J. Y. Lin, S. M. Sze, and J. C. Lou, "Memory characteristics of Co nanocrystal memory device with HfO_2 as blocking oxide," *Appl. Phys. Lett.*, vol. 90, no. 13, pp. 132102-1–132102-3, Mar. 2007.

[3] S. C. Chen, T. C. Chang, P. T. Liu, Y. C. Wu, P. S. Lin, B. H. Tseng, J. H. Shy, S. M. Sze, C. Y. Chang, and C. H. Lien, "A novel nanowire channel poly-Si TFT functioning as transistor and nonvolatile SONOS memory," *IEEE Electron Device Lett.*, vol. 28, no. 9, pp. 809–811, Sep. 2007.

[4] D. D. Jiang, M. H. Zhang, Z. L. Huo, Q. Wang, J. Liu, Z. A. Yu, X. N. Yang, Y. Wang, B. Zhang, J. N. Chen, and M. Liu, "A study of cycling induced degradation mechanisms in Si nanocrystal memory devices," *Nanotechnology*, vol. 22, no. 25, p. 254009, Jun. 2011.

[5] S. Q. Yang, Q. Wang, M. H. Zhang, S. B. Long, J. Liu, and M. Liu, "Titanium tungsten nanocrystals embedded in SiO_2/Al_2O_3 gate dielectric stack for low-voltage operation in non-volatile memory," *Nanotechnology*, vol. 21, no. 24, p. 245201, Jun. 2010.

[6] M. Tsai, K. C. Chang, T. C. Chang, G. W. Chang, Y. E. Syu, Y. T. Su, G. R. Liu, K. H. Liao, M. C. Chen, H. C. Huang, Y. H. Tai, D. S. Gan, C. Ye, H. Wang, and S. M. Sze, "Origin of hopping conduction in Sn-doped silicon oxide RRAM with supercritical CO_2 fluid treatment," *IEEE Electron Device Lett.*, vol. 33, no. 12, pp. 1693–1695, Dec. 2012.

[7] M. Tsai, K. C. Chang, T. C. Chang, Y. E. Syu, S. L. Chuang, G. W. Chang, G. R. Liu, M. C. Chen, H. C. Huang, S. K. Liu, Y. H. Tai, D. S. Gan, Y. L. Yang, T. F. Young, M. J. Tsai, C. Ye, H. Wang, and S. M. Sze, "Bipolar resistive RAM characteristics induced by nickel incorporated into silicon oxide dielectrics for IC applications," *IEEE Electron Device Lett.*, vol. 33, no. 12, pp. 1696–1698, Dec. 2012.

[8] Y. Wang, Q. Liu, S. B. Long, W. Wang, Q. Wang, M. H. Zhang, S. Zhang, Y. T. Li, Q. Y. Zuo, J. H. Yang, and M. Liu, "Investigation of resistive switching in Cu-doped HfO_2 thin film for multilevel non-volatile memory applications," *Nanotechnology*, vol. 21, no. 4, p. 045202, Jan. 2010.

[9] Q. Liu, S. B. Long, H. B. Lv, W. Wang, J. B. Niu, Z. L. Huo, J. N. Chen, and M. Liu, "Controllable growth of nanoscale conductive filaments in solid-electrolyte-based ReRAM by using a metal nanocrystal covered bottom electrode," *ACS Nano*, vol. 4, no. 10, pp. 6162–6168, Sep. 2010.

[10] Y. E. Syu, T. C. Chang, T. M. Tsai, G. W. Chang, K. C. Chang, J. H. Lou, Y. H. Tai, M. J. Tsai, Y. L. Wang, and S. M. Sze, "Silicon introduced effect on resistive switching characteristics of WO_X thin films," *Appl. Phys. Lett.*, vol. 100, no. 2, pp. 022904-1–022904-4, Jan. 2012.

[11] T. M. Tsai, K. C. Chang, T. C. Chang, Y. E. Syu, K. H. Liao, B. H. Tseng, and S. M. Sze, "Dehydroxyl effect of Sn-doped silicon oxide resistance random access memory with supercritical CO_2 fluid treatment," *Appl. Phys. Lett.*, vol. 101, no. 11, pp. 112906-1–112906-4, Sep. 2012.

[12] A. Sawa, "Resistive switching in transition metal oxides," *Mater Today*, vol. 11, no. 6, pp. 28–36, Jun. 2008.

[13] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nat. Mater.*, vol. 6, no. 11, pp. 833–840, Nov. 2007.

[14] M. C. Chen, T. C. Chang, C. T. Tsai, S. Y. Huang, S. C. Chen, C. W. Hu, S. M. Sze, and M. J. Tsai, "Influence of electrode material on the resistive memory switching property of indium gallium zinc oxide thin films," *Appl. Phys. Lett.*, vol. 96, no. 26, pp. 262110-1–262110-3, Jun. 2010.

[15] M. Liu, Z. Abid, W. Wang, X. L. He, Q. Liu, and W. H. Guan, "Multilevel resistive switching with ionic and metallic filaments," *Appl. Phys. Lett.*, vol. 94, no. 23, pp. 233106-1–233106-3, Jun. 2009.

[16] K. C. Chang, T. M. Tsai, T. C. Chang, Y. E. Syu, C. C. Wang, S. L. Chuang, C. H. Li, D. S. Gan, and S. M. Sze, "Reducing operation current of Ni-doped silicon oxide resistance random access memory by supercritical CO_2 fluid treatment," *Appl. Phys. Lett.*, vol. 99, no. 26, pp. 263501-1–263501-4, Dec. 2011.

[17] Q. Liu, C. M. Dou, Y. Wang, S. B. Long, W. Wang, M. Liu, M. H. Zhang, and J. N. Chen, "Formation of multiple conductive filaments in the Cu/ZrO_2 : Cu/Pt device," *Appl. Phys. Lett.*, vol. 95, no. 2, pp. 023501-1–023501-3, Jul. 2009.

[18] Y. E. Syu, T. C. Chang, T. M. Tsai, Y. C. Hung, K. C. Chang, M. J. Tsai, M. J. Kao, and S. M. Sze, "Redox reaction switching mechanism in RRAM device with Pt/$CoSiO_X$/TiN structure," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 545–547, Apr. 2011.

[19] Y. E. Syu, T. C. Chang, T. M. Tsai, G. W. Chang, K. C. Chang, Y. H. Tai, M. J. Tsai, Y. L. Wang, and S. M. Sze, "Asymmetric carrier conduction mechanism by tip electric field in $WSiO_X$ resistance switching device," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 342–344, Mar. 2012.

[20] D. Ielmini and Y. Zhang, "Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices," *J. Appl. Phys.*, vol. 102, no. 5, pp. 054517-1–054517-13, Sep. 2007.