# Ni/$GeO_x$/$TiO_y$/TaN RRAM on Flexible Substrate With Excellent Resistance Distribution

K. I. Chou, C. H. Cheng, Z. W. Zheng, Ming Liu, and Albert Chin, *Fellow, IEEE*

***Abstract*—Excellent device-to-device distribution was achieved in high-performance Ni/$GeO_x$/$TiO_y$/TaN resistive random access memory on low-cost flexible plastics, with low 30-$\mu$W switching power (9 $\mu$A at 3 V; $-1$ $\mu$A at $-3$ V), $10^5$ cycling endurance, and good retention at 85 °C. These were ascribed to bulk transport property by tunneling between traps, forming-free resistive switching, and the less destructive low power switching.**

***Index Terms*—Flexible electronics, $GeO_x$, resistive random access memory (RRAM), $TiO_y$.**

## I. Introduction

FLEXIBLE electronics are attractive for next-generation display technology. One challenge of flexible electronics is the lacking of nonvolatile memory (NVM) for system-on-a-chip function. The conventional floating-gate or charge-trapping Flash (CTF) memory [1], [2] is difficult to be integrated into flexible substrate due to the severely degraded gate oxide quality at low temperature [3]. On the contrary, the resistive random access memory (RRAM) [4]–[11] has inherent merits of low-temperature process and simple structure for flexible electronics application [12]–[17], but the fundamental issues for RRAM are the high-cost noble metal electrode and poor resistance distribution. Such large distribution prevents further memory array realization, in sharp contrast to the existing subterabit Flash memory. To address this issue, previously, we developed the ultralow power RRAM [5]–[7] to lessen the dielectric stress. The Ni/$GeO_x$/high-$\kappa$/TaN RRAMs showed a negative temperature coefficient that is opposite to other conductive-filament-type RRAMs by ion migration.

In this letter, we report a novel RRAM NVM device on flexible plastics. Record-best distributions among RRAM devices are achieved on flexible substrate for the first time, much better than the devices using metallic filament switching [4], [8], [10]–[12], [14]–[17]. Improved uniformity was also reported in metal-doped $ZrO_2$ RRAMs [18], but the high set/reset currents ($\sim 10^{-2}$/ $\sim 10^{-4}$ A) and high processing temperature (700 °C) are the challenges. Low set and reset power, large enough 85 °C retention window, and good electrical endurance are also reached. These much better performances are attributed to the bulk transport property of hopping conduction [19]–[22] and the less destructive low power switching in Ni/$GeO_x$/$TiO_y$/TaN RRAM.

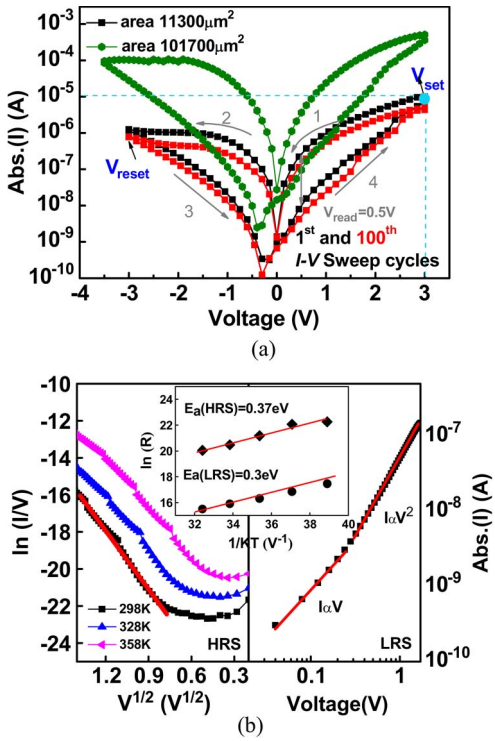


Fig. 1. (a) Swept $I$–$V$ curves of Ni/$GeO_x$/$TiO_y$/TaN flexible RRAM devices. (b) $I$–$V$ curves of the HRS and LRS of Ni/$GeO_x$/$TiO_y$/TaN flexible RRAM by fitting with FP and SCLC mechanisms.

## II. Experiments

The RRAM devices were made on low-cost flexible polyimide substrate at room temperature. First, a thin 200-nm $SiO_2$ isolation layer was deposited on plastic substrate. Then, a 100-nm bottom TaN electrode was deposited and patterned. After that, the stacked 15-nm $TiO_y$ and 10-nm $GeO_x$ layers were deposited. Finally, a 50-nm Ni was deposited and patterned to form the top electrode with an area of 11 300 or 101 700 $\mu m^2$.

## III. Results and Discussion

Fig. 1(a) shows current–voltage ($I$–$V$) switching curves of Ni/$GeO_x$/$TiO_y$/TaN RRAM devices on polyimide.

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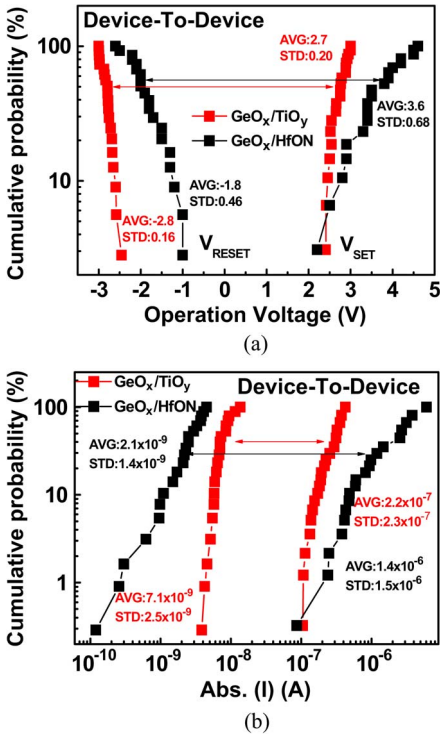


Fig. 2. (a) Voltage and (b) current distributions of Ni/GeO$_x$/TiO$_y$/TaN flexible RRAM and previous Ni/GeO$_x$/HfON/TaN flexible RRAM devices [6].

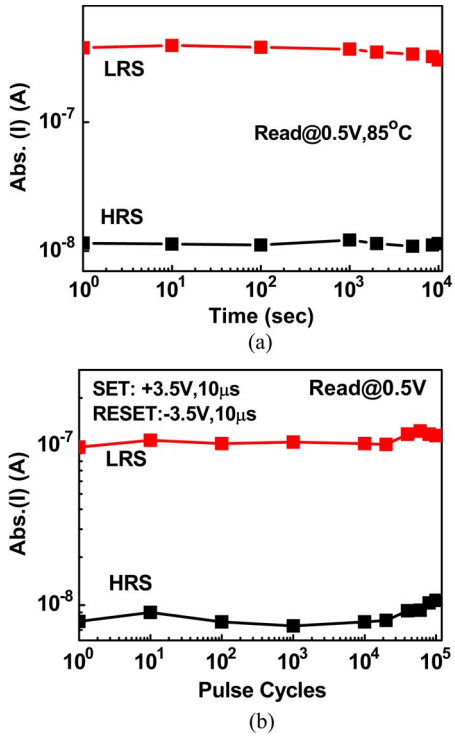


Fig. 3. (a) Retention and (b) endurance characteristics of Ni/GeO$_x$/TiO$_y$/TaN flexible RRAM devices.

Forming-free and self-compliance current switching were measured, which are vital to simplify the circuit design. This RRAM device can be set from high- to low-resistance state (HRS to LRS), at a very low power of only 27 $\mu$W (9 $\mu$A at 3 V). The ultralow reset power of 3 $\mu$W ($-1$ $\mu$A at $-3$ V) is related to the break of the weakly linked phonon-assisted tunneling pass by injected electrons over electrode [6], [7], [19]. The low switching current is due resistance on the order of megaohms by hopping conduction [20] via phonon-assisted tunneling between traps [19]. A good HRS/LRS memory window of 30 is measured at 0.5-V read, with small changes between the 1st and 100th dc-cycled $I$–$V$ curves. The set and reset current densities ($J_{\rm reset}$ and $J_{\rm set}$) at 0.5-V read are $3 \times 10^{-3}$ and $9 \times 10^{-5}$ A/cm$^2$ for 11 300-$\mu$m$^2$ RRAM, which are close to the $4 \times 10^{-3}$ and $9 \times 10^{-5}$ A/cm$^2$ values for the 101 700-$\mu$m$^2$ device. This result suggests the bulk conduction effect that is well predicted by modeling [19]. We also studied the RRAM with different top electrodes. The HRS current monotonically decreases with increasing work-function from Al, W, Ni to Pt, which is similar to MIM capacitors [23], [24] used for DRAM/analog-RF functions to offset the band bending [24]. Although the set/reset resistance window is the best using noble Pt, the high set/reset voltage of $\pm$6 V is above the 5-V source in IC, in addition to its expansive cost and difficult etching issues.

We further analyzed the current conduction mechanism shown in Fig. 1(b). The good agreement between measured and calculated HRS currents suggests the current conducted by Frenkel–Poole (FP) emission via dielectric traps [19]. The increasing HRS current at a higher temperature is due to the higher emission rate from traps. The LRS exhibits defect-conductive space-charge-limited current (SCLC) [25], as evident from the linear $I$–$V$ to $V^2$ from low to high fields. Such phonon-assisted tunneling via defects is verified by temperature-dependent $I$–$V$ and supported by the unified theoretical modeling of HRS and LRS currents [19]. Both LRS and HRS conductivity are governed by multiphonon ionization and tunneling between neighboring traps, where the only different parameter is the trapping concentration (N) [19]. The major defects are charged oxygen vacancies in oxygen-deficient GeO$_x$ and TiO$_y$, as confirmed by X-ray photoelectron spectroscopy.

Good uniformity is the fundamental challenge of RRAM devices for NVM array application. Only few RRAM papers reported the cycle-to-cycle (C2C) distribution in a same device, rather than NVM-array-needed device-to-device (D2D) distribution among different devices [4]–[17]. Fig. 2(a) and (b) shows the voltage and current distributions of the Ni/GeO$_x$/TiO$_y$/TaN RRAM devices, respectively. The set voltage ($V_{\rm set}$) in this letter was defined to a constant current level [26] of 10 $\mu$A. The reset voltage ($V_{\rm reset}$) is defined as the point at which the current is minimized after appearing in the negative differential resistance region [27]. At a voltage higher than $V_{\rm reset}$, the device switches back to the HRS. Because of the different mean value, the coefficient of variation (CV) was used to evaluate the distribution. The CV is a normalized measure of dispersion of a probability distribution, which is defined as the ratio of standard deviation ($\sigma$) to mean value ($\mu$). Here, the current distribution is much wider than voltage distribution. The current CV for LRS and HRS are 45% and 34%, respectively, which are the best data for RRAMs on flexible substrate. The larger CV distribution for LRS than HRS is attributed due to the higher current in the LRS to form the current conduction pass.

TABLE I
COMPARISON OF DEVICE INTEGRITY DATA FOR RRAM DEVICES

| Dielectric (substrate) | $GeO_x$/HfON (PI) [5] | ZnO (PES) [16] | IGZO (PES) [17] | $GeO_x$/$TiO_y$ (PI) (this work) |
|---|---|---|---|---|
| Top/Lower electrode | Ni/TaN | Al/Al | Cu/Cu | Ni/N-rich-TaN |
| $I_{SET}$@$V_{SET}$ | 1.6μA@3V | 5mA@2V | 3mA@1.5V | 9μA@3V |
| $I_{RESET}$@$V_{RESET}$ | -0.5nA@-2V | 10mA@0.4V | 6mA@0.5V | -1μA@-3V |
| On/Off Ratio | 900 | $10^5$ | ~50 | 30 |
| CV, V distrib. set/reset | —<br>19%/26% (D2D) | —<br>— | 37%/27% (C2C)<br>— | 3.8%/4.5% (C2C)<br>7.4%/5.7% (D2D) |
| CV, I distrib. set/reset | —<br>108%/67% (D2D) | 35%/78% (C2C)<br>— | 28%/122% (C2C)<br>— | 12%/9% (C2C)<br>45%/34% (D2D) |
| Retention | $10^4$@85°C | 7x$10^4$@25 °C | — | $10^4$@85°C |
| Cycling | $10^5$ | $10^4$ | 150 | $10^5$ |
| Bending Cycles | $10^5$ | $10^5$ | $10^5$ | $10^5$ |
| Power | 5.8μW | 14mW | 7.5mW | 30μW |

Good retention and endurance are the essential characteristics for NVM. Fig. 3(a) and (b) shows the retention and endurance characteristics, respectively. Good retention with a small HRS/LRS decay for $10^4$ s was measured at 85 °C. Under 10-$\mu$s switching pulse, an excellent electrical endurance of $10^5$ cycles was obtained and comparable with CTF NVM [1], [2].

Table I shows the comparison for various flexible RRAMs. The Ni/$GeO_x$/$TiO_y$/TaN devices have excellent distribution, low set/reset voltages, large enough retention window at 85 °C, low 30-$\mu$W switching power, and good $10^5$ endurance among NVM devices on flexible plastics [12]–[17].

## IV. CONCLUSION

We have reported a high-performance NVM device on low-cost flexible substrate, with excellent distribution, low 30-$\mu$W switching power, and $10^5$ electrical endurance, which are related to the bulk-conductive property, forming-free resistive switching, and low set/reset currents and power.

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