Gate-All-Around Single-Crystal-Like Poly-Si Nanowire TFTs With a Steep-Subthreshold Slope

Tung-Yu Liu, Shen-Chuan Lo, and Jeng-Tzong Sheu

***Abstract*— We investigate the characteristics of single-crystal-like (SCL) poly-Si nanowire (SCL poly-Si NW) thin-film-transistors with gate-all-around (GAA) structures. The GAA SCL poly-Si NWs are prepared by a modified sidewall spacer process utilizing an amorphous silicon (α-Si) mesa structure. The combination of the high surface-to-volume ratio of the NW and a nominal gate length of 0.25 μm lead to clear improvement in electrical performance, including a steep subthreshold swing (90 ± 15 mV/dec), a virtual absence of drain-induced barrier lowering (21 ± 13 mV/V), and a very high ON/OFF current ratio ~7 × 10^7 (V_D = 1 V, V_G = 3 V).**

***Index Terms*— Gate-all-around (GAA), nanowire (NW), single-crystal-like (SCL), thin film transistor (TFT).**

I. Introduction

DUE TO the simplicity in device preparation and excellent performance in electrical properties, polycrystalline silicon thin-film transistors (Poly-Si TFTs) have been studied and applied in many applications, such as active matrix liquid crystal displays [1] and memory devices [2]. Recently, poly-Si TFTs utilizing nanowire (NW) channel with multiple-gate structures have been demonstrated to meet demands in both TFT performance and suppression of short channel effects encountered during scale-down [3]–[5]. Although gate controllability was enhanced through multiple-gate structures, defects at grain boundaries and dangling bonds in the poly-Si NW channel undermine the carrier mobility and the device switching speed [6]. Different techniques such as solid-phase crystallization (SPC) [7], metal-induced-lateral crystallization [8], and excimer laser annealing [9] have been proposed to increase the grain size so that trap-state density can be reduced. Plasma treatment has also been demonstrated to reduce the defect density [5], [10]. In addition, reduction of defect density and improvement of gate controllability via scale-down of the poly-Si NW channel have been reported. Some studies have even demonstrated the scale-down of the poly-Si NW without using advanced lithographic tools and have obtained excellent device characteristics [11]–[14]. Poly-Si NW TFTs with small gate length (< 0.1 μm) and very thin dielectrics have also been proposed to improved transfer characteristics [15], [16]. However, short-channel effects (SCEs) like large leakage current and drain-induced barrier lowering (DIBL) have emerged as problems. Therefore, poly-Si TFT with the GAA structure still suffers from intrinsic defects in the poly-Si channel. In this letter, we present a novel modified sidewall spacer process to prepare poly-Si NW TFTs with a gate-all-around (GAA) structure. The nanowire channel exhibits SCL structure after SPC process. Without any trap-reduced plasma treatment, the GAA SCL poly-Si NW TFTs possessing channels of high surface-to-volume ratio and a 0.25-μm gate length exhibited superior channel controllability and the ability to suppress SCEs.

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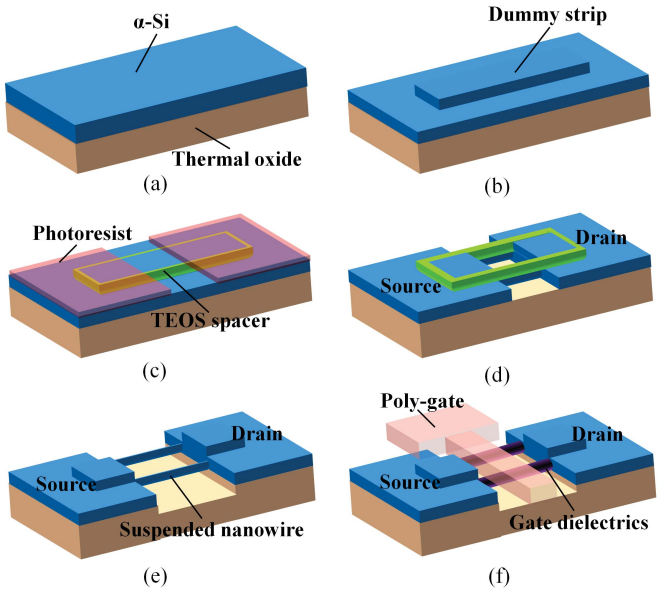

Fig. 1. (a)–(f) Key process flow of device fabrication using the simplified sidewall spacer technique.

II. Device Fabrication

The GAA SCL poly-Si NW TFTs were fabricated by a simplified top-down sidewall spacer technique, with the key process flow shown in Fig.1. Wafers with 500-nm thick thermal oxide were grown as the starting substrate layer, and a 70-nm thick amorphous silicon (α-Si) layer was deposited using low pressure chemical vapor deposition (LPCVD) at 550 °C [Fig. 1(a)]. Next, the α-Si layer was patterned into a mesa structure through optical lithography, which was followed by reactive ion etching (RIE). The α-Si layer was transformed into two parts; the thicker part served as a

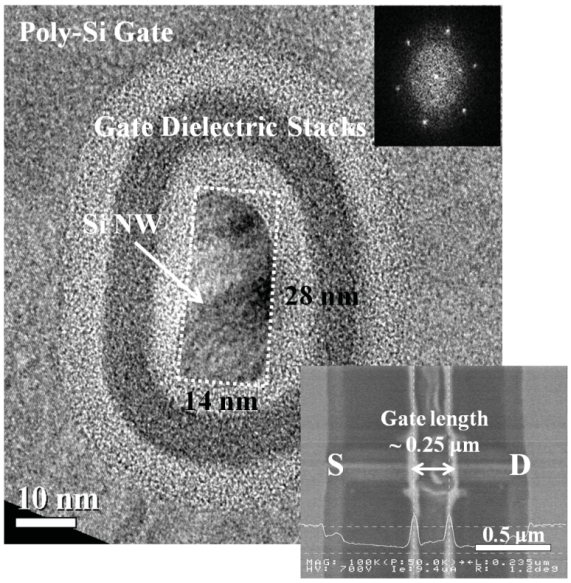

Fig. 2. Cross-section TEM image of a GAA SCL poly-Si NW TFT. The NW was surrounded by gate dielectric stacks (ONO = 5 nm/8 nm/8 nm) and a poly-Si gate. Upper inset: FFT patterns confirming the zone axis of the Si NWs is in the [110] direction. Lower inset: SEM image confirming the gate length of the GAA SCL poly-Si NW TFT is around 0.25 μm.

dummy strip, and the thinner one served as device active layer [Fig. 1(b)]. A 60-nm thick tetraethylorthosilicate (TEOS) layer was deposited using LPCVD, and then etched through RIE, leaving TEOS spacers. Before NW formation, the source and drain (S/D) regions were defined through an I-line stepper [Fig. 1(c)]. Next, the α-Si layer was etched through high-selective RIE, and the NWs were formed through TEOS hard masks [Fig. 1(d)]. After NWs formation, the TEOS hard masks were removed in 1:50 diluted HF solution. Next, the SPC was performed at 600 °C for 24 h in nitrogen ambient to turn the α-Si into polycrystalline silicon. Then the NWs were released from the bottom thermal oxide during the RCA cleaning [Fig. 1(e)]. The TEOS oxide/ nitride/ TEOS oxide (O/N/O = 5 nm/ 8 nm/ 8 nm) gate dielectric stacks and a 200-nm in situ N^+doped poly-Si film were placed surrounding NWs by using LPCVD conformal deposition. After the patterning of the poly-Si gate [Fig. 1(f)], the wafers were doped with phosphorus for the S/D at a dose of 5×10^{15} cm^{-2} (10 keV) through self-aligned implantation to reduce the contact resistance and the series resistance of the S/D access regions. A 300-nm thick TEOS layer was deposited as the passivation layer using LPCVD. Then, samples were activated at 600 °C for 8 h in nitrogen ambient. The contact holes were defined, and Al metallization was performed. Finally, the wafers were sintered at 450 °C in a mixture of hydrogen (5%) and nitrogen (95%) ambient for 30 min. Despite the fact that the O/N/O gate stack undermines gate controllability, this poly-Si NW TFT device with surrounding ONO layers were prepared for potential memory applications.

III. Results and Discussion

Fig. 2 presents the high-resolution TEM channel cross-section image of a GAA SCL poly-Si NW TFT. The NW channel is surrounded by ONO stacks (TEOS/nitride/TEOS = 5 nm/8 nm/8 nm) and a poly-Si gate with channel width ~14 nm and thickness ~28 nm. The upper inset is fast Fourier transform (FFT) patterns confirming that the zone axis of the Si NWs is the [110] direction. The FFT pattern also shows that the Si NWs are highly crystalline. The lower inset SEM image confirms that the gate length of GAA SCL poly-Si NW TFT is ~0.25 μm. In the process flow, the TEOS oxide was used as a sidewall hard mask instead of traditional silicon nitride hard mask. Without using the time-consuming wet etching process to remove silicon nitride and the additional dummy layer material, GAA SCL poly-Si NWs can be prepared efficiently with an improved device yield.

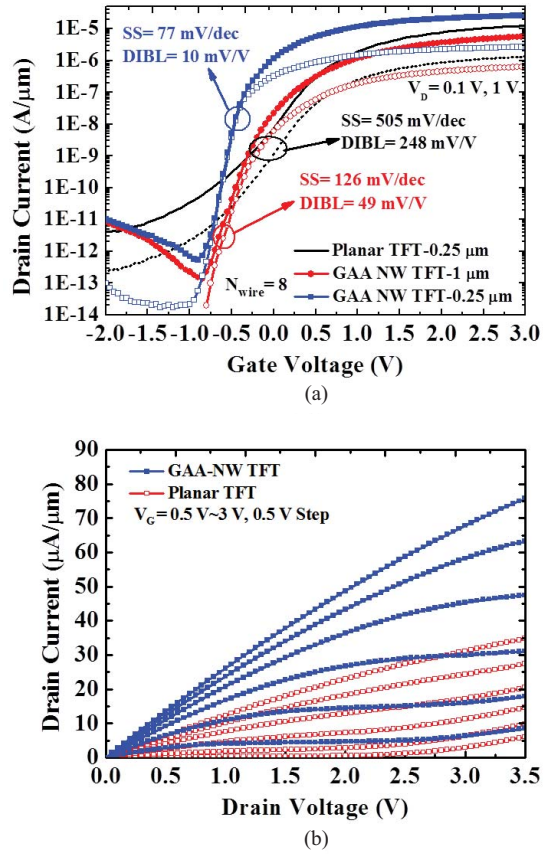

Fig. 3. (a) Transfer characteristics for a GAA SCL poly-Si NW TFT (gate lengths of 0.25 μm and 1 μm) and conventional planar TFT. (b) Comparison of output characteristics between the GAA SCL poly-Si NW TFT and conventional planar TFT.

Fig. 3(a) presents a comparison of the normalized transfer characteristics (I_D–V_G curve) between the GAA SCL poly-Si NW TFT and a planar TFT without any plasma-related treatment. The gate lengths of the TFTs were 0.25 μm, and the effective width of the GAA SCL poly-Si NW and planar TFTs were 0.672 μm (84 nm × 8) and 1.1 μm, respectively. The GAA SCL poly-Si NW TFT exhibits a threshold voltage of ~−0.4 V at $I_D = (W_{eff}/L) \times 10^{-8}$ A and $V_D = 0.1$ V. An analysis of 24 TFTs showed that the GAA SCL poly-Si NW TFT exhibits a very small subthreshold swing (90 ± 15 mV/dec, extracted from $I_D = 10^{-8}$ A to $I_D = 10^{-12}$ A and $V_D = 0.1$ V), one which is superior to that of the planar

TABLE I
CHARACTERISTICS OF RECENTLY REPORTED POLY-SI NW TFTs USING SPC TECHNIQUE

Source	This Letter	[5]	[14]	[15]	[16]
Gate structure	GAA	GAA	Double-gated	Ω−gate	Ω−gate
Gate length (μm)	0.25	2	1	0.1	0.09
Channel dimension (nm^2)	14 × 28	75 × 38	18 × 72	14 × 17	20 × 10
NH_3 plasma treatment	W/O	1 h	3 h	W/O	W/O
EOT (nm)	18	20	20	1.7	10 (HfO_2)
S.S. (mV/dec)	90 ± 15	114	115	79	113
DIBL (mV/V)	21 ± 13	13	60	78	251
I_{ON}/I_{OFF} V_G; V_D	$>10^7$ 3 V; 1 V	$>10^8$ 6 V; 3 V	$>10^7$ 6 V; 3 V	$>10^4$ 1 V; 1 V	$>10^7$ 6 V; 1 V

device (396 ± 57 mV/dec). Furthermore, the DIBL of the GAA SCL poly-Si NW and planar TFTs are 21 ± 13 mV/V and 237 ± 97 mV/V (extracted from $\Delta V_{gs}/\ \Delta V_{ds}$ of $V_D = 0.1$ and 1 V at $I_D = 10^{-10}$ A), respectively. Furthermore, we suspect that large variations in both SS and DIBL could be further improved by increasing the grain size under the gate. The 0.25-μm planar device exhibits SCEs, including a large SS and a clear DIBL due to inferior gate controllability. However, the 0.25-μm GAA poly-Si NW TFT shows gate-induced leakage current (GIDL) in the OFF state as the result of stronger electric field between the gate and drain. The transfer characteristics of a 1-μm GAA poly-Si NW TFT are also shown in Fig. 3(a). Despite the 1-μm device exhibiting a lower leakage current, the 0.25-μm device exhibits superior transfer characteristics owing to the short gate length and the reduction of grain boundaries under the gate area. We suspect that the gate length between 0.1 μm and 0.25 μm may be an appropriate length for further improvement of device characteristics. Fig. 3(b) presents a comparison of output characteristics between GAA SCL poly-Si NW and conventional planar TFTs. The proposed NW device exhibits a saturation current improvement of 223% at $V_G = 3$ V and $V_D = 3.5$ V (NW TFT ∼76 μA/μm over the planar device ∼34 μA/μm). Table I shows a performance summary for the recently reported poly-Si NW TFTs using the SPC technique [5], [14]–[16]. Poly-Si NW TFTs with low SS and high ON/OFF current ratio were most usually subjected to NH_3 plasma treatment. In the absence of a lightly doped drain, devices with a gate length smaller than 0.1 μm usually suffered from SCEs. However, this GAA SCL poly-Si NW TFT with a 0.25-μm gate length and a very small NW channel (14 × 28 nm^2) exhibited single-crystal like electrical properties.

IV. CONCLUSION

We characterized GAA SCL poly-Si NW TFTs prepared by a novel modified side-wall spacer technique. Without the need for plasma treatment, the GAA SCL poly-Si NW TFTs showed an excellent S.S. (90 ± 15 mV/dec), a very small DIBL (21 ± 13 mV/V), and a high ON/OFF current ratio $\sim 7 \times 10^7$ at a relatively low voltage condition ($V_G = 3$ V and $V_D = 1$ V), resulting from the very small channel and the reduction of grain boundaries and defects under the gate area.

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