Improving Electrical Properties of Bottom-Gate Poly(3-Hexylthiophene) Thin-Film Transistor Using CF_4 Plasma Treatment

Hung-Chi Wu and Chao-Hsin Chien

***Abstract*—In this letter, the effect of CF_4 plasma treatment on poly(3-hexylthiophene)-based organic thin-film transistors has been investigated. It was found that CF_4 plasma treatment on the source/drain electrode can reduce contact resistance and increase mobility. The CF_4 plasma treatment can increase the mobility from 0.0021 to 0.0102 $cm^2/V \cdot s$ and decrease the contact resistance by about 70%. Moreover, the CF_4 plasma treatment is compatible with the bottom-gate bottom-contact structure without degrading the SiO_2 layer.**

***Index Terms*—Organic thin-film transistors (OTFTs), plasma treatment, poly(3-hexylthiophene) (P3HT).**

I. Introduction

SEMICONDUCTING π-conjugated polymers have attracted the attention in the last several decades due to many advantages. For example, they can be fabricated with low cost and low energy consumption. Moreover, they have excellent mechanical flexibility and the ability of large-area coverage [1]. There are many applications for semiconducting polymers such as organic thin-film transistors (OTFTs), light-emitting diodes, electronic paper, radio frequency identification tags, and chemical or biological sensors [2], [3].

Compared with other semiconducting π-conjugated polymers, regioregular poly(3-hexylthiophene) (P3HT) has relatively high field-effect mobility $(0.001-0.01\ cm^2/V \cdot s)$ and reasonable on/off ratio (10^3-10^6). Therefore, P3HT is one of the most promising materials. However, there are still many challenges needed to be overcome for the real applications. For example, P3HT cannot endure high temperature, and its crystallinity by spin cast is worse. Also, the interface between metal electrodes and semiconducting polymers (M/S) is more complex than that of the conventional a-Si TFT [4]. High contact resistance of the M/S interface will certainly degrade the performance of the devices [5]–[7]. In this letter, we have found that the contact resistance can be significantly reduced by the CF_4 plasma treatment. This approach can enhance the quality of the M/S interface and improve electrical performances of P3HT OTFTs.

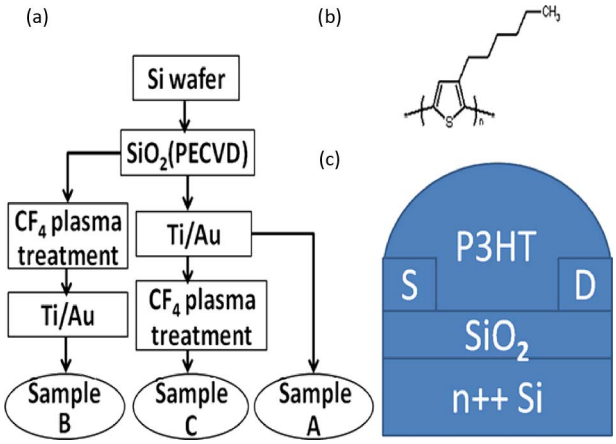

Fig. 1. (a) Outline of process flow. (b) Chemical structure of P3HT. (c) Device structure in this letter.

II. Device Fabrication

Fig. 1(a) shows the outline of the process flow. Heavily doped n-type Si wafer was used as a substrate. A 200-nm-thick SiO_2 layer was grown on the Si wafer by plasma-enhanced chemical vapor deposition after standard RCA cleaning. Moreover, the backside of the Si wafer was deposited with Al by thermal evaporation. Then, we divided the samples into three categories—samples A, B, and C. Sample A is the control one without plasma treatment, and sample B is the one exposed to the CF_4 plasma treatment with $CF_4 = 50$ SCCM at 500 mtorr and 300 °C for 90 s right after SiO_2 deposition. Subsequently, we defined the channel length and width by photolithography and deposited Ti/Au (20/500 Å) as source/drain (S/D) electrodes by thermal evaporation. Then, sample C was treated by the CF_4 plasma treatment after the S/D formation. All samples were cleaned by acetone–isopropyl alcohol–deionized water with ultrasonic system. Then, the surface was converted into hydrophobic surface with hexamethyldisilazane (HMDS) in a vacuum oven at 150 °C. The P3HT was purchased from Uni-Region, Inc., and the chemical structure is shown in Fig. 1(b). The molecular weight is 50 000, and the ratio of head–tail to head–head and tail–tail is 98+%.

Chloroform $(CHCl_3)$ was used as a solvent. P3HT was dissolved in $CHCl_3$, and its concentration was 0.25 wt%. The

Manuscript received December 13, 2012; revised January 11, 2013; accepted January 29, 2013. Date of publication March 7, 2013; date of current version March 20, 2013. The review of this letter was arranged by Editor S. J. Koester.

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Digital Object Identifier 10.1109/LED.2013.2244840

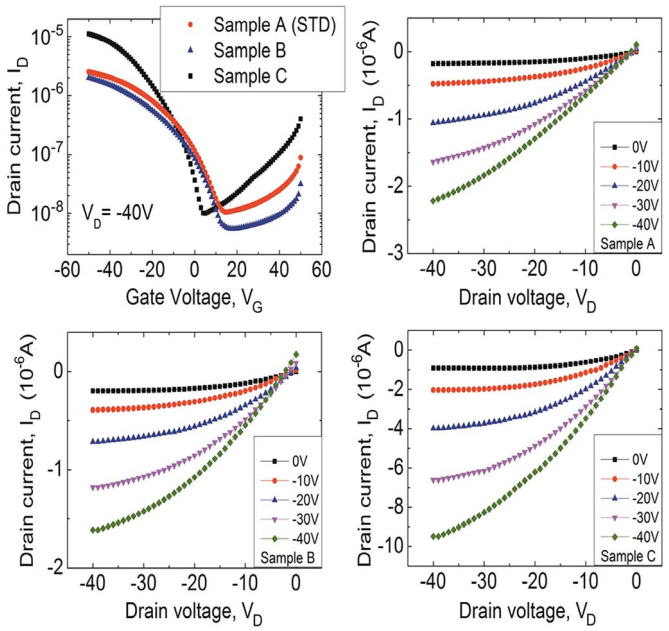

Fig. 2. Transfer and output characteristics of samples A, B, and C (device channel $W/L = 3700/50\ \mu$m).

P3HT active layer was fabricated by spin cast with two steps, i.e., 1000 rpm for 10 s in the first step and 2000 rpm for 30 s in the second step. The samples were annealed in furnace at 200 °C with 10-L N_2 for 30 min. The device structure is shown in Fig. 1(c). The electrical properties were measured by Hewlett–Packard 4156C. The P3HT thin films were characterized by atomic force microscope (AFM; Veeco D3000), X-ray diffraction (XRD; Bede D1), and contact angle measurement system (KRUSS GH100).

III. Results and Discussion

Fig. 2 shows the transfer and output characteristics of the OTFTs. Both off- and on-currents of sample B slightly decrease in comparison to those of sample A, while on-current of sample C increases remarkably albeit with a slight increase in off-current. The mobility in the saturated regime is extracted based on the conventional Si MOSFET current model [8]

$$I_D = \frac{W\mu C_i}{L}\left[(V_G - V_T)^2\right]$$

where W is the transistor channel width, L is the transistor channel length, C_i is the capacitance per unit area of the gate insulator (SiO_2), μ is the field-effect mobility, V_T is the threshold voltage, and I_D, V_D, and V_G are the drain current, drain voltage, and gate voltage, respectively. The mobilities of samples A, B, and C are 0.0021, 0.0015, and 0.0102 $\text{cm}^2/\text{V}\cdot\text{s}$, respectively. Sample C depicts near five times mobility improvement and sample B shows slightly inferior mobility as compared to sample A. Comparing output characteristics of all samples, we found that all samples show a saturation region at large V_D but curves with different gate biases come close together at small V_D except sample C. It means that the contact resistances of samples A and B are larger than that of sample C. I_D offset of sample B is more serious than those of samples A and C. It

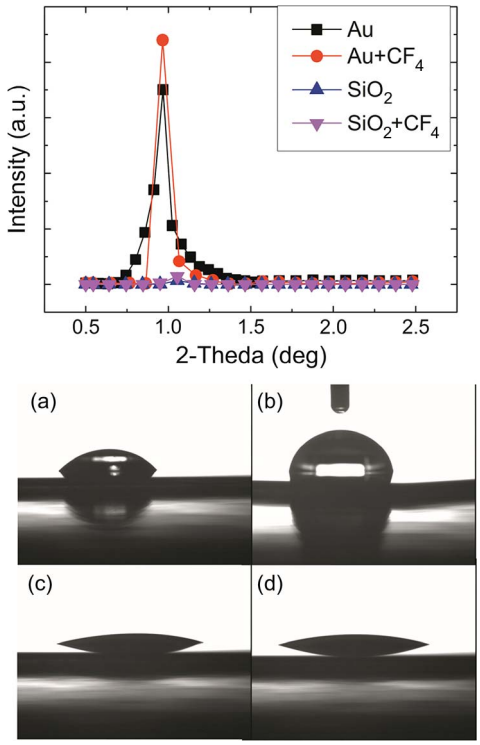

Fig. 3. (Top) XRD spectra of P3HT thin film on different surfaces. (Bottom) Images of water drop on the surface of (a) Au, (b) Au with CF_4 plasma treatment, (c) SiO_2, and (d) SiO_2 with CF_4 plasma treatment.

should be noted that I_D offset is closely related to gate leakage. Therefore, we think that CF_4 plasma treatment would degrade the SiO_2 property. The V_T's of samples A, B, and C are 9.98, 9.71, and 3.32, respectively. We also checked the C–V curve of a MOS structure (not shown); the CF4 plasma treatment can make V_T shift about 3 V. The reason about small V_T for sample C would be explained in the coming discussion. Also, we examined the thickness of the SiO_2 layer with and without the plasma treatment by the thickness analyzer (N&K 1200). The SiO_2 thickness decreased from 2013 to 1982 Å, which was a negligible change. Hence, we rule out the possibility that the device performance improvement results from the SiO_2 thickness reduction.

Therefore, the plausible reason is the reduced S/D contact resistance. We used transfer line method [9] by using devices with different lengths (10, 25, 50, and 100 μm) but the same width to measure their resistance under low-drain-voltage application and extracted their contact resistance. The contact resistances for samples A, B, and C are 1.82×10^6, 3.20×10^6, and $5.71 \times 10^5\ \Omega\cdot$cm, respectively. Sample B has larger contact resistance than sample A, while the contact resistance of sample C significantly reduces. It means that the injection barrier height is lowered after CF_4 plasma treatment. This result echoes the assertion that the injection from the source to the P3HT layer is the most critical step in the carrier transportation [10]–[14]. The carrier transportation is faster in intramolecule than in intermolecule, and the carrier injection from the source electrode to the P3HT layer is the most important step during carrier transportation in OTFTs. Therefore, the CF_4 plasma treatment can improve the S/D surface, lead to the injection barrier lowering, and improve the mobility effectively.

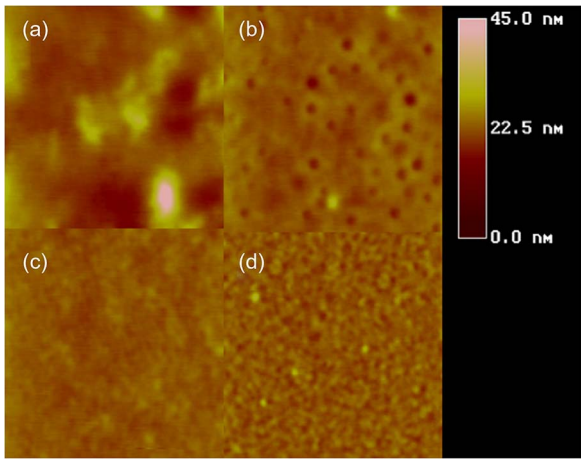

Fig. 4. AFM images of P3HT layers on (a) SiO_2 surface with CF_4 plasma treatment, (b) SiO_2 surface, (c) Au surface with CF_4 plasma treatment, and (d) Au surface.

To rule out the effect of HMDS treatment, we characterize the Au and SiO_2 surface by material analysis. Fig. 3 shows the XRD spectra of P3HT deposited on the different surfaces. The P3HT thin film on the Au has much better crystallinity than that on the SiO_2 whether we use the CF_4 plasma treatment or not. It can be found that the crystallinity can be improved by the CF_4 plasma treatment since the curves become narrower. The contact angles of Au, Au with CF_4 plasma treatment, SiO_2, and SiO_2 with CF_4 plasma treatment are 47.1°, 77.3°, 14.8°, and 15.3°, respectively. It means that the Au surface with CF_4 plasma treatment is in favor with P3HT deposition. The good interface between P3HT and Au can decrease the difficulty of carrier injection. Furthermore, it could be an explanation of the V_T difference between samples A and C. Fig. 4 shows the AFM images of P3HT thin films on different surfaces. The roughness of the P3HT thin film on the SiO_2 increases from 1.44 to 3.66 nm, while the roughness on the Au decreases from 1.21 to 0.98 nm after the CF_4 plasma treatment. From the electrical and material analysis, the P3HT OTFTs have better electrical performances such as mobility and subthreshold swing after the CF_4 plasma treatment on Au electrodes.

IV. Conclusion

In summary, we have investigated the effect of CF_4 plasma treatment on the performance of P3HT TFTs. The CF_4 plasma treatment can improve the interface between Au and P3HT. It makes better crystallinity of P3HT near S/D electrodes and reduces the contact resistance. The CF_4 plasma treatment can form better contact between the Au and P3HT layers and enhance the field-effect mobility effectively. The CF_4 plasma treatment is compatible with the bottom-gate bottom-contact structure without degrading the SiO_2 layer.

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