Germanium N and P Multifin Field-Effect Transistors With High-Performance Germanium (Ge) p^+/n and n^+/p Heterojunctions Formed on Si Substrate

Che-Wei Chen, Cheng-Ting Chung, Ju-Yuan Tzeng, Pin-Hui Li, Pang-Sheng Chang, Chao-Hsin Chien, and Guang-Li Luo

***Abstract*— We demonstrate the characteristics of p^+-Ge/n-Si and n^+-Ge/p-Si heterojunction diodes formed by heteroepitaxial Ge grown on Si leading to high performance and very low leakage current. The ON/OFF current ratio of the p^+-Ge/n-Si and n^+-Ge/p-Si heterojunction was $>10^7$ and $>10^6$, respectively. The OFF current density was extremely low at <10 μA/cm^2 for the p^+-Ge/n-Si formed with different implantation energies of 10 $\sim$ 40 KeV and $\sim$20 μA/cm^2 for the n^+-Ge/p-Si with different implantation energies of 20 $\sim$ 50 KeV at a reverse bias of $|V_R| = \pm 1$ V, respectively. Both p and n-Ge channel multifin field-effect transistors (FinFETs) were formed by a mesa structure using these p^+-Ge/n-Si and n^+-Ge/p-Si heterojunctions. A high-κ/metal gate stack was employed. The body-tied Ge multifin FinFET with a fin width (W_{Fin}) of $\sim$40 nm, and the channel length ($L_{Channel}$) was 150 nm for p-FinFET and of 110 nm for n-FinFET, exhibiting a driving current of 174 μA/μm at $V_G = -2$ V and 102 μA/μm at $V_G = 2$ V, respectively. This is the first experimental demonstration of a body-tied high mobility Ge channel multifin FinFET using a top-down approach.**

***Index Terms*— Body-tied, germanium, multifin field-effect transistors (FinFETs), silicon p^+-Ge/n-Si heterojunction, n^+-Ge/p-Si heterojunction**

I. Introduction

In THE past decade, Germanium (Ge) has been investigated as a high-mobility channel material as a substitute for silicon channels in order to continuously boost the ON current (I_{on}) of MOSFETs. One of the concerns, however, is a small band gap ($Eg = 0.67$ eV) owing to the presence of band-to-band tunneling (BTBT) leakage current at the drain junction when a high electric field exists [1], [2]. However, when the device is scaled down to a short-channel region, especially at the level of nanometer dimensions, the junction leakage becomes more severe because a stronger electric field exists, caused by the higher substrate-doping concentration [3]. Moreover, the source/drain (S/D) junctions of Ge MOSFETs need to be designed carefully for the purpose of parasitic resistance reduction and short-channel effect control [4] in advanced devices such as multifin field-effect transistors (FinFETs). However, n-type dopants in Ge diffuse extraordinarily fast [5], and possess relatively low dopant solubility [6]. These two features make the formation of shallow junctions with sufficiently low resistance very challenging. Moreover, the presence of Fermi level pinning in the metal/n-Ge contact has been reported, which leads to large contact resistance [7]. This effect will also contribute to the magnitude of parasitic resistance and in turn deteriorate the ON current of the Ge-channel transistor. Therefore, making a high-performance Ge-n-FET is rather challenging. On the other hand, integrating Ge devices onto a Si wafer is very attractive from the viewpoint of cost control and the range of platforms already built on Si, despite the $\sim$4.2% lattice mismatch existing between Ge and Si. Thus, depositing high-quality epitaxial Ge film with minimum defect density is also very hard. This is why in the previous studies, the heterojunction diodes always showed low I_{ON}/I_{OFF} ratios and high-leakage current densities [8], [9].

In our previous works [10], [11], we reported that the Ge p-channel FinFET (p-FinFET) was successfully fabricated directly on the Si and Si-on-insulator (SOI) substrate. The low leakage current of p^+/n and n^+/p heterojunctions were also investigated [12]. We suppose that most of the junction depletion region was built inside the Si side, which can restrain the BTBT-leakage current in Ge and then can lead extremely low junction-leakage current. However, fabrication of nonplanar CMOS FinFETs has not yet been demonstrated in the published literature. The nonplanar FET is very attractive for future applications since it has better channel potential control ability to cope with the short-channel effects (SCEs) [13], [14]. Certainly, there are still a lot of challenges that need to be overcome in integrating Ge FinFET on top of the Si wafer before mass production. In this paper, we illustrate p^+-Ge/n-Si and n^+-Ge/p-Si heterojunction diodes with a very high I_{ON}/I_{OFF} ratio and very low leakage current using

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C.-W. Chen, C.-T. Chung, J.-Y. Tzeng, P.-H. Li, and P.-S. Chang are with the Department of Electronics Engineering and the Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan (e-mail: leo2591738@gmail.com; cody0926@gmail.com; ytps5105@hotmail.com; kobe8422.ee96@g2.nctu.edu.tw; bc299168@gmail.com).

C.-H. Chien is with the Department of Electronics Engineering and the Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan, and also with the National Nano Device Laboratories, Hsinchu 30078, Taiwan (e-mail: chchien@faculty.nctu.edu.tw).

G.-L. Luo is with the National Nano Device Laboratories, Hsinchu 30078, Taiwan (e-mail: glluo@ndl.narl.org.tw).

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heteroepitaxial growth of Ge integration on the Si substrate. Combining p^+-Ge/n-Si and n^+-Ge/p-Si heterojunction diodes with a high-κ/metal gate stack, we demonstrate both n and p-Ge channel multifin FinFETs with high driving current. The illustrative structure is shown in Fig. 1(a). The p- and n-FinFET depict high driving currents of 174 μA/μm at $V_G = -2$ V with $L_{Channel}$ of 150 nm and 102 μA/μm at $V_G = 2$ V with $L_{Channel}$ of 110 nm, respectively.

II. Experiments

Undoped Ge films with thicknesses of 120 and 160 nm were grown on the n- (2 $\sim$ 7 ohm-cm) and p-type (15 $\sim$ 25 ohm-cm) 6-in Si(100) substrates, respectively, using ultrahigh vacuum chemical vapor deposition after a standard cleaning. The films were baked at 900 °C for 10 min in a high-vacuum ambient to desorb Si surface native oxide before Ge was deposited. After Ge deposition, the postdeposition annealing (PDA) was performed at 900 °C for 10 min without a vacuum break in order to reduce dislocation, owing to lattice mismatch between Si and Ge. According to a previous study, 900 °C annealing is capable of effectively reducing the threading dislocation density and improving single crystalline Ge-film quality [15].

In order to avoid the channeling effect, an oxide of 10-nm thickness was deposited by plasma-enhanced chemical vapor deposition (PECVD) on the Ge surface before an implanted region was defined. Various dopant energy of boron ions (10, 20, 30, 40 keV, 1×10^{15} cm^{-2}) and phosphorus ions (20, 35, 50 keV, 1×10^{15} cm^{-2}) were respectively implanted in the active area with 120- and 160-nm Ge, and subsequently a 100-nm PECVD oxide was deposited for restraining dopant outdiffusion during a rapid thermal annealing (RTA) process. The implantation energy was 20 keV for p-FinFETs and 35 keV for n-FinFETs, respectively. Activation was performed in nitrogen ambient for 10 s at 500 °C (p^+-Ge/n-Si) and for 10 s at 600 °C (n^+-Ge/p-Si) to form the Ge/Si heterojunction diode as an S/D of CMOS devices. A heterojunction area (625 μm^2) and multifin channel structure was formed by using reactive ion etch (RIE) anisotropic etching in Cl_2/HBr ambient using oxide as a hard mask after patterns were performed by lithography. At the same time, a Si substrate was also etched slightly by chlorine until the etching was stopped at the Si substrate. The spin on glass (SOG) was coated ($\sim$650 nm) and etched back for device isolation after removing oxide and dilute hydrofluoric cyclic surface cleaning. The GeO_2 was used as a surface passivation layer using rapid thermal oxidation (RTO) at 520 °C for 30 s and then an Al_2O_3 high-κ dielectric deposition was performed by atomic layer deposition. In particular, the utility of thermally grown GeO_2 as a good electrical passivation layer for high-κ dielectrics was investigated [16]–[20]. The metal gate Ti (5 nm)/Pt (100 nm) was deposited by sputtering, and a lift-off process was performed. Metallization Ti (5 nm)/Pt (50 nm) contact for p^+-Ge/n-Si and Ti (5 nm)/Au (50 nm) contact for n^+-Ge/p-Si heterojunction were deposited by sputtering and a lift-off process as well. Finally, a back-metal contact Al was carried out by thermal evaporation. Both p^+-Ge/n-Si and n^+-Ge/p-Si heterojunction diodes and the body-tied Ge FinFET CMOS devices were created. All patterns were defined by electron-beam system and a Keithley 4200 was used to measure electrical characterization.

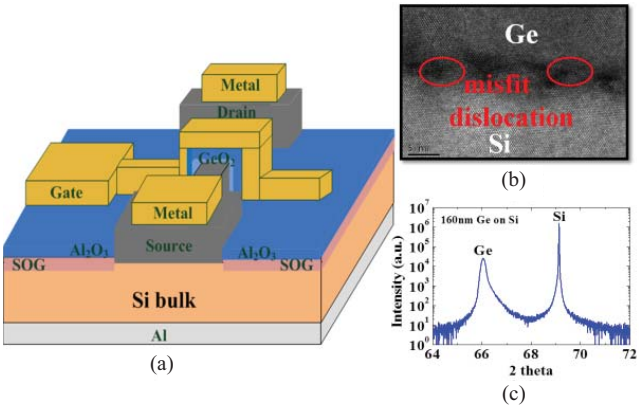

Fig. 1. (a) Schematic illustration of Ge-channel multifin FinFET. (b) TEM image of a Ge/Si interface showing the existence of a misfit dislocation density. (c) XRD of 160-nm Ge on Si with postdeposition annealing.

III. Heterojunction Diodes

Fig. 1(b) shows the transmission electron microscopy (TEM) image of crystalline Ge film on Si. The existence of misfit dislocations at the Ge/Si interface can be observed owing to the lattice mismatch. A uniform interface between Ge and Si was also seen, implying PDA does not result in the diffusion of Ge into Si. In the x-ray diffraction (XRD) rocking curve, as shown in Fig. 1(c), we saw that the intensity of the Ge peak was slightly higher and the full width half maximum was also narrower than those in the previous report [21], indicative of better Ge-film quality. Both suggest that high quality of single-crystalline Ge film had been grown directly on the Si wafer for the starting material.

Fig. 2(a) shows secondary ion mass spectrometry (SIMS) dopant profiles of the p^+-Ge/n-Si heterojunction diode with implantation energies of 10, 20, 30, and 40 KeV before and after RTA. The dashed line indicates the thickness of the epitaxial Ge film. After the RTA process, the depth profile of boron dopants were hardly redistributed, and no deeper diffusion was observed. This result was similar to that in the previous report [22]; the pairing of boron with the defects has a high binding energy so that the atoms are almost immobile at each level of implantation energy. Moreover, we think most of the dopants residing in the Si region remain inactive since the thermal energy of low-temperature RTA used in this work was insufficient to activate the dopants. As a result, a similar leakage current level of the diodes with four implantation energies was obtained. Fig. 2(b) shows the SIMS-dopant profiles of the n^+-Ge/p-Si heterojunction diode. A slight diffusion of phosphorous dopants was observed after the annealing due to the relatively higher thermal budget required for the n-type dopant activation in Ge [23]. Upon prolonged annealing, P is more likely to precipitate, and the profile of the junction tends to become more graded [24].

Thermal annealing for reducing the threading dislocation density is known to enhance device performance and lead to an OFF current reduction [25]. Moreover, a good passi-

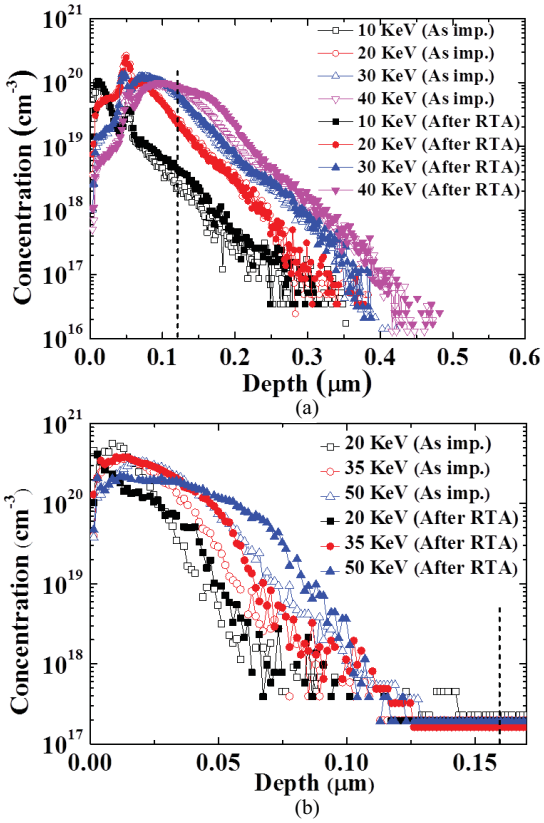

Fig. 2. (a) SIMS depth profile of the p^+-Ge/n-Si heterojunction diode with 10 ~ 40 KeV implantation energies and RTA (500 °C 10 s in N2 + 520 °C 30 s in O_2). (b) SIMS depth profile of the n^+-Ge/p-Si heterojunction diode with 20 ~ 50 KeV implantation energies and RTA (600 °C 10 s in N2 + 520 °C 30 s in O_2). The dashed line indicates the epi-Ge layer thickness.

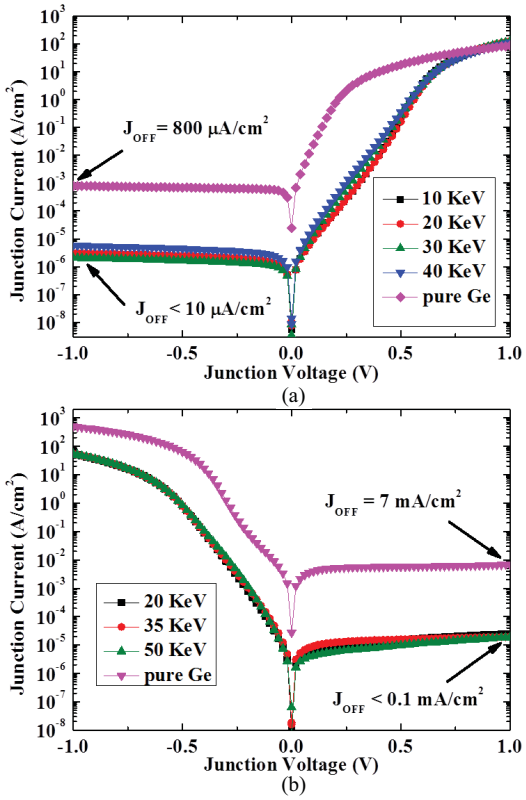

Fig. 3. (a) *I–V* characteristics of p^+-Ge/n-Si heterojunction diode with high $I_{ON}/I_{OFF} > 10^7$ with various implantation energies of 10 ~ 40 KeV and a pure Ge p^+/n homojunction for comparison. (b) *I–V* characteristics of n^+-Ge/p-Si heterojunction diode with high $I_{ON}/I_{OFF} > 10^6$ with various implantation energies of 20 ~ 50 KeV and a pure Ge n^+/p homojunction for comparison.

vation is also required for fabricating Ge diodes with sufficiently low OFF current density [26], [27] because the surface leakage current can be eliminated [28]. We fabricated the p^+-Ge/n-Si and n^+-Ge/p-Si heterojunction diodes with the GeO_2 surface passivation by RTO at 520 °C for 30 s and SOG isolation. The different implantation energies varied from 10 to 40 keV for p^+-Ge/n-Si and from 20 to 50 keV for n^+-Ge/p-Si heterojunctions in order to examine the corresponding variation of the leakage current. Pure Ge p^+/n and n^+/p junction diodes were also made for comparison; GeO_2 was formed by the same condition of 520 °C for 30 s and removed during the contact-holes formation. As a result, as shown in Fig. 3(a), the p^+-Ge/n-Si heterojunction diode depicts a very high $I_{ON}/I_{OFF} > 10^7$ and an extremely low OFF current density (<10 μA/cm^2 at $V = -1$ V) no matter what implantation energy was used. The pure Ge p^+/n homojunction showed the I_{ON}/I_{OFF} of $\sim 10^5$ and I_{OFF} of 800 μA/cm^2 at $V = -1$ V. Strikingly, the leakage current of heterojunction is about two orders of magnitude smaller than that of pure Ge p^+/n junction, even though the misfit dislocations have been seen at the Ge/Si interface. On the other hand, the BTBT leakage current in Ge was effectively suppressed due to the fact that most of the depletion region was built inside the n-Si side for every implantation energy. The ideality factor ~1.1 of our p^+-Ge/n-Si heterojunction was extracted. Recently, there are many articles focusing on the Ge-junction diode being published. Yu *et al.* [29] also reported the selective growth method epi-Ge p^+/n junction diode on the Si using the selective multiple hydrogen anneals by heteroepitaxial (MHAH) technique. The diode had an OFF current density of $>10^{-4}$ A/cm^2 at $V = -1$ V and $I_{ON}/I_{OFF} < 10^4$. Park *et al.* [8] reported the Ge p^+/n junction diode on the Si substrate using metal-induced dopant activation (MIDA) technique with $I_{ON}/I_{OFF} \sim 2.1 \times 10^4$ in which I_{OFF} was >1 mA/cm^2 at $V = -1$ V.

Fig. 3(b) shows the electrical characteristic of n^+-Ge/p-Si heterojunction diodes with high $I_{ON}/I_{OFF} > 10^6$ and a low OFF current density ~20 μA/cm^2 at $V = 1$ V with implantation energies of 20, 35, and 50 KeV. The pure Ge n^+/p homojunction showed I_{ON}/I_{OFF} of $\sim 10^5$ and I_{OFF} of 7 mA/cm^2 at $V = 1$ V. The leakage current level of n^+-Ge/p-Si heterojunction is two orders of magnitude lower than that of the pure Ge homojunction due to the fact that Si has a relatively large band gap. However, the ON current of the n^+-Ge/p-Si heterojunction was slightly lower than that of the pure Ge homojunction. We speculate that this is due to the fact that the defects in the phosphorus doped epitaxial Ge are very difficult to annihilate compared to those in the single crystalline Ge [4]. In the previous study, Park *et al.* [30] reported the Ge n^+/p junction diode formed on the Si substrate

by a Co technique with I_{ON}/I_{OFF} ~3.7×10^2, $I_{OFF} \sim 7 \times 10^{-1}$ A/cm^2 and $I_{ON} \sim 3 \times 10^2$ A/cm^2 at $V = \pm 1$ V. The OFF current density of our heterojunction was at least four orders of magnitude lower than that reported in the above literature. The ideality factor of our n^+-Ge/p-Si heterojunction was ~1.16 at low forward voltages. In modern advanced devices, the junction leakage indeed contributes to the OFF-state power consumption. Therefore, our heterojunction with extremely low OFF current density is very attractive from the viewpoint of power consumption. To demonstrate the uniformity of leakage current in the electrical performance, the cumulative probability versus leakage current density (at $V = -1$ V) is shown in Fig. 4. We can see that a tight control had been obtained since there was a very narrow distribution of leakage current density of p^+-Ge/n-Si heterojunction. No matter what implantation energy was used, the leakage current distributed between 2 and 6 μA/cm^2.

In order to explain why our diodes have exhibited such excellent properties, we think it is necessary to resort to the fundamental current conduction mechanisms of the pn diodes. As is well known, there are four possible primary origins of leakage current in a diode: 1) generation current within the space charge region; 2) diffusion current outside the space charge region; 3) generation of minority carriers at the surface in the periphery [31], [32]; and 4) BTBT current. We suppose that the surface generation current was restrained by the GeO_2 surface passivation because GeO_2/Ge system has much better interface quality. Meanwhile, the BTBT leakage current was effectively eliminated by the heterostructure since Si has a relatively large band gap. Therefore, we suggest that the generation current within the space charge region and the diffusion current outside the space charge region are the dominant factors. If $V \gg kT/q$, the magnitude of the generation current within the depletion region will be given by

$$I_{\text{gen}} = \frac{1}{2} q \frac{n_i}{\tau_0} W A \tag{1}$$

where q is the charge on an electron, n_i is the intrinsic carrier concentration, τ_0 is the minority carrier lifetime, W is the width of the depletion region, and A is the area of the heterojunction. We expect the generation current component to have the same temperature dependence as n_i, and it is dependent on the magnitude of the reverse bias. The generation current increases in proportion to W due to the fact that more centers are within the depletion region. From *I–V* curve, we saw that the OFF current was nearly independent of reverse bias. So, we can rule out the possibility that the leakage current is generated through the threading dislocations. On the other hand, there is no significant electric field present in the neutral regions and the minority carriers move by diffusion. The diffusion currents due to holes and electrons are described by

$$I_{\text{diff},p} = q D_p \frac{n_i^2}{N_D L_p} A \tag{2}$$

and

$$I_{\text{diff},n} = q D_n \frac{n_i^2}{N_A L_n} A \tag{3}$$

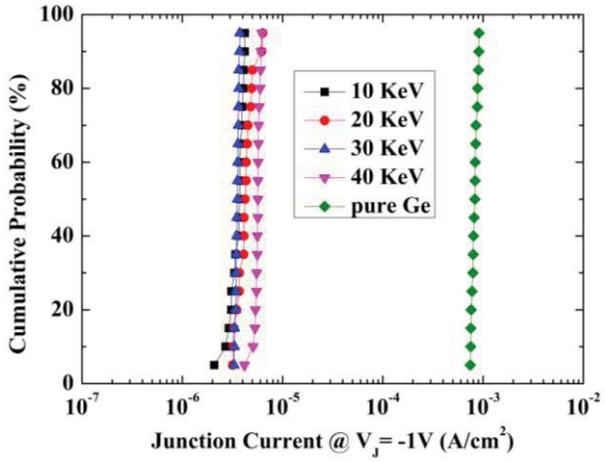

Fig. 4. Plot of cumulative probability versus leakage current density (at $V = -1$ V), showing tight control and narrow distribution of leakage current density of p^+-Ge/n-Si heterojunction.

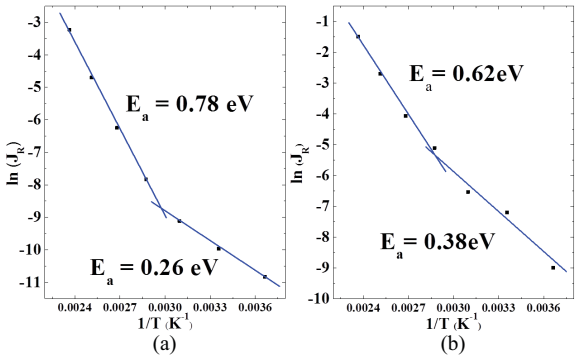

Fig. 5. Activation energies (E_a) estimated from the slope of the ln(J_R) versus $1/T$ plot of (a) p^+-Ge/n-Si and (b) n^+-Ge/p-Si heterojunction, respectively.

respectively, where D_p is the hole diffusivity, N_D is the donor impurity concentration, L_p is the diffusion length of holes in the n-region, and vice versa. No bias-dependent item is seen in these equations and the temperature dependence arises from the term of n_i^2.

The temperature dependence of *I–V* characteristic of the heterojunction diodes was measured in order to identify the carrier conduction mechanism. Fig. 5(a) and (b) shows the activation energies (E_a) of our diodes, which were estimated from the slope of the ln(J_R) at $V = \pm 1$ V versus 1/T plot of p^+-Ge/n-Si and n^+-Ge/p-Si, respectively. In Fig. 5(a), it was seen that there were two different slopes in the whole temperature range, representing different dominant conduction mechanisms. However, the temperature dependencies of the generation and diffusion current are known to come form n_i and n_i^2, respectively; at a higher temperature the feature of higher band gap material dominates the characteristic of the heterojunction pn diode [32]. The value of ~0.26 eV suggests that generation-recombination current of Ge is dominant at low temperatures. On the other hand, the value of ~0.78 eV suggests that the generation-recombination current of Si is dominant at high temperatures. From Fig. 5(b), a larger E_a (~0.38 eV) of n^+-Ge/p-Si heterojunction than that of

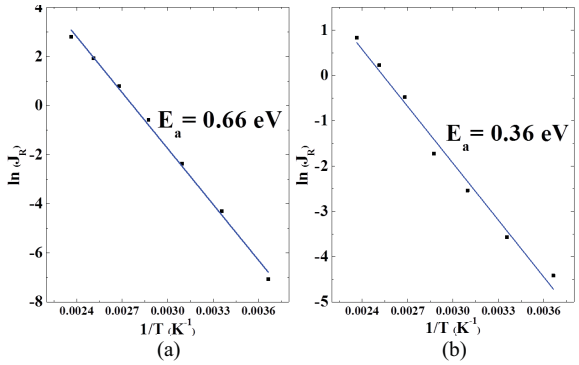

Fig. 6. Activation energies (E_a) of (a) p^+/n Ge and (b) n^+/p Ge homojunction as a function of temperature, respectively.

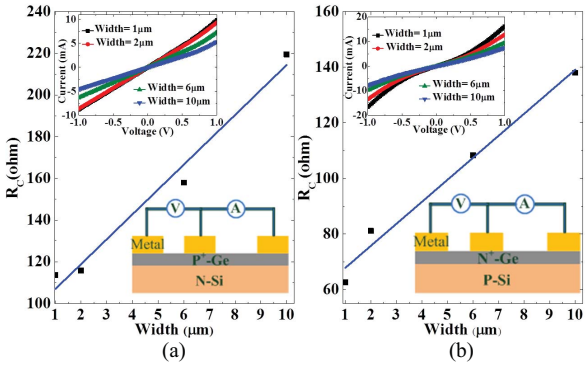

Fig. 7. (a) I–V plots and TLM structure (inset) of the metal/p^+-Ge contact, and contact resistance is plotted versus width (contact spacing). (b) I–V plots and TLM structure (inset) of the metal/n^+-Ge contact and contact resistance is plotted versus width (contact spacing).

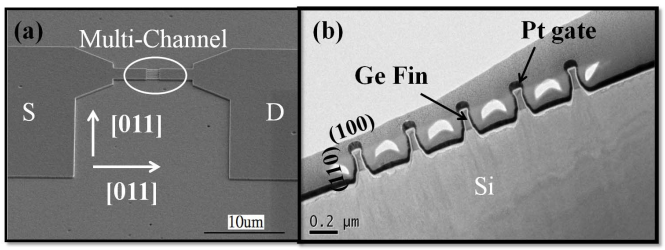

Fig. 8. (a) Shows the tilted SEM image of Ge multifin with S/D patterns on Si substrate with five fins and fin width was ~40 nm. (b) Shows the cross-sectional TEM image of Ge multifin with 5-nm Al_2O_3 high-κ dielectrics Ti/Pt metal gate stack and SOG as device isolation.

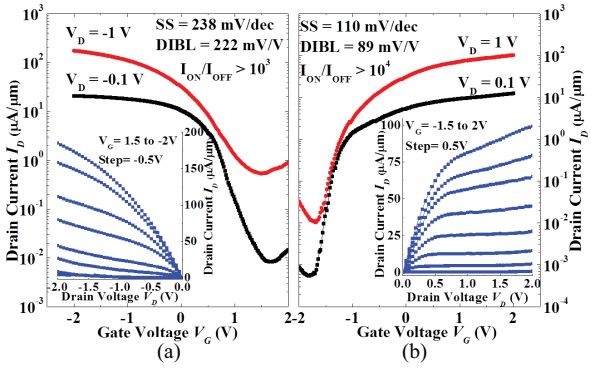

Fig. 9. (a) I_{DS}–V_G transfer characteristic and I_{DS}–V_{DS} output characteristic (inset) of Ge multifin p-FinFET with a $L_{Channel}$ of 150 nm and W_{Fin} of 40 nm. (b) I_{DS}–V_G transfer characteristic and I_{DS}–V_{DS} output characteristic (inset) of Ge multifin n-FinFET with a $L_{Channel}$ of 110 nm and W_{Fin} of 40 nm.

p^+-Ge/n-Si heterojunction is shown at low temperatures. This value is close to half of the band gap of Ge, implying that generation-recombination current in Ge dominates for the heterojunction due to the fact that the diffusion of phosphorus dopants is further enhanced by the implant damage [33]. A smaller E_a (~0.62 eV) of n^+-Ge/p-Si heterojunction indicates that the implantation-induced-defect-assisted tunneling is a possible conduction mechanism in the high-temperature region. Fig. 6(a) and (b) shows the activation energies of the p^+/n Ge and n^+/p Ge homojunctions, respectively. The activation energy was of about 0.66 eV, indicating that that the characteristic of the Ge homojunction diode is dominated by the diffusion current. This is the same with the situation found in the p^+/n Si homojunction with an activation energy of about 1.1 eV ($\sim E_g$) [34]. From Fig. 6(b), an activation of about 0.36 eV of n^+/p Ge homojunction was close to half of the band gap of Ge, implying that the generation-recombination current is a dominant component. Our results are similar to those reported in the previous work [35].

A specific contact resistance R_C is important issue for high-performance devices. The specific contact resistances of our metal/p^+ and metal/n^+ junctions were evaluated using the TLM structures [36], which are known to depend on both the metal pad area and width (contact spacing). The TLM structure and *I–V* electrical characteristics are shown in the inset of Fig. 7. In Fig. 7(a), the contact resistance of the metal/p^+-Ge is plotted versus contact width, in which the slope of the curve gives the sheet resistance (ρ_{sh}) and the intercept of x axis gives the transfer length (L_T). The specific contact resistance was c.a. 2.8×10^{-5} Ω-cm^2 and the sheet resistance was c.a. 180Ω/sq. These values are acceptable, and further improving of the specific contact resistance can be through a germanide layer between the contact metal and p^+-Ge. The specific contact resistance the metal/n^+-Ge was c.a. 1.7×10^{-5} Ω-cm^2 and the sheet resistance was 118 Ω /sq, as shown in Fig. 7(b). Furthermore, the specific contact resistance is lower than the values reported in the former literature [37], [38].

IV. Multifin FinFET CMOS

Fig. 8(a) shows the tilted plane-view scanning electron microscope (SEM) image of Ge multifin with S/D electrodes on the Si substrate. There were five Ge fins with fin width ~40 nm. Fig. 8(b) shows the cross-sectional TEM image of Ge multifins with 5-nm Al_2O_3 high-κ dielectrics and Ti/Pt metal gate stack. Fig. 9(a) shows the I_{DS}-V_G transfer characteristic of Ge multifin p-FinFET with $L_{Channel}$ of 150 nm and W_{Fin} of 40 nm in the linear region at $V_{DS} = 0.1$ V and saturation region at $V_{DS} = 1$ V. The total effective channel width ($W_{Eff} = 2 \times H_{Fin} + W_{Fin}$) of p-FinFET was ~285 nm and drain current (I_{DS}) was normalized by $5 \times W_{Eff}$. The subthreshold swing (S.S.) was 238 mV/dec and the drain-induced barrier lowering (DIBL) was 222 mV/V. The I_{ON}/I_{OFF} ratio was $\sim 2 \times 10^3$. These results suggest that the equivalent oxide

thickness (EOT) of 4.9 nm determined by *C–V* curve is too thick and the S/D junction seems too deep. We believe further EOT reduction, interface traps (D_{it}) improvement and shallower junction formation can effectively improve the subthreshold characteristics and I_{ON}/I_{OFF} ratio. Recently, a study used epitaxial Ge on the SOI substrate for p-FinFET [21] with ratio was $\sim 2 \times 10^4$ and S.S. was 350 mV/dec. Our device ($L_{Channel} = 150$ nm) not only was much smaller that ($L_g = 200$ nm) in [21] but also depicted much steeper subthreshold slope. Our device exhibited a driving current of 174 μA/μm at $V_G = -2$ V, which was higher than seen in the earlier literature ($\sim$30 μA/μm) [21]. Certainly, the multifin structure is more appropriate for future applications than the single fin one. More importantly, our device structure is a Ge body-tied FinFET, which is much preferred from the viewpoint of cost effectiveness. Fig. 9(b) shows the I_{DS}-V_G transfer characteristic of Ge multifin n-FinFET with $L_{Channel}$ of 110 nm and W_{Fin} of 40 nm. The W_{Eff} of n-FinFET was $\sim$365 nm. The S.S. value was 110 mV/dec and the DIBL value was 89 mV/V. The I_{ON}/I_{OFF} ratio was $\sim 2 \times 10^4$. The good sub-threshold characteristics and a high driving current of 102 μA/μm at $V_G = 2$ V were obtained. We think that the low ON current level is due to the low solubility and the fast diffusivity of n-type dopants [23]. As seen with the p-FinFET, a shallower junction formation of n-FinFET can mitigate the SCEs. The $I_{DS}-V_{DS}$ output characteristic of Ge multifin p-FinFET with $L_{Channel}$ of 150 nm and n-FinFET with $L_{Channel}$ of 110 nm was illustrated (see inset of Fig. 9). The saturation current of p-FinFET and n-FinFET was 81 μA/μm and 56 μA/μm, respectively, at V_{DS} and $V_{GS} = \pm 1$ V. Finally, we fabricated the short-channel Ge multifin n and p FinFETs directly on the Si substrate with relatively high driving current density with a fully Si CMOS compatible scheme.

V. Conclusion

We have demonstrated the p^+-Ge/n-Si and n^+-Ge/p-Si heterojunction diodes achieved by the mesa structure directly on the Si substrate and investigated the origins of leakage current density on the diode's performance through activation energy extraction and *I–V* measurements. Afterwards, nonplanar body-tied Ge multifin FinFET CMOS devices with Al_2O_3 high-κ dielectrics Ti/Pt metal gate stack were fabricated. Both p^+-Ge/n-Si and n^+-Ge/p-Si heterojunction diodes exhibited very high I_{ON}/I_{OFF} ratios, which were $>10^7$ and $>10^6$, respectively. Significantly low OFF current density was observed <10 μA/cm^2 for p^+-Ge/n-Si and $\sim$20 μA/cm^2 for n^+-Ge/p-Si at $V_R = \pm 1$ V with various implantation energies. The short-channel length 150-nm Ge multifin p-FinFET device had a high driving current of 174 μA/μm at $V_G = -2$ V with S.S. = 238 mV/dec and DIBL = 222 mV/V. We think the subthreshold performances can be further improved by reducing EOT, interface traps (D_{it}) improvement, and using a shallower junction formation. The short-channel length 110-nm Ge multifin n-FinFET device had a high driving current of 102 μA/μm at $V_G = 2$ V with good S.S. = 110 mV/dec and DIBL = 89 mV/V. Finally, we think that our results for heterojunction diodes are promising for future applications of high-performance Ge FinFET CMOS logic circuits and more importantly enable devices to be made using large diameter Si wafers.

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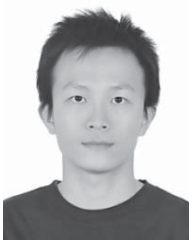

Che-Wei Chen received the M.S. degree in electronic engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2010, where he is currently pursuing the Ph.D. degree in electronic engineering with National Chiao Tung University, Hsinchu.

Cheng-Ting Chung is currently pursuing the Ph.D. degree with the Department of Electronics Engineering and the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan.

His current research interests include Ge MOSFETs, high-k/Ge gate stack, and tri-gate FETs.

Ju-Yuan Tzeng is currently pursuing the M.S. degree in electronic engineering with National Chiao Tung University, Hsinchu, Taiwan.

His current research interests include Germanide contact.

Pin-Hui Li is currently pursuing the M.S. degree with the Department of Communications Engineering, National Chiao Tung University.

His current research interests include device physics of Ge MOSFETs.

Pang-Sheng Chang is currently pursuing the M.S. degree in electronic engineering from National Chiao Tung University, Hsinchu, Taiwan.

His current research interests include the study of post Si devices.

Chao-Hsin Chien received the B.S., M.S., and Ph.D. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1990, 1992, and 1997, respectively.

He is currently a Full Professor.

Guang-Li Luo received the Ph.D. degree in solid state physics from the Institute of Physics, Chinese Academy of Sciences, Beijing, China, in 1997.

He is currently a Full Researcher. His current research interests include SiGe epitaxy and related devices.