Investigation and Comparison of Work Function Variation for FinFET and UTB SOI Devices Using a Voronoi Approach

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***Abstract*— Using a novel Voronoi method that can provide a more realistic representation of metal-gate granularity, we investigate and compare the impact of work-function variation (WFV) on FinFET and ultrathin body (UTB) silicon-on-insulator (SOI) devices. Our study indicates that, for a given electrostatic integrity and total effective gate area, the FinFET device exhibits better immunity to WFV than its UTB SOI counterpart. We further show that, unlike other sources of random variation, the WFV cannot be suppressed by equivalent oxide thickness scaling.**

***Index Terms*— FinFET, ultrathin body silicon-on-insulator MOSFET, variability, Voronoi, work-function variation (WFV).**

I. Introduction

WITH the scaling down of device dimensions, atomic-level fluctuations such as random dopant fluctuation (RDF) [1], [2] and line edge roughness (LER) [3]–[6] have become critical problems for nano-CMOS [7], [8]. More importantly, random variation may hinder the scaling of the supply voltage and therefore aggravate the power dissipation problem [7]. Although the smaller equivalent oxide thickness (EOT) provided by high-k metal gate can mitigate the threshold voltage ($V_{\rm th}$) variability [8], [9] from most sources of random variation (e.g., RDF, LER), the work-function variation (WFV) associated with the metal gate remains [10]–[15]. Whether WFV will impact the variability of FinFET and ultrathin body (UTB) silicon-on-insulator (SOI) devices differently has rarely been studied and merits investigation.

In this paper, using a novel Voronoi approach to accurately and efficiently account for the grain pattern of the metal gate, we compare the immunity of FinFET and UTB SOI devices (with the same total effective gate area) to WFV. This paper is organized as follows. Section II describes the methodology used to simulate WFV. The characteristics of WFV and its impact on threshold voltage variation are demonstrated in Section III. In Section IV, the immunity of FinFET and UTB SOI MOSFET to WFV is compared and explained. Conclusions are drawn in Section V.

Manuscript received September 7, 2012; revised January 8, 2013; accepted February 7, 2013. Date of current version March 20, 2013. This work was supported in part by the National Science Council of Taiwan under Contract NSC 101-2221-E-009-073 and the Ministry of Education in Taiwan under the ATU Program. The review of this paper was arranged by Editor H. S. Momose.

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Digital Object Identifier 10.1109/TED.2013.2248087

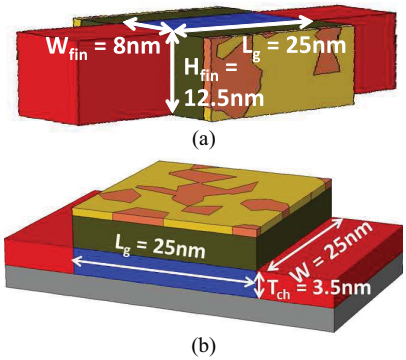

Fig. 1. Schematics of (a) FinFET and (b) UTB devices with identical effective width. L_g is the channel length, $H_{\rm fin}$ is the fin height, $W_{\rm fin}$ is the fin width, W is the channel width, and T_{ch} is the channel thickness.

TABLE I
DEVICE PARAMETERS OF UTB SOI AND FinFET

UTB		FinFET	
L_g [nm]	25	L_g [nm]	25
W [nm]	25	$H_{\rm fin}$ [nm]	12.5
T_{ch} [nm]	3.5	$W_{\rm fin}$ [nm]	8
EOT [nm]	0.65	EOT [nm]	0.65
N_{ch} [cm^{-3}]	10^{17}	N_{ch} [cm^{-3}]	10^{17}

II. Simulation Methodology

Although several methods have been proposed to simulate WFV in the past [10]–[14], in this paper, we use a novel Voronoi method [16]–[22] that can provide a more realistic representation of metal-gate granularity to investigate the impact of WFV on FinFET and UTB SOI devices. Fig. 1 shows the schematic of FinFET and UTB SOI devices designed with the same total gate area ($W_{\rm total} = 25$ nm) and comparable electrostatic integrity (SS $\approx$ 70 mV/dec) for fair comparison. Other pertinent device parameters are listed in Table I. In this paper, we employ TiN as the gate material for both FinFET and UTB SOI MOSFET. For TiN metal gate, two possible grain orientations (<200> and <111> [15], [27], [28]) with distinct work function and probability should be considered. Table II summarizes the characteristics for the two orientations of the TiN metal gate.

To generate various metal-gate grain patterns for macroscopically identical devices, four factors regarding the grain

TABLE II
GRAIN ORIENTATIONS WITH THE CORRESPONDING PROBABILITY AND WORK FUNCTION FOR A TiN METAL GATE [15]

TiN Metal Gate		
Orientation	<200>	<111>
WF [eV]	$\psi_1 = 4.6$	$\psi_2 = 4.4$
Probability [%]	60	40

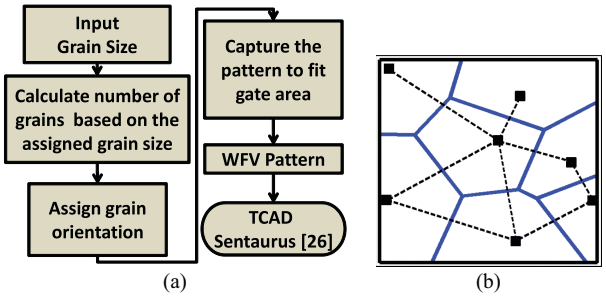

Fig. 2. (a) Flowchart for determining the WFV pattern [N_{grain} = (Area)/(π × (grain size/2)^2)]. (b) Formation of the Voronoi pattern. The solid lines are the perpendicular bisectors of the dashed lines that connect each grain seed.

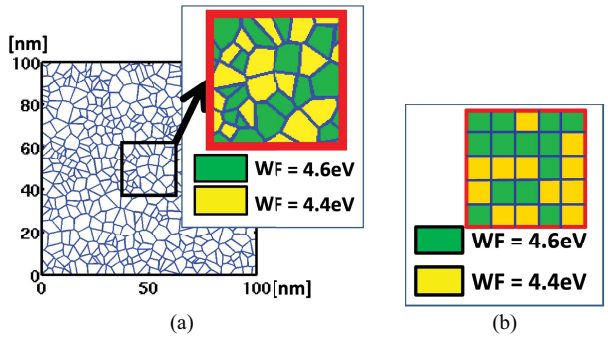

Fig. 3. Comparison of two different grain patterns (average grain size = 5 nm) for the simulation of WFV. (a) Voronoi. (b) Square.

should be considered: 1) seed position; 2) shape; 3) size; and 4) orientation. Fig. 2(a) shows the simulation flow of our proposed Voronoi approach to simulate WFV. First, the assigned average grain size is used to estimate the number of grains (seeds) for constructing the random Voronoi grain pattern. The determined seeds are randomly placed in the metal gate region [black solid points in Fig. 2(b)]. The distributions of seed position are different for each device. With the seed location shown in Fig. 2(b), the Voronoi pattern is constructed by connecting the solid lines which are the perpendicular bisectors of each dashed line. Fig. 3(a) shows the generated Voronoi pattern for the simulation of WFV in the metal gate region. Notice that, in addition to the shape of metal grain, the effective work function for each grain varies with orientation. For comparison, Fig. 3(b) shows a conventional method [13] which describes the shape of grain by the square pattern.

It should be noted that the underlying assumption for the Voronoi method is that the grain growth rate of each grain is the same. In other words, the voids and grain boundaries that may be present in a real polycrystalline structure are not considered in Voronoi method used by us. More detailed approaches beyond the classical Voronoi tessellation to consider the effect of voids and grain boundaries can be found in [21] and [22].

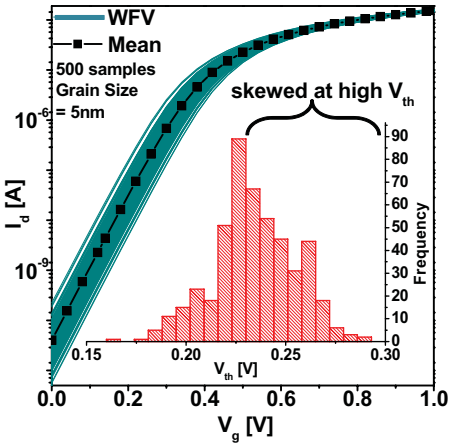

Fig. 4. Dispersion of I_d–V_g curves (at V_{ds} = 0.05 V) and skewed V_{th} distribution for FinFET with WFV.

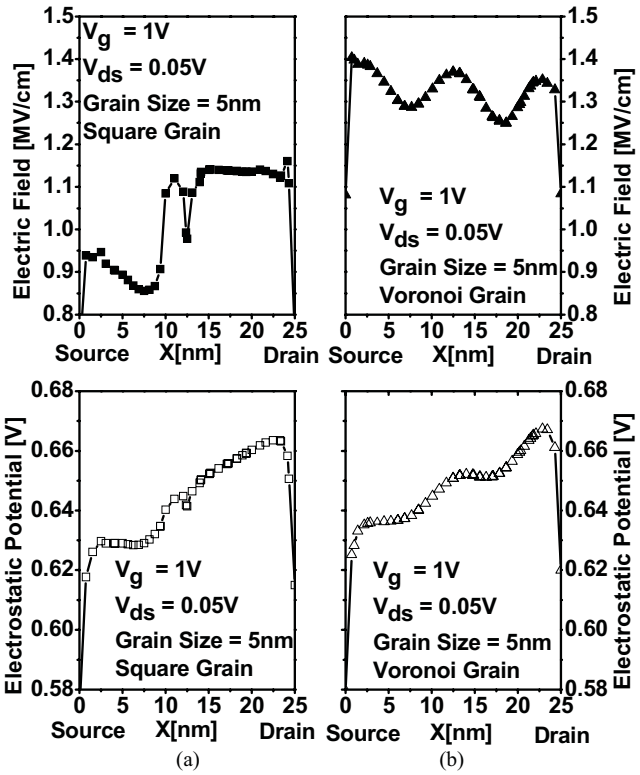

Fig. 5. Electric field and electrostatic potential at channel surface with two kinds of WFV simulation methods. (a) Square. (b) Voronoi.

III. CHARACTERISTICS OF WFV

Based on our Voronoi approach, Fig. 4 shows the I_d–V_g dispersion for FinFET devices with WFV. As can be seen, the resulting V_{th} dispersion is asymmetric and skews at high V_{th}. The deviation from a Gaussian distribution is due to the difference in the orientation probability (see Table II) of the TiN metal gate. The <200> orientation with larger work

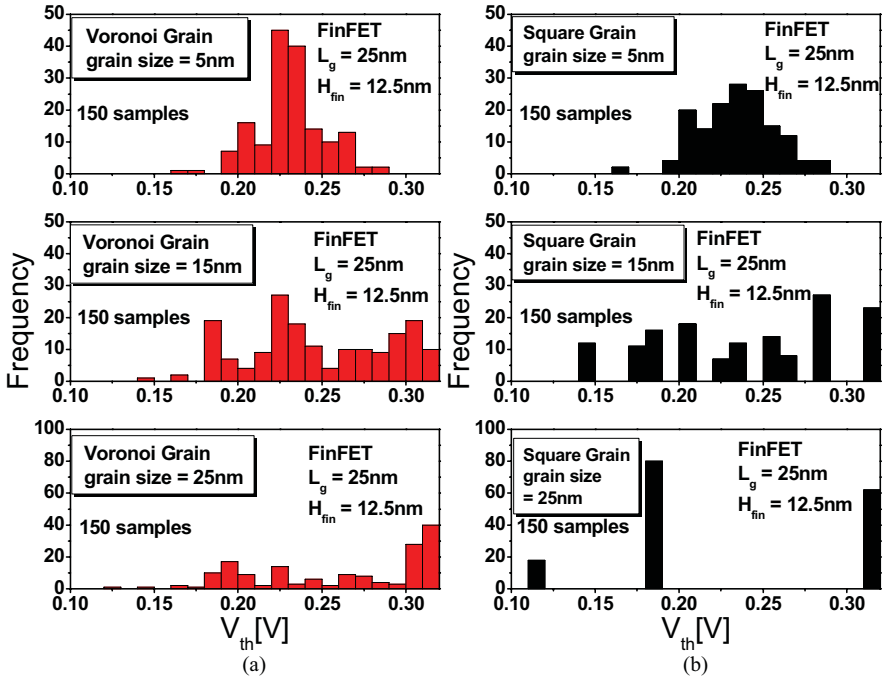

Fig. 6. V_{th} dispersion from (a) Voronoi grain method and (b) square grain method with various grain sizes. For the cases with larger grain sizes (15, 25 nm), unrealistic discrete bars are observed in (b).

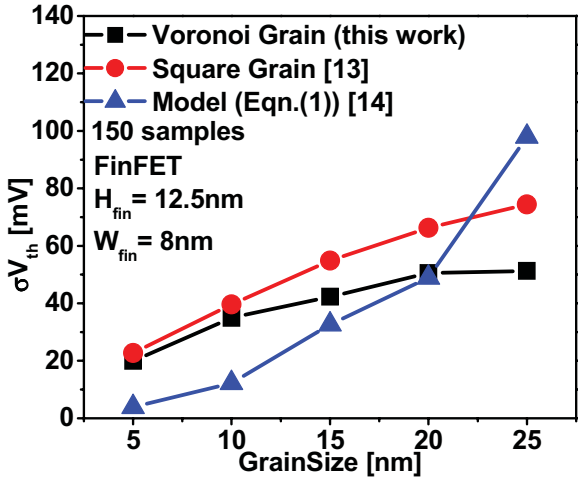

Fig. 7. Comparison of WFV-induced V_{th} variations in FinFET devices for the three methods.

function possesses higher probability, thus distorting the V_{th} dispersion to a higher value.

It should be noted that, different from the method proposed in this paper, the square grain method [13], which uses the square pattern for each grain [Fig. 3(b)], exhibits abrupt electric field change near the grain boundary. Fig. 5(a) shows the significant change in electric field at the channel surface using the square grain method, whereas the irregular grain shapes by using the Voronoi method can faithfully account for the interaction between neighboring grains and thus smooth the electric field near the grain boundary [Fig. 5(b)].

In Fig. 6, we compare the V_{th} dispersion of the Voronoi and square methods for FinFET devices with various grain sizes. It can be seen that, as the grain size increases, the V_{th} variation becomes broader and the distribution extends to the V_{th} extreme values bounded by the work function difference between the two orientations (0.2 eV). Besides, obvious discrete V_{th} dispersion is observed for the square method whereas the Voronoi method is still able to reflect the continuous V_{th} dispersion at grain size = 25 nm.

In addition to these two simulation approaches, a model had also been proposed to evaluate the impact of WFV in the past [14]. This model considers only the number fluctuations of the two different grains for a given grain number (N_{grain}) and can be expressed as

$$\sigma V_{\text{th}} = \sqrt{\frac{1}{N_{\text{grain}}}\left(\sum_{i=0}^{N_{\text{grain}}}(P_i\Phi_i^2) - \sum_{i=0}^{N_{\text{grain}}}(P_i\Phi_i)^2\right)} \quad (1)$$

$$\text{where } P_i = \frac{N_{\text{grain}}!}{i!(N_{\text{grain}}-i)!}(60\%)^i(40\%)^{N_{\text{grain}}-i} \quad (2)$$

$$\text{and } \Phi_i = \frac{i}{N_{\text{grain}}}(4.6\text{ eV}) + \frac{N_{\text{grain}}-i}{N_{\text{grain}}}(4.4\text{ eV}). \quad (3)$$

Fig. 7 shows a comparison of the WFV-induced V_{th} variations among the three methods. It can be seen that the model in [14] (1) shows higher sensitivity to the grain number (i.e., grain size), because it merely considers the grain number fluctuation, while the other two simulation methods show a saturated trend in V_{th} variation [10] as the grain size approaches the size of the device gate area. In addition, the discrepancy between the Voronoi and square methods increases with increasing grain size, and the V_{th} variation predicted by the square method overestimates the influence of WFV-induced variability.

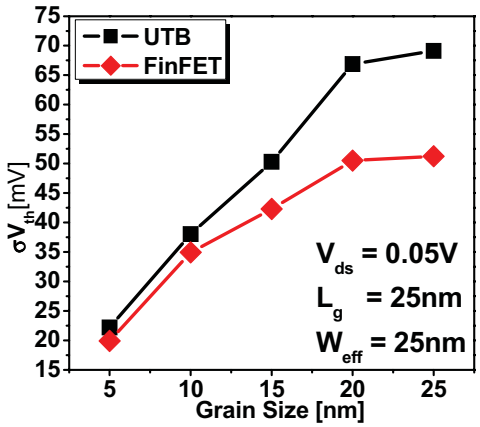

Fig. 8. Comparison of V_{th} variations for FinFET and UTB devices with various grain sizes.

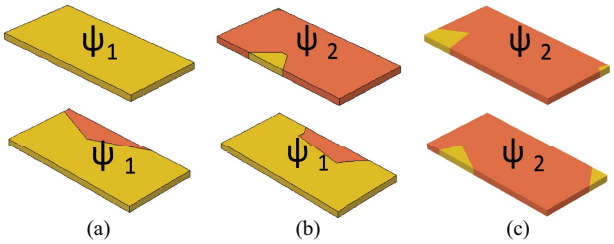

Fig. 9. Extreme case of metal-gate patterns for FinFET. (a) Both front-gate and back-gate WF = ψ_1. (b) Front-gate WF = ψ_1 and back-gate side WF = ψ_2. (c) Both front-gate and back-gate WF = ψ_2. Grain size = 25 nm for each case.

IV. Comparison Between FinFET and UTB SOI

Using our proposed Voronoi method, we investigate and compare the impact of WFV on FinFET and UTB SOI devices designed with comparable electrostatic integrity (SS $\approx$ 70 mV/dec) and the same total effective width (W_{total} = 25 nm). Fig. 8 compares the WFV-induced V_{th} variation between the two device structures with different grain sizes. As can be seen, the UTB SOI MOSFET is more vulnerable to WFV (larger V_{th} variation) and the difference between UTB and FinFET devices increases with increasing grain size. This is because, in the extreme case with grain size close to the device gate area, the possible grain number inside the gate area is close to 1 and the FinFET device with double-gate structure possesses three possible work-function combinations, as illustrated in Fig. 9. For UTB SOI MOSFET with single-gate structure, however, only two work-function combinations are allowed (Fig. 10). In other words, the FinFET device with one more possible work-function combination possesses more averaging effect in WFV, and thus better immunity to WFV than the UTB counterpart.

The importance of WFV can be demonstrated in Fig. 11, where the impact of Fin Line-Edge-Roughness (Fin LER) [23]–[25] on V_{th} variation is compared with that of WFV under various EOT. To assess the LER in FinFET devices, the rough line-edge patterns are generated using Fourier synthesis with correlation length = 30 nm and rms amplitude = 1.5 nm [23] for FinFET MOSFETs. It can be seen that, while the Fin-LER-induced V_{th} variation can be mitigated by smaller

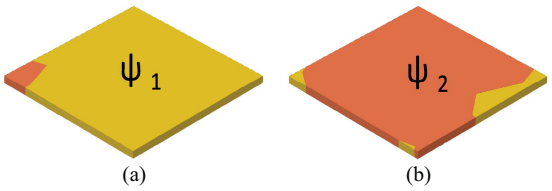

Fig. 10. Extreme case of metal gate patterns for UTB. (a) WF = ψ_1. (b) WF = ψ_2. Grain size is 25 nm for each case.

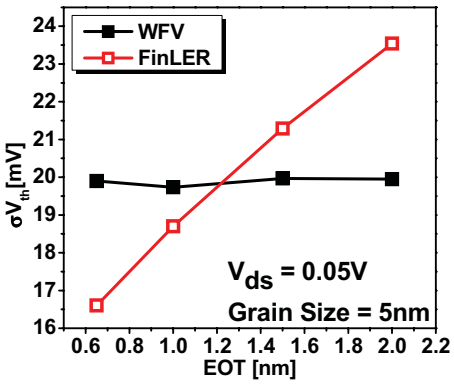

Fig. 11. Comparison of WFV and Fin-LER-induced V_{th} variations for the FinFET device with L_g = 25 nm and W_{eff} = 25 nm. Unlike Fin LER, WFV cannot be suppressed by EOT scaling.

EOT and improved EI, the impact of WFV cannot be suppressed by EOT scaling.

V. Conclusion

We investigated and compared the impact of WFV on FinFET and UTB SOI devices using a novel Voronoi method that can provide a more realistic representation of metal-gate granularity. We found that for a given electrostatic integrity and total effective gate area, the FinFET device exhibits better immunity to WFV than its UTB SOI counterpart. We further showed that, unlike other sources of random variation, the WFV cannot be suppressed with EOT scaling. Our study may provide insights for device design in nanoscale CMOS.

Acknowledgment

The authors would like to thank the National Center for High-Performance Computing in Taiwan for the computational software and facilities.

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