Enhanced Light Output Power and Growth Mechanism of GaN-Based Light-Emitting Diodes Grown on Cone-Shaped SiO_2 Patterned Template

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***Abstract*—In this study, we successfully transferred the patterns of a cone-shaped patterned sapphire substrate (CPSS) into SiO_2 layer to fabricate a cone-shaped SiO_2 patterned template by using nanoimprint lithography (NIL). The GaN-based light-emitting diodes (LEDs) were grown on this template by metal-organic chemical vapor deposition (MOCVD). The transmission electron microscopy (TEM) images suggest that the stacking faults formed near the cone-shaped SiO_2 patterns during the epitaxial lateral overgrowth (ELOG) can effectively suppress the threading dislocations, which results in an enhancement of internal quantum efficiency. The Monte Carlo ray-tracing simulation reveals that the light extraction efficiency of the LED grown on cone-shaped SiO_2 patterned template can be enhanced as compared with the LED grown on CPSS. As a result, the light output power of the LED grown on cone-shaped SiO_2 patterned template outperformed the LED grown on CPSS.**

***Index Terms*—Epitaxial lateral overgrowth (ELOG), internal quantum efficiency (IQE), light extraction efficiency (LEE), light-emitting diodes (LEDs), nano-imprint lithography (NIL).**

I. Introduction

III-NITRIDE materials have attracted great attention and have various applications, such as solid-state lighting, laser diodes, and display backlight. Although high brightness nitride-based light-emitting diodes (LEDs) grown by metal-organic chemical vapor deposition (MOCVD) have been mass-produced, for developing solid-state lighting, further improving the light output power and external quantum efficiency (EQE) are needed. Typically, the EQE of an LED can be expressed as the product of the internal quantum efficiency (IQE) and the light extraction efficiency (LEE) [1]. Recent advance in the development of native GaN substrates with very low dislocation density and high crystalline quality have attracted much attention on developing nitride-based devices on GaN substrates [2], [3]. However, since the GaN substrates is high-priced and difficult to secure, up to now, the foreign substrates, such as sapphire, GaAs, SiC, and silicon are still the most commonly used substrates for growing GaN epilayers. Such heteroepitaxial layers typically show high threading dislocation densities (approximately 10^8–10^{10} cm^2) due to large lattice and thermal mismatches between GaN epilayers and foreign substrates [4]. The threading dislocations (TDs) act as a nonradiative center inside GaN films and hence limit the IQE of LED devices. To solve such problems, various growth techniques have been proposed, such as epitaxial lateral overgrowth (ELOG) [5], pendeoepitaxy [6], and *in situ* SiN_x nanomasks [7]. In addition, the quantum-confined Stark effect (QCSE) caused by the internal piezoelectric field also plays an important role in LEDs performance. These effects may decrease the wave function overlap between holes and electrons and limit the output power of LEDs [8]. In order to suppress the charge separation in active regions, several approaches have been proposed, such as nonpolar and semipolar InGaN quantum wells (QWs) [9]–[11] and polar QWs with improved electron-hole wave function overlap designs [12]–[14]. On the other hand, the LEE of an LED is limited mainly due to the total internal reflection occurred as the ray of light striking the medium boundary with the incident angle greater than the critical angle of GaN $(n = 2.5)$ and air $(n = 1)$. Also, several methods have been developed to improve the LEE of an LED, including surface roughness [15], photonic crystal [16], [17], and patterned sapphire substrate (PSS) [17], [18]. Among all of the above technologies, PSS has become more and more popular in the current LED industry due to the threading dislocation density in the GaN epilayer can be effectively reduced by ELOG and the micron-scaled patterns act as scattering centers for the light trapped inside the LED structures [19]–[21]. Moreover, the pattern density of micron-scaled PSS had been shown to have strong effect on the LEE in GaN-based LEDs [22]. In addition, it is noteworthy that some recent works indicate using nano-scaled PSS can also improve the IQE and the EQE of an InGaN-based LED [23]–[28]. Even though some studies indicate that the LEDs grown on nano-scaled PSS outperform the LEDs grown on micron-scaled PSS [29], there are still no complete physical interpretation and understanding for various shaped and scaled PSS fabricated by various processes.

On the other hand, some groups focused on investigating the shape of micron-scaled PSS. Lee *et al.* considered that

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the GaN epilayer grown on cone-shaped patterned sapphire substrate (CPSS) has outstanding growth mode and crystalline quality [30]. Wang *et al.* analyzed the GaN epilayer grown on two kinds of PSS, trapezoid-shaped PSS (TPSS) and CPSS and found that the GaN epilayer grown on CPSS has better epitaxial quality and less residual strain than GaN epilayer grown on TPSS [31]. In this study, a general CPSS was used to transfer its cone-shaped patterns into SiO_2 layer to fabricate a cone-shaped SiO_2 patterned template by using nanoimprint lithography (NIL). The LEDs grown on this novel cone-shaped SiO_2 patterned template combine the benefits of enhancement of LEE by SiO_2 cone-shaped patterns and high quality GaN epilayer with the ELOG mechanism. The detailed experimental procedure and analyses will be discussed as follows.

II. Experiments

Fig. 1(a) and (b) shows the schematic diagrams of process flow for fabricating reverse cone-shaped mold and cone-shaped SiO_2 patterned template, respectively. As shown in Fig. 1(a), the reverse cone-shaped mold was constructed by imprinting a cone-shaped patterned sapphire substrate (CPSS) on the intermediate polymer stamp (IPS). The bottom diameter, the center-to-center spacing, and the height of the CPSS are 2.5 μm, 3 μm, and 1.5 μm, respectively. After imprinting the CPSS on IPS, the stack of the IPS/CPSS was heated to solidify the IPS. Finally, the stack of the IPS/CPSS was cooled down to room temperature to separate the IPS reverse cone-shaped mold from CPSS. This reverse cone-shaped mold was used to fabricate the cone-shaped SiO_2 patterns on planar sapphire substrate. The schematic diagrams of process flow are shown in Fig. 1(b). First, the SiO_2 was deposited on the planar sapphire substrate by plasma-enhanced chemical vapor deposition (PECVD). Then an 800 nm thick imprint resist (IR) layer was coated on the SiO_2 layer by spin-coating. Next, the 800 nm thick IR layer was imprinted by the reverse cone-shaped mold and then exposed by UV light and heated up. After that, the exposed IR was etched by a reactive ion etching (RIE) process with O_2 plasma to form cone-shaped patterns. Also, the RIE process with CHF_3 plasma was used to etch the SiO_2 and transfer the cone-shaped patterned IR into SiO_2 layer. Finally, the cone-shaped SiO_2 patterns were formed on the planar sapphire substrate.

The epitaxial InGaN/GaN LED structure was grown on the cone-shaped SiO_2 patterned template by metal-organic chemical vapor deposition (MOCVD). After thermal cleaning of the substrate in hydrogen ambient for 5 min at 1200 °C, a 30 nm thick GaN nucleation layer was grown at 500 °C. On the top of the low-temperature GaN nucleation layer, a 2 μm undoped GaN was grown at 1100 °C, followed by a 2 μm Si-doped n-type GaN layer grown at 1050 °C ($n =\sim 3 \times 10^{18}$ cm^{-3}). After the growth of n-type GaN layer, six-period $In_{0.18}Ga_{0.82}N$/GaN multiple quantum wells (MQWs) were grown, followed by a p-type $Al_{0.12}Ga_{0.88}N$ electron blocking layer (EBL) and a 120 nm thick p-type GaN contact layer. The MQW active region consists of 3-nm-thick InGaN wells and 10-nm-thick GaN barriers. The Mg doping concentrations in the p-type AlGaN EBL and p-type GaN contact layer are about 2×10^{19} and 3×10^{19} cm^{-3}, respectively, which are from the measurement of the secondary ion mass spectrometry (SIMS). The In and Al compositions in InGaN/GaN MQWs and AlGaN EBL were estimated by performing high-resolution X-ray diffraction (HRXRD) measurement. Subsequently, the LED mesa with an area of 350×350 μm^2 was defined by using standard photolithography and dry etching. In addition, a transparent conduction indium tin oxide (ITO) layer was employed to be the p-type Ohmic contact layer and Cr/Pt/Au metal was deposited as p- and n-type electrodes, respectively. The identical epitaxial LED structures were also grown on the CPSS and the planar c-plane sapphire substrate for comparison. For convenience, the LEDs grown on the planar sapphire substrate, CPSS, and cone-shaped SiO_2 patterned template would be denoted as C-LED, CPSS-LED, and SiO_2-LED, respectively.

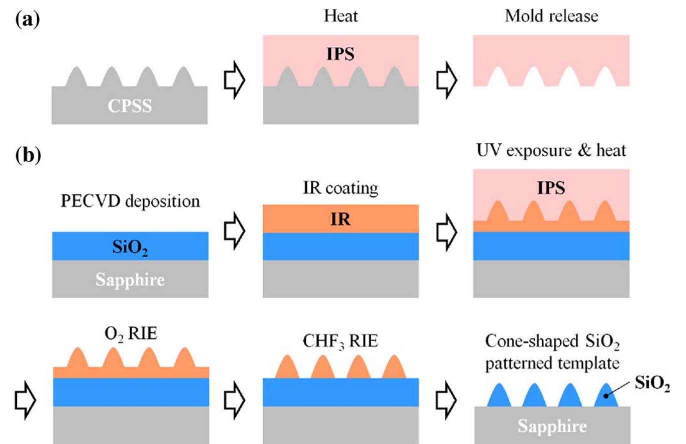

Fig. 1. Schematic diagram of process flow for (a) reverse cone-shaped mold and (b) cone-shaped SiO_2 patterned template.

The transmission electron microscopy (TEM) was employed to resolve the distribution and behaviors of threading dislocations and stacking faults in epitaxial layer. The internal quantum efficiency (IQE) was measured by a photoluminescence (PL) system with a wavelength of 400 nm Ti: sapphire laser as the excitation source. In addition, the Monte Carlo ray-tracing simulation was used to estimate the light extraction efficiency (LEE) of LEDs grown on these three types of templates. Finally, the current-voltage (I-V) and the light output power–current (L–I) of LEDs were measured by a conventional probe station and an integrated sphere setup.

III. Results and Discussion

Fig. 2 show the TEM images of GaN epilayers grown on planar sapphire substrate, cone-shaped patterned sapphire substrate (CPSS) and cone-shaped SiO_2 patterned template. As shown in Fig. 2(a), there were many threading dislocations (TDs) propagating along the vertical direction for the GaN epilayer grown on the planar sapphire substrate. This phenomenon is caused by the large lattice and thermal mismatches between GaN epilayer and sapphire substrate [4]. On the other hand, the growth mechanism of GaN epilayer grown on CPSS is much different than it grown on planar sapphire substrate. As shown in Fig. 2(b), the GaN epilayer can be divided into two parts, wing and window regions. The TDs were mainly distributed in the window region, which are similar to the TDs in the GaN epilayer grown on planar sapphire. However, the crystalline

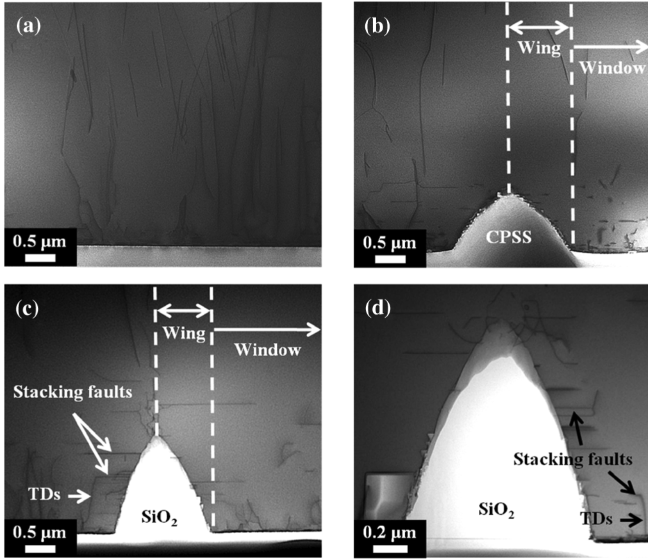

Fig. 2. Cross-sectional TEM images of GaN epilayer grown on: (a) planar sapphire substrate; (b) CPSS; and (c), (d) cone-shaped SiO_2 patterned template.

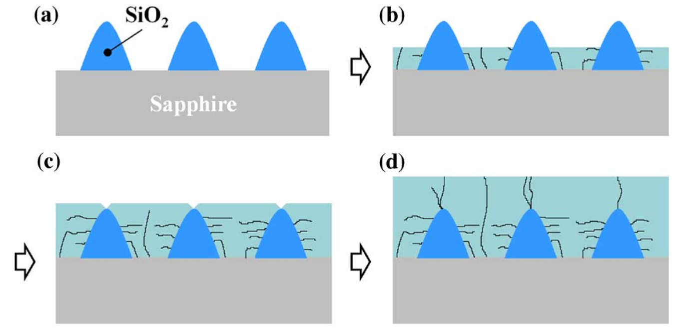

Fig. 3. Schematics of the growth evolution and the propagation of the TDs for GaN epilayer grown on the cone-shaped SiO_2 patterned template.

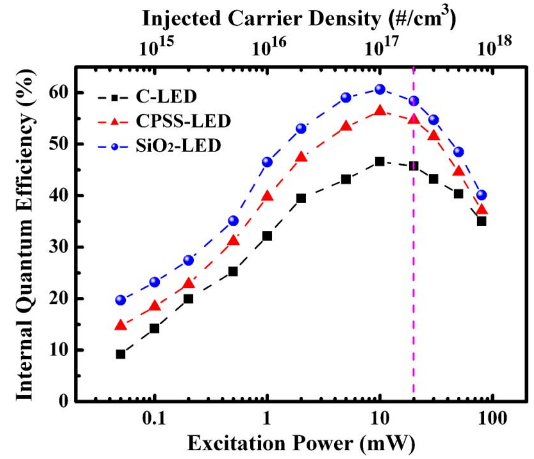

Fig. 4. The IQE as a function of excitation power for C-LED, CPSS-LED, and SiO_2-LED.

quality of GaN epilayer in the wing region was drastically improved from that grown in the window region due to the epitaxial lateral overgrowth (ELOG) occurred and the TDs were bended along the direction parallel to the surface of the cone-shaped patterned sapphire. This result is consistent with other research of GaN epilayer grown on CPSS [31]. In addition, Fig. 2(c) and (d) show the behaviors of TDs and stacking faults for GaN epilayer grown on the cone-shaped SiO_2 patterned template. The schematics of the growth evolution and the propagation of the TDs for GaN epilayer grown on the cone-shaped SiO_2 patterned template are also shown in Fig. 3. The GaN epilayer grown on the cone-shaped SiO_2 patterned template has a similar ELOG as it grown on CPSS except the tilted surface of the cone-shaped SiO_2 patterns cannot be grown. As a result, some of the TDs were bended along the direction parallel to the surface of the cone-shaped SiO_2 patterns. Moreover, we found that there were many stacking faults originated from the edge of the cone-shaped SiO_2 patterns and extended to its window region. These stacking faults can effectively suppress and block the TDs in the window region from propagating to the upper GaN epilayer and MQWs. The formation of stacking faults and the propagation of TDs are depicted in Fig. 3(b). However, during the lateral coalescence of GaN epilayer on the cone-shaped SiO_2 patterns, there were a few TDs formed from the peak of the cone-shaped SiO_2 patterns, shown as Fig. 3(c) and (d). Because there were no stacking faults above the peak of the cone-shaped SiO_2 patterns, these TDs would not be suppressed. Even though there were a few TDs formed from the peak of the cone-shaped SiO_2 patterns and some parts of the window region without stacking faults covering above, the GaN epilayer grown on cone-shaped SiO_2 patterned template still display less TDs and better crystalline quality in these three samples.

It has been reported that the improvement of the crystalline quality can effectively enhance the internal quantum efficiency (IQE) of the InGaN/GaN multiple quantum wells (MQWs) [32]. In order to clarify the correlation between the crystalline quality and IQE for LED grown on planar sapphire substrate, CPSS and cone-shaped SiO_2 patterned template, the photoluminescence (PL) internal quantum efficiency (IQE) measurement was performed. A general approach to evaluate the IQE of LEDs is to compare the PL integrated intensity between low and room temperatures [1]. The IQE is defined as the collected photon numbers divided by the injected photon numbers and normalized to the maximum efficiency at low temperature (15 K). Fig. 4 shows the measured IQE as a function of excitation power at room temperature (300 K) for these three samples. In addition, for clearly estimating the corresponding injected carrier density, the following equation was used to transfer the injected power into injected carrier density [33]:

$$\begin{aligned}&\text{Injected Carrier Density}\\&\quad= \frac{P}{(hv) * \phi * d_{\text{active}} * f} \times \exp(-\alpha_{\text{GaN}} d_{\text{GaN}})\\&\quad\times [1 - \exp(-\alpha_{\text{InGaN}} d_{\text{active}})] * (1 - R).\end{aligned}$$

The injected carrier density is determined by the power of the pumping laser (P), the energy of the injected photon (hv), the spot size of the pumping laser (φ), the thickness of the GaN and active region $(d_{\text{GaN}}, d_{\text{active}})$, the repetition rate of the pumping laser (f), the absorption efficiency of GaN and InGaN $(\alpha_{\text{GaN}}, \alpha_{\text{InGaN}})$, and the reflectance of the pumping laser (R).

The pumping laser used in this experiment was a frequency-doubled Ti: sapphire laser at a wavelength of 400 nm and the

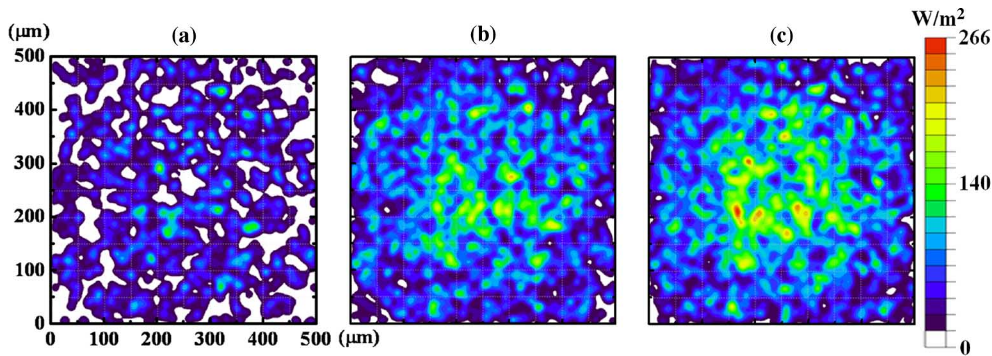

Fig. 5. Monte Carlo ray-tracing simulated illuminance maps of: (a) C-LED; (b) CPSS-LED; and (c) SiO2-LED.

laser output power was modulated from 0.05 to 80 mW by a neutral density filter. The laser pulse width was 200 fs and the repetition rate was 76 MHz. Moreover, other parameters, including $\varphi = 50\ \mu$m, $d_{GaN} = 60$ nm, $d_{\rm active} = 78$ nm, $\alpha_{\rm InGaN} = 10^5\ {\rm cm}^{-1}$ and $R = 0.17$ were used to calculate the injected carrier density. By using the above equation, the excitation power of 20 mW can be calculated to be the carrier density of $2 \times 10^{17}\ {\rm cm}^{-3}$, which is approximately the same level of our devices operated under 20 mA. At 20 mW of excitation power, the IQE for C-LED, CPSS-LED, and SiO_2-LED were 45.7%, 54.7%, and 58.4%, respectively. The highest IQE of LEDs grown on cone-shaped SiO_2 patterned template can be attributed to the least TDs in the MQWs grown on this template.

To investigate the influence of these three kinds of substrate (planar sapphire substrate, CPSS, and cone-shaped SiO_2 patterned template) on the light extraction efficiency (LEE) of LEDs, a Monte Carlo ray-tracing simulation was used. For simplifying the simulations, we did not consider the effects of the electrical pad. In these Monte Carlo simulations, the light with a power of 100 mW (10000 light rays) and a wavelength of 450 nm were assumed to be generated randomly from the active region, and isotropically emitted and monochromatic unpolarized. The trajectory and energy of each ray were determined by using Snell's law and Fresnel losses, respectively. A detector with the size of $500 \times 500\ \mu{\rm m}^2$ was located at the top and apart from the LED model for 300 μm. Fig. 5 show the simulated illuminance maps of these three cases. As shown in Fig. 5, the maximum candelas values in these three maps were 162, 228, and 266 W/m^2 for C-LED, CPSS-LED, and SiO_2-LED, respectively. In addition, the corresponding LEE, which was the ratio of the energy collected from the detector and the total energy emitted from the active region, were 8.0%, 16.1%, and 18.8% for C-LED, CPSS-LED, and SiO_2-LED, respectively. This simulated results indicates that more photons escape out into the air for CPSS-LED and SiO_2-LED than C-LEDs. Moreover, the SiO_2-LED show better light extraction efficiency than CPSS-LED. This result can be simply explained by Snell's law. Owing to the refractive index of SiO_2 and sapphire are 1.4 and 1.7, respectively, the critical angles of occurring total internal reflection for a blue ray emitted from MQWs, then passed through GaN $(n = 2.5)$, and finally reached to SiO_2 and sapphire are calculated to be 34.1° and 42.8°, respectively. As a result, it is reasonable that the cone-shaped SiO_2 patterns have better capability for reflecting the downward ray to upward than CPSS due to its smaller critical angle. This is the reason for the SiO_2-LED outperform the CPSS-LED in LEE.

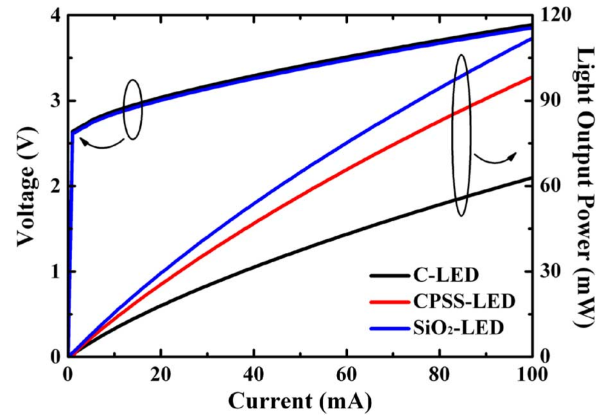

Fig. 6. Power–current–voltage (L–I–V) characteristics of C-LED, CPSS-LED, and, SiO_2-LED.

Fig. 6 shows the typical power-current-voltage (L-I-V) characteristics of C-LED, CPSS-LED, and SiO_2-LED. With an injection current of 20 mA, the forward voltages are 3.04 V, 3.02 V, and 3.00 V, and the light output powers are 18.0, 25.5, and 29.4 mW for C-LED, CPSS-LED, and SiO_2-LED, respectively. The light output power enhancement of SiO_2-LED can be attributed to both the improvements of IQE and LEE. During the growth of GaN epilayer on cone-shaped SiO_2 patterned template, the stacking faults originated from the edge of the cone-shaped SiO_2 patterns can effectively suppress the threading dislocations, which results in an enhancement of IQE. Moreover, the cone-shaped SiO_2 patterns with a relatively small refractive index $(n = 1.4)$ can improve the LEE as compared to the CPSS $(n = 1.7)$, which was verified by the Monte Carlo ray-tracing simulation. As a result, the light output power of SiO_2-LED is higher than CPSS-LED.

IV. Conclusion

In conclusion, we successfully transferred the cone-shaped sapphire patterns into SiO_2 layer to fabricate cone-shaped SiO_2 patterned substrate by using nanoimprint lithography (NIL) and the GaN-based light-emitting diodes (LEDs) were grown on this substrate by metal-organic chemical vapor deposition (MOCVD). The transmission electron microscopy images suggest that the stacking faults introduced during the epitaxial

lateral overgrowth can effectively suppress the threading dislocation density. From the IQE measurement, the SiO_2-LED has the highest IQE (58.4%) as compared with C-LED (45.7%) and CPSS-LED (54.7%). The Monte Carlo ray-tracing simulation also reveals that the light extraction efficiency of the LED grown on cone-shaped SiO_2 patterned substrate can be enhanced as compared with cone-shaped patterned sapphire substrate due to the smaller refractive index for SiO_2 than sapphire. As a result, the SiO_2-LED shows the highest light output power in these three cases due to the better performance for both internal quantum efficiency (IQE) and light extraction efficiency (LEE).

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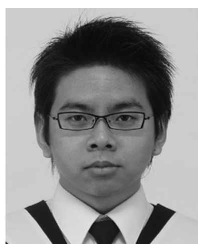

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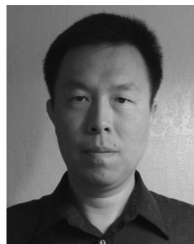

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