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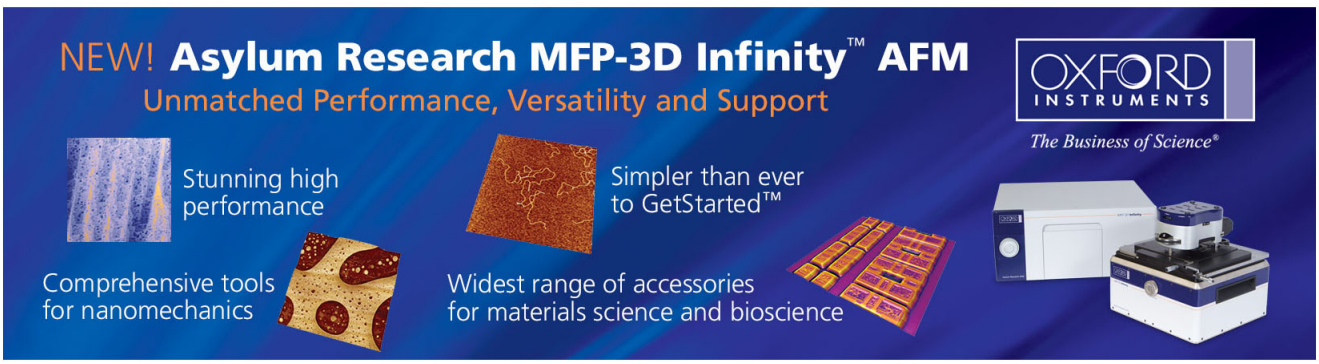

Hot carrier effect on gate-induced drain leakage current in high-k/metal gate n-channel metal-oxide-semiconductor field-effect transistors

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This paper investigates the channel hot carrier stress (CHCS) effects on gate-induced drain leakage (GIDL) current in high-k/metal-gate n-type metal-oxide-semiconductor field effect transistors. It was found that the behavior of GIDL current during CHCS is dependent upon the interfacial layer (IL) oxide thickness of high-k/metal-gate stacks. For a thinner IL, the GIDL current gradually decreases during CHCS, a result contrary to that found in a device with thicker IL. Based on the variation of GIDL current at different stress conditions, the trap-assisted band-to-band hole injection model is proposed to explain the different behavior of GIDL current for different IL thicknesses. © *2011 American Institute of Physics*. [doi:10.1063/1.3608241]

With the scaling down of metal-oxide semiconductor field electrical field transistors (MOSFETs), the aggressive shrinking of conventional SiO_2-based dielectric in recent years has approached its physical limits. To meet the International Technology Roadmap for Semiconductors, Hf-based dielectrics have been heavily investigated as a replacement for the SiO_2 gate insulator in order to reduce both tunneling gate leakage and power consumption in complementary metal-oxide-semiconductor (CMOS) circuits.[1–3] However, one of the key issues in high-k gate stacks is the high density of traps in the bulk high-k layer. These traps degrade the device performance and reliability.[3–5] It has been additionally reported that bulk traps significantly enhance the gate-induced drain leakage (GIDL) current in devices with high-k dielectric.[6] On the other hand, the hot carrier effect in high-k/metal gate n-MOSFETs remains a major device reliability concern in device scaling. As is well known, under hot carrier injection a high lateral electric field in the pinch-off region heats the electrons sufficiently to gain enough energy to overcome the Si/SiO_2 potential barrier, causing damage on the drain side which leads to the degradation of current-voltage characteristics. However, most studies have concentrated on device driving current and transconductance deterioration,[7–10] while stress-induced drain leakage current degradation in a device with high-k/metal gate stacks has not received as much attention. Therefore, the aim of this Letter is to investigate the effects of channel hot carrier stress (CHCS) on the GIDL current for n-MOSFETs with HfO_2/TiN gate stacks. It was found that the behavior of GIDL current after hot carrier stress (HCS) is dependent on interfacial layer (IL) thickness. To explain this phenomenon, the device with thin IL thickness was subjected to different stress conditions. Based on the experimental results, the trap-assisted band-to-band hole injection model is proposed to explain the different behavior of GIDL current for different IL thicknesses.

HfO_2/TiN n-MOSFETs with an IL thickness of 10 and 30 Å were studied in this paper as an element of high-performance 28-nm CMOS technology. Both devices were fabricated using conventional self-aligned transistor flow through the gate first process. For gate first process devices, high quality thermal oxides with different thicknesses of 10 and 30 Å were grown on a (100) Si substrate as an IL oxide layer. After standard cleaning procedures, 30 Å of HfO_2 film was sequentially deposited by atomic layer deposition. Next, 10 nm of TiN film was deposited by radio frequency physical vapor deposition, followed by poly-Si deposition as a low resistance gate electrode. The activation for source/drain and poly-Si gate was performed at 1025 °C. The channel and source/drain doping concentrations were about 3×10^{17} cm^{-3} and 5×10^{22} cm^{-3}, respectively. In this study, the dimensions of the selected devices were 1 μm in both width and length. The devices with IL thickness of 10 and 30 Å were subjected to the maximum substrate current I_{bmax} during CHCS conditions while at 3 V drain voltage (V_d). The stress was briefly interrupted to measure the drain current-gate voltage (I_d-V_g) and substrate current-gate voltage (I_b-V_g) transfer characteristics. GIDL current was measured at $V_g = -0.5$ V and $V_d = 2$ V. All experimental curves were measured using an Agilient B1500 semiconductor parameter analyzer.

Figures 1(a) and 1(b) show the effects of CHCS on the transfer characteristics of I_d-V_g and corresponding I_b-V_g at $V_d = 2$ V for high-k/metal gate n-MOSFETs of different IL thicknesses, respectively. Both devices were stressed at the maximum substrate current I_{bmax} ($V_g \sim V_d/2$) of CHCS conditions while $V_d = 3$ V. Due to interface trap generation during CHCS, the on-current decreases with the peak of I_b increases for both devices. However, there is a noteworthy contrary trend in GIDL for components of different IL thicknesses. For the device with an IL thickness of 30 Å, the

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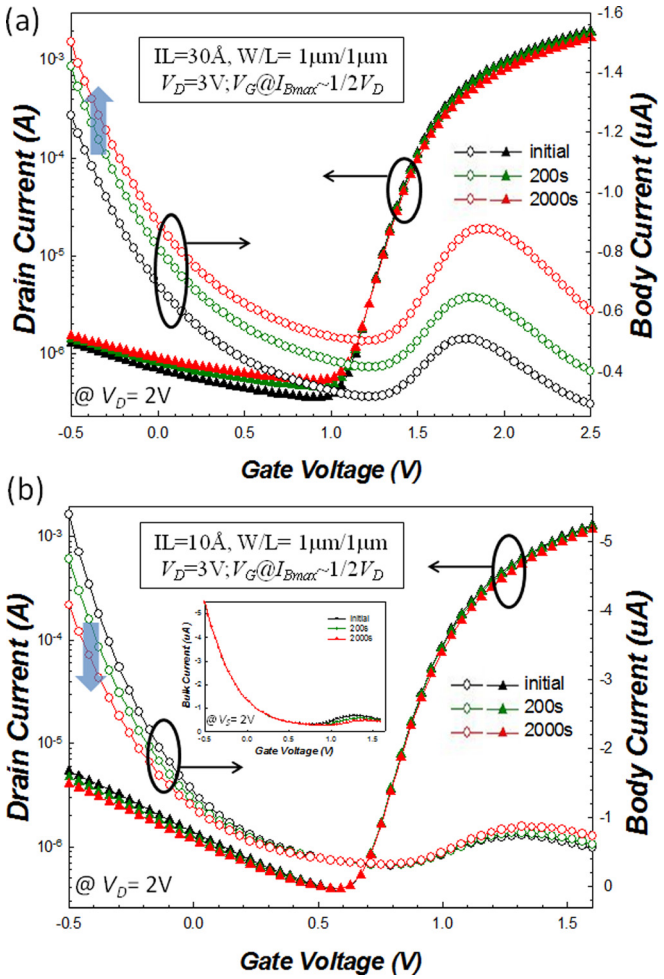

FIG. 1. (Color online) I_d-V_g and corresponding I_b-V_g transfer characteristic curves as a function of stress time during CHCS for devices with (a) 10 Å and (b) 30 Å IL thicknesses. The inset of (b) shows the I_b-V_g curves measured by reverse mode operation (source/drain interchanged).

GIDL current gradually increased during CHCS. This is consistent with the previous reports of conventional n-MOSFETs due to lucky electron trapping in the oxide near the drain side. The negative charge induced by the trapped electrons bends the bands upward, enhances the electric field, and decreases the tunneling distance.[11] However, in the case of a thinner IL (10 Å), CHCS causes a reduction in the GIDL current, as shown in Fig. 1(b). This result implies that as the IL becomes thinner, additional hole trapping occurs during CHCS. The inset of Fig. 2(a) shows the variation of the energy-band diagram taken from drain overlap region under initial and after hole trapping. It can be seen that hole trapping bends the bands downward, reduces the electric field, and consequently increases the tunneling distance. Therefore, the GIDL current gradually decreases during CHCS. No variation in the GIDL component measured by reverse mode operation (source/drain interchanged) was observed, as shown in the inset of Fig. 1(b). This further suggests that trapped holes induced by CHCS occur only near the drain side.

To further confirm the hole trapping region is located mainly in the high-k dielectric, Fig. 2 shows the effect of CHCS on the GIDL characteristics for devices with different high-k thicknesses. As can be seen, the GIDL current shows a gradual decrease with increasing stress time for both cases. In addition, the change of the GIDL current decreases as

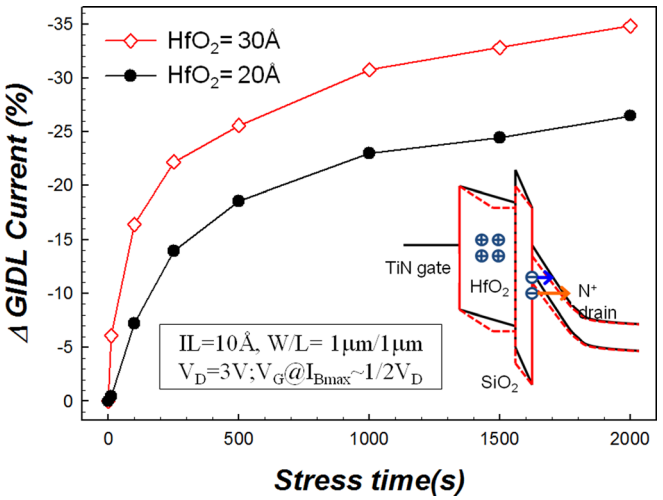

FIG. 2. (Color online) ΔI_{GIDL} versus stress time under CHCS for thin IL oxide devices with different HfO_2 thicknesses. The inset shows the band diagrams before (solid line) and after (dashed line) hole capture by bulk traps.

high-k becomes thinner. This result supplies evidence for the fact that hole injection induced by CHCS is mainly trapped in the bulk of HfO_2 dielectric due to the fact that the physically thinner high-k dielectric results in fewer holes trapping to suppress the GIDL current.

Based on these observations, the ΔI_{GIDL} can be confirmed to have a high dependence on IL thickness of high-k/metal gate stacks. As the IL becomes thinner, the CHCS induces additional hole trapping in the high-k dielectric near the drain side. To investigate the origin of these holes generated by CHCS, devices with thin IL were stressed under low,

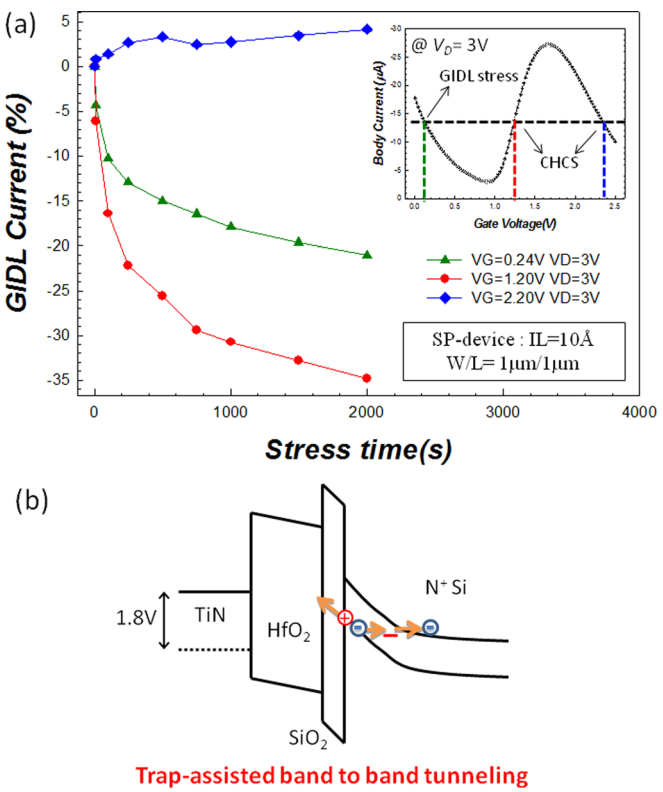

FIG. 3. (Color online) (a) ΔI_{GIDL} versus stress time under various V_g stress conditions with $V_d = 3$ V. The GIDL current is measured at $V_d = 2$ V and $V_g = -0.5$ V. Inset shows substrate current as function of V_g at $V_d = 3$ V. (b) Schematic of energy band diagram of trap-assisted band-to-band hole tunneling model.

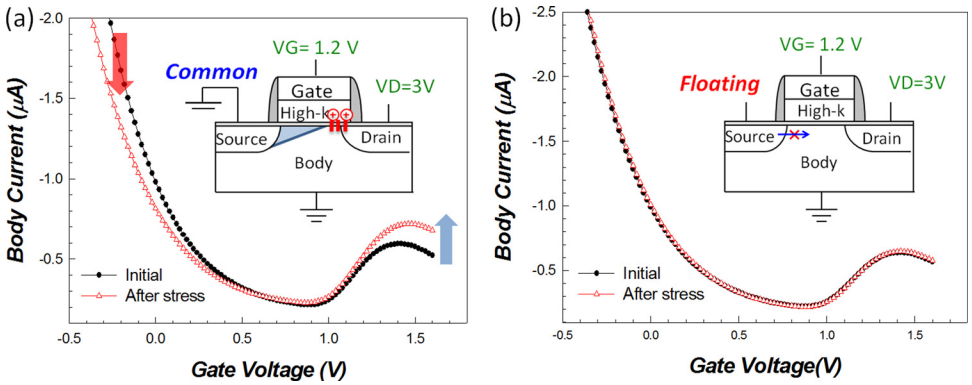

FIG. 4. (Color online) I_b-V_g transfer characteristic curves before and after CHCS for thin IL oxide devices with (a) ground and (b) floating source terminal during stress.

medium, and high V_g stress conditions, while V_d was fixed at 3 V. These include GIDL stress and both hot carrier stress conditions, corresponding to the same value of I_b (-14 μA), as shown in the inset of Fig. 3(a). The ΔI_{GIDL} as function of stress time during these conditions is exhibited in Fig. 3. It can be seen that at high V_g CHCS condition, the GIDL current shows an increase with increasing stress time. This result is contrary to that of a device under $V_g \sim 1/2$ V_d stress condition, meaning that whether or not CHCS induces holes trapped in the high-k dielectric near the drain side is closely related to stress voltage across the gate and drain terminals. On the other hand, while the GIDL stress was applied to an identical device, the GIDL current decreases with increasing stress time. This can be attributed to the band bending downward induced by the band-to-band hot holes trapped in the bulk of high-k dielectric near the drain side. However, it is noteworthy that while the device was stressed at a medium V_g as the hot carrier stress condition, corresponding to the same impact ionization ($I_b = -14$ μA), the magnitude of reduction in GIDL current is much more serious when compared to the GIDL stress condition. This result indicates that the amount of hole injection is not purely dominated by stress voltage across gate and drain terminals. The additional hole trapping induced by CHCS can be attributed to the bulk trap-assisted band-to-band hole tunneling. The diagram of energy band cut from the drain overlap region is shown in Fig. 3(b). It can be seen that these bulk traps caused by CHCS assist hole generation by band-to-band tunneling. Further, if stress voltage across gate and drain voltage is large enough, these additional holes possibly gain enough energy to inject into the bulk high-k dielectric layer near the drain side. This phenomenon cannot be observed for the device with 30 Å IL thickness due to the fact that the thicker IL decreases the possibility of hole injection in the HfO_2 dielectric layer.

To further confirm that this phenomenon of hole trapping during CHCS is mainly determined by the trap-assisted band-to-band hole tunneling process, an identical device, with the exception of a floating or grounded source, was subjected to the CHCS stress condition. It can be seen from Fig. 4(a) that while the source terminal is ground, the hot carriers cause damage in the drain side, leading to suppression of the GIDL component. On the country, Fig. 4(b) shows that the peak of I_b has no change under floating source condition due to the fact that the floating source cannot utilize hot carriers to generate the traps in the drain side. There is also no change in the GIDL component in this stress condition. These results further confirm that trap-assisted band-to-band tunneling is the dominant process causing additional hole generation during CHCS.

This paper investigates the effects of CHCS on the GIDL current in n-MOSFETs with high-k/metal gate stacks. It was found that the behavior of GIDL current during CHCS is dependent upon the IL thickness of the high-k/metal gate stacks. As IL becomes thinner, the CHCS induces additional hole trapping in the high-k dielectric near the drain side, resulting in a ΔI_{GIDL} trend contrary to those of devices with thicker IL or conventional n-MOSFETs. The results of ΔI_{GIDL} at different stress voltages across gate and drain terminals supports trap-assisted band-to-band tunneling as the dominant mechanism responsible for hole generation during CHCS. This mechanism was further verified by applying identical stress conditions to a device with a floating source.

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