High Area-Efficient ESD Clamp Circuit With Equivalent RC-Based Detection Mechanism in a 65-nm CMOS Process

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Abstract—A power-rail electrostatic discharge (ESD) circuit realized with ESD clamp device drawn in the layout style of big field-effect transistor (BigFET), and with parasitic diode of BigFET as a part of ESD-transient detection mechanism, is proposed and verified in a 65-nm 1.2-V CMOS process. Skillfully utilizing the diode-connected MOS transistor as the equivalent large resistor and the parasitic reverse-biased diodes of BigFET as the equivalent capacitors, the new RC-based ESD-transient detection mechanism can be achieved without using an actual resistor and capacitor to significantly reduce the layout area by ∼82%, as compared to the traditional RC-based ESD-transient detection circuit. From the measured results, the new proposed power-rail ESD clamp circuit with body effect of ESD clamp device can perform adjustable holding voltage under the ESD stress condition, as well as better immunity against mistrigger and transient-induced latch-on under fast power-on and transient noise conditions.

Index Terms—Big field-effect transistor (BigFET), electrostatic discharge (ESD), power-rail ESD clamp circuit.

I. Introduction

IN ADVANCED nanoscale CMOS technology, the electrostatic discharge (ESD) clamp device drawn in the layout style of big field-effect transistor (BigFET) had demonstrated excellent ESD protection performance [1]–[6]. In these power-rail ESD clamp circuits, the ESD clamp devices can discharge a large ESD current by the inversion channel layer without snapback operation of the parasitic BJT [7]–[10]. Practically, there are two different circuit skills, namely, the RC-delay technique [1]–[3] and the capacitance-coupling design [4]–[6], to realize the ESD-transient detection circuit in the power-rail ESD clamp circuit. The turn-on duration of the ESD clamp device is mainly controlled by the RC-time constant of the RC-based ESD-transient detection circuit [1]–[3]. Therefore,

the RC-time constant would be designed large enough, about several hundreds of nanoseconds, to keep the ESD clamp device at "ON" state under the ESD stress condition. However, the extended RC-time constant of the ESD-transient detection circuit suffers not only the larger layout area from the resistance and capacitance but also the mistrigger of the ESD clamp device under fast power-on application [2]. In previous studies [1], [2], [5], [6], they demonstrated the power-rail ESD clamp circuits with feedback circuit methods to extend the turn-on duration by using a small RC-time constant. However, the feedback circuit designs would suffer the latch-on issue under the fast power-on or the electrical fast-transient conditions [11]. Moreover, some circuit designs, such as on-time control circuits [1] and multi-RC-triggered circuits [3], had also been used to extend the turn-on duration without the latch-on issue. However, those previous circuits are more complicated with large silicon layout area including the requested resistances and capacitances in the ESD-transient detection circuits.

Low standby leakage of the power-rail ESD clamp circuit is highly demanded by the hand-held, portable, and battery-powered products [6]. In advanced CMOS technology, the leakage current of nMOS was often larger than that of pMOS in the same device dimension. Moreover, pMOS used as ESD clamp device has become important for low voltage and mixed voltage supply in deep submicrometer CMOS products [12], [13]. Hence, pMOS is suggested to be used as the ESD clamp device.

In this paper, a high area-efficient ESD-transient detection circuit, which is combined with the parasitic diode of the ESD clamp pMOS transistor drawn in BigFET layout style, has been proposed and verified in a 65-nm 1.2-V CMOS process. From the measured results, the new proposed power-rail ESD clamp circuit can achieve excellent electrical performances with greatly reduced layout area.

II. Prior Arts of Power-Rail ESD Clamp Circuit

A. Traditional RC-Based Power-Rail ESD Clamp Circuit

The traditional RC-based power-rail ESD clamp circuit was widely used to protect the core circuits [14], as shown in Fig. 1. The RC-based ESD-transient detection circuit commands the ESD clamp nMOS transistor to turn on under ESD stress condition and to turn off under normal circuit operation condition. The turn-on time of the ESD clamp nMOS transistor can be adjusted by the RC-time constant of the RC-based ESD-transient detection circuit to meet the half-energy discharging time of the human-body-model (HBM) ESD event [15]. To
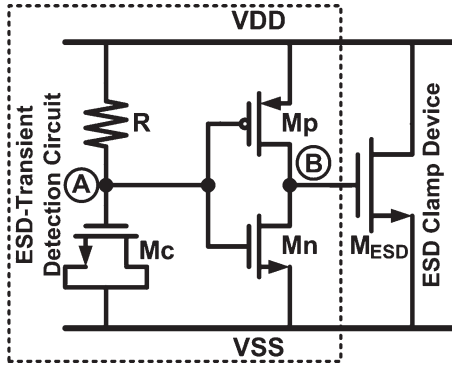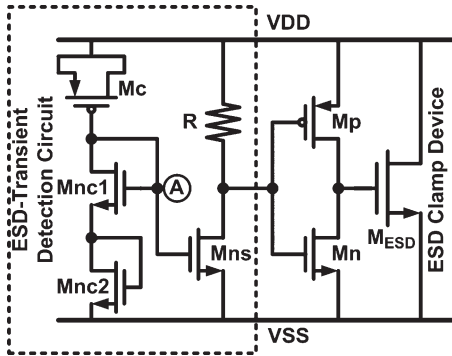
Fig. 1.   Traditional *RC*-based power-rail ESD clamp circuit [14].

Fig. 2.   Power-rail ESD clamp circuit with smaller capacitance design [4].
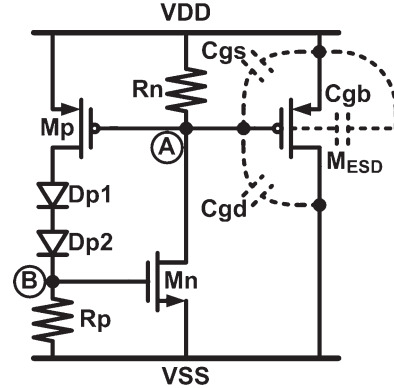

Fig. 3.   Capacitor-less power-rail ESD clamp circuit with diode string in the ESD-transient detection circuit and ESD clamp pMOS transistor [16].

TABLE I
DEVICE DIMENSION OF PRIOR ARTS OF
POWER-RAIL ESD CLAMP CIRCUIT

Device Dimension	Traditional *RC*-Based Design [14]	Smaller Capacitance Design [4]	Capacitor-Less Design [16]
Capacitor (Mc)	64μm / 2μm (W/L)	8μm / 60nm	None
Resistor (Ω)	R = 165.3k	R = 1.8k	Rn = 40k ; Rp = 20k
pMOS Transistor (Mp)	184μm / 60nm	184μm / 60nm	24μm / 60nm
nMOS Transistor (Mn)	36μm / 60nm	36μm / 60nm	12μm / 60nm
Diodes (Dp1 and Dp2)	None	None	0.057μm²
Mnc1, Mnc2, and Mns	None	Mnc1 = 8μm / 60nm Mnc2 = 8μm / 60nm Mns = 60μm / 60nm	None
ESD Clamp Transistor (M_ESD)	2000μm / 100nm (nMOS)	2000μm / 100nm (nMOS)	2000μm / 100nm (pMOS)

meet the aforementioned requirements, the *RC*-time constant of the *RC*-based ESD-transient detection circuit is designed about 0.1–1 μs to achieve the desired operations.

B. Power-Rail ESD Clamp Circuit With Smaller Capacitance

A power-rail ESD clamp circuit with smaller capacitance that adopts the capacitance-coupling mechanism has been shown in Fig. 2 [4]. The smaller capacitor implemented in this work is a MOS capacitor. The cascode nMOS transistors (Mnc1 and Mnc2) operated at the saturation region are used as a large resistor and combined with the smaller capacitor to construct a capacitance-coupling network. Under ESD stress condition, the potential of node A will be synchronously elevated toward a positive voltage potential by capacitance coupling of the smaller capacitor. Then, the gate terminal of the ESD clamp nMOS transistor will be promptly charged toward the positive voltage potential. Under normal circuit operation condition, the potential of node A will actually be kept at VSS through the high-resistance path of the cascode nMOS transistors. Therefore, the ESD clamp nMOS transistor will be kept at the "OFF" state under normal circuit operation condition.

C. Capacitor-less Design of Power-Rail ESD Clamp Circuit

The capacitor-less design of power-rail ESD clamp circuit was also proposed to protect the core circuits [16], as shown in Fig. 3. The large parasitic capacitances (Cgd, Cgs, and Cgb) of the ESD clamp pMOS transistor and the resistor Rn can be used to realize the capacitance-coupling mechanism. Under ESD stress condition, the voltage of node A will be quickly pulled down to the ground level to turn on the ESD clamp pMOS transistor. The diode string in the ESD-transient detection circuit is

used to adjust the holding voltage of the power-rail ESD clamp circuit to avoid from the transient-induced latch-on event [17]. Under normal circuit operation condition, the power-rail ESD clamp circuit can be totally turned off because the voltages of nodes A and B are kept at VDD and VSS through the resistors Rn and Rp, respectively.

The device dimensions of the traditional *RC*-based design [14], the smaller capacitance design [4], and the capacitor-less design [16] fabricated in a 65-nm 1.2-V CMOS process are listed in Table I. The device dimension of M_{ESD} in all power-rail ESD clamp circuits verified in the silicon test chip is kept the same, i.e., 2000 μm/100 nm. It should be noticed that the M_{ESD} used in capacitor-less design is an ESD clamp pMOS transistor.

III. NEW PROPOSED ESD-TRANSIENT DETECTION CIRCUIT

A. Circuit Schematic

The circuit schematic and the cross-sectional view of the new proposed ESD-transient detection circuit with the ESD clamp pMOS transistor drawn in BigFET layout style are shown in Fig. 4(a) and (b), respectively. In Fig. 4(a), the body of ESD clamp pMOS transistor is not connected to VDD but to the diode-connected pMOS transistor Mpd and the input node of the controlling circuit, which is composed of two transistors (Mp and Mn) and two resistors (Rp and Rn). The output node of the controlling circuit is connected to the gate of the ESD clamp pMOS transistor to command M_{ESD} at "ON" or "OFF" state. As shown in Fig. 4(b), there is a large-area reverse-biased diode existed in the body and the drain of ESD clamp pMOS
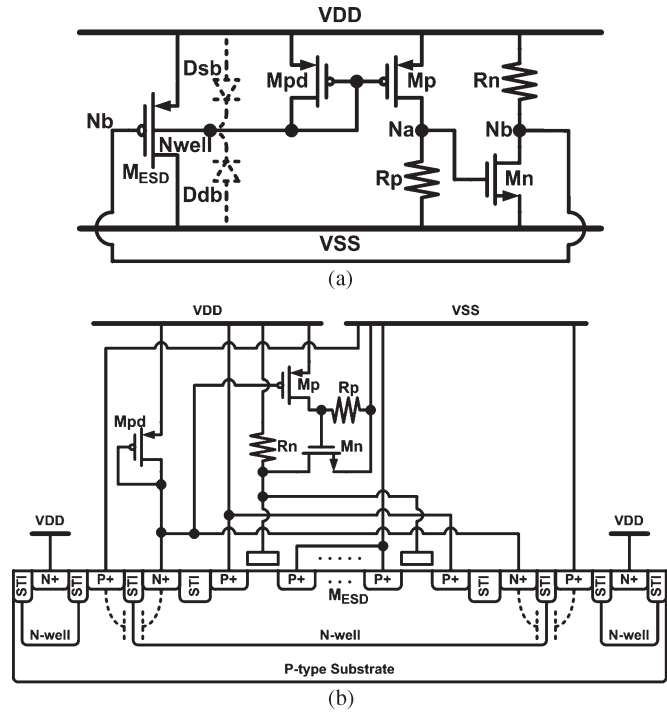
Fig. 4. (a) Circuit schematic and the (b) cross-sectional view of the new proposed ESD-transient detection circuit with the ESD clamp pMOS transistor.

TABLE II
DEVICE DIMENSION OF THE NEW PROPOSED
POWER-RAIL ESD CLAMP CIRCUIT

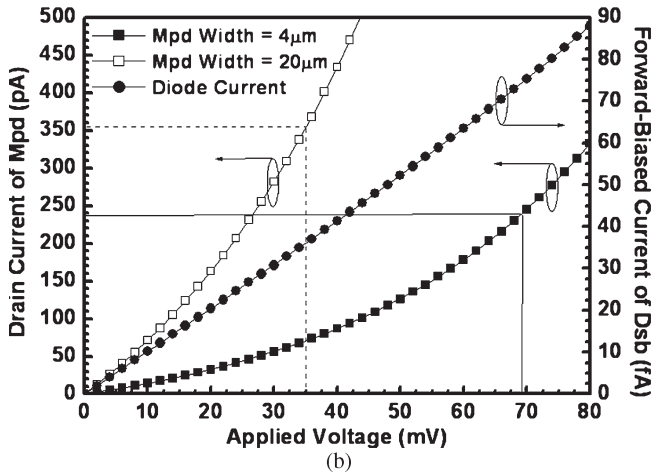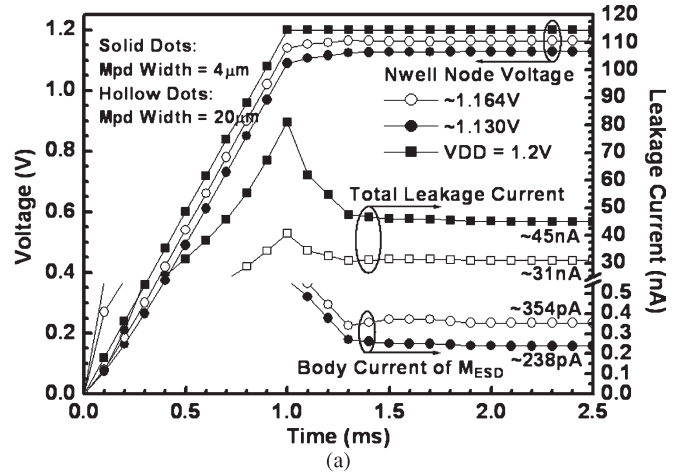| Device Dimension	Ultra-Area-Efficient Power-Rail ESD Clamp Circuit					
Resistor (Ω)	Rn = 3.6k ; Rp = 6k					
MOS Transistors	Mn = 20μm / 60nm ; Mp = 24μm / 60nm					
Diode-Connected Transistor (Mpd)	4μm / 60nm			20μm / 60nm		
ESD Clamp pMOS Transistor (M_{ESD})	2000μm / 100nm	1600μm / 100nm	1200μm / 100nm	2000μm / 100nm	1600μm / 100nm	1200μm / 100nm

Fig. 5. Simulated voltage waveforms on the nodes and the leakage currents of the (a) proposed power-rail ESD clamp circuit under the normal power-on transition and the (b) diode-connected transistor Mpd and forward-biased diode Dsb.

transistor. The other one exists in the body of ESD clamp pMOS transistor and the $P+$ pickup. These two parasitic diodes are used as the equivalent capacitors, and the diode-connected pMOS transistor Mpd is used as the equivalent large resistor. Therefore, an equivalent RC-based ESD-transient detection mechanism is constructed without using an actual resistor and capacitor to significantly reduce the layout area.

B. Operation Under Normal Power-On Transition

Under the normal circuit operation condition, the body voltage of M_{ESD} [Nwell in Fig. 4(a)] can be biased toward VDD through the diode-connected transistor Mpd. The Mpd acts as an equivalent large resistor to charge the Nwell node toward VDD. Then, the controlling circuit can output a voltage level of VDD to command M_{ESD} at "OFF" state.

With the SPICE parameters provided from foundry and the device sizes listed in Table II (adopting an M_{ESD} width of 2000 μm), the simulated voltage waveforms and the leakage current of the proposed power-rail ESD clamp circuit during the normal power-on transition are shown in Fig. 5(a). In Fig. 5(a), the voltage of node Nwell can be smoothly charged to the voltage level near VDD through the Mpd. When the width of Mpd is 4 μm (20 μm), the voltage of node Nwell is charged to 1.130 V (1.164 V). At the same time, the body current of M_{ESD} is 238 pA (354 pA). This body current is obviously not provided by the parasitic forward-biased diode Dsb of M_{ESD}, as shown in Fig. 5(b), because the forward-biased current is only on the order of femtoampere. On the contrary, the drain current of Mpd with 4-μm (20-μm) width is 238 pA (354 pA) when it dissipates ∼69-mV (∼35-mV) voltage drop. Mpd with smaller width would cause larger voltage drop to provide drain current. As a result, Mp would not be completely turned off

to induce more leakage current. Therefore, the simulated total standby leakage current is 45 nA (31 nA) for an Mpd width of 4 μm (20 μm) when VDD is raised up to 1.2 V with a rise time of 1 ms.

C. Operation Under ESD Transition

When a positive fast-transient ESD-like voltage is applied to VDD with VSS grounded, the RC-time constant keeps the node Nwell at a relatively low voltage level as compared with that on VDD power line. The RC-time constant is consisted by the equivalent resistor implemented by Mpd and the equivalent capacitors from the parasitic diodes of Nwell/Psub and Nwell/drain junctions. Consequently, Mp can be quickly turned
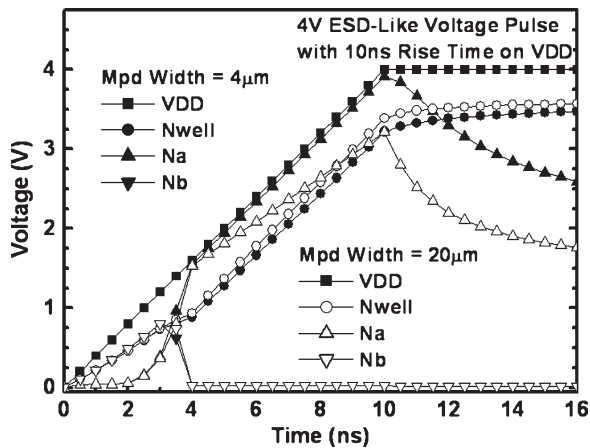
Fig. 6. Simulated voltage waveforms on the nodes of the proposed power-rail ESD clamp circuit under the ESD-like transition.

on, and the controlling circuit can output a voltage level of VSS to command M_{ESD} at "ON" state.

In order to simulate the fast-transient edge of the HBM ESD event before the breakdown on the internal devices, a 4-V voltage pulse with a rise time of 10 ns is applied to VDD. The simulated voltage waveforms of the proposed power-rail ESD clamp circuit during such an ESD-like transition are illustrated in Fig. 6. During this ESD-like transition, the voltage of node Nwell is increased much slower than that on the VDD power line due to RC-time constant at node Nwell. The voltage difference between the VDD power line and node Nwell is nearly kept at the value of turn-on voltage of the diode Dsb. However, such a turn-on voltage of the diode Dsb is still larger than the threshold voltage of Mp to activate the controlling circuit. Therefore, the voltage level of node Nb is successfully pulled down to the VSS level in about 4 ns. Therefore, M_{ESD} can be fully turned on to discharge ESD current from VDD to VSS.

In Fig. 6, the voltages of node Nwell are slightly different under different Mpd widths. The equivalent resistance of Mpd with smaller width is larger than that of Mpd with larger width. As a result, the voltage of node Nwell under smaller Mpd width would be slightly lower due to larger RC-time constant. Moreover, the body and the source of M_{ESD} are not connected together. It will induce the body effect of MOSFET to influence the conduction behavior of M_{ESD}. This phenomenon will be observed and discussed in the following experimental results.

IV. EXPERIMENTAL RESULTS

The test chips of power-rail ESD clamp circuits with the traditional RC-based, smaller capacitance, capacitor-less, and proposed high area-efficient ESD-transient detection circuits have been fabricated in a 65-nm 1.2-V CMOS process, as shown in Fig. 7(a)–(d). The dimension of M_{ESD} in all circuits verified in the silicon test chip is kept 2000 μm/100 nm. Compared with the traditional RC-based power-rail ESD clamp circuit, the layout area of the proposed power-rail ESD clamp circuit is reduced by $\sim$46%, and the layout area of the high area-efficient ESD-transient detection circuit is reduced by $\sim$82%. These circuits are prepared for leakage measurement, ESD robustness and transmission line pulsing (TLP)
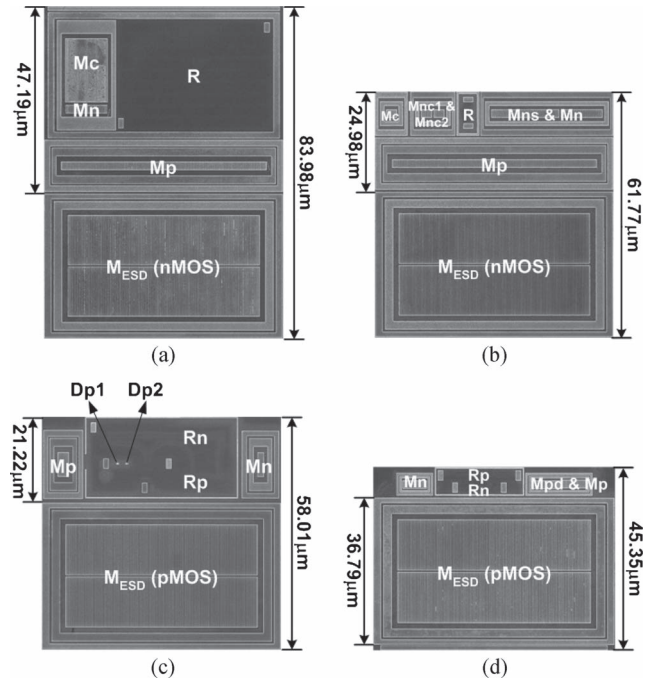

Fig. 7. Chip microphotograph of the fabricated power-rail ESD clamp circuits with the (a) traditional RC-based, (b) smaller capacitance, (c) capacitor-less, and (d) new proposed high area-efficient ESD-transient detection circuits.
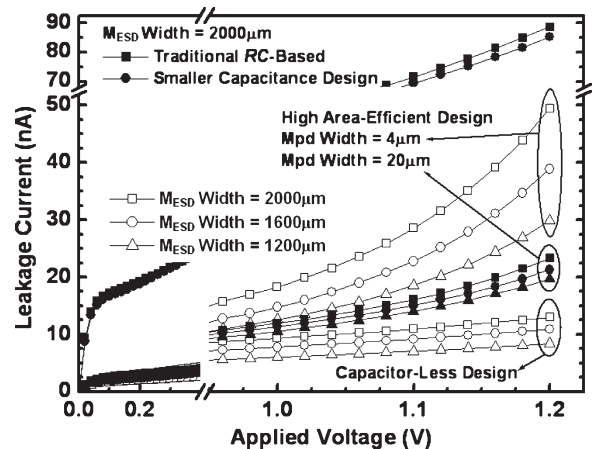

Fig. 8. Measured leakage currents of fabricated power-rail ESD clamp circuits.

measurement, very fast TLP (VF-TLP) measurement, and turn-on verification.

A. Standby Leakage Current Measurement

The leakage currents of the power-rail ESD clamp circuits are measured by HP4155 at 25 °C, as shown in Fig. 8. The leakage currents of the traditional RC-based and the smaller capacitance designs are 88.66 and 85.22 nA, respectively. At the same M_{ESD} width of 2000 μm, the leakage current of the capacitor-less design can be reduced to only 12.97 nA due to the ESD clamp pMOS transistor. For the proposed design, the leakage current is 23.35 nA for an Mpd width of 20 μm. Because the body node of M_{ESD} is not fully biased to VDD, the Mp would not be fully turned off to increase the leakage current [as shown in Fig. 5(a)]. Although the leakage current of the proposed design is slightly larger than that of the capacitor-less

Leakage @ 1.2V	Traditional *RC*-Based [14]	Smaller Capacitance [4]	Capacitor-Less Design [16]		
M_{ESD} Width	2000μm (nMOS)	2000μm (nMOS)	2000μm	1600μm	1200μm
25°C	88.66nA	85.22nA	12.97nA	10.91nA	8.40nA
75°C	0.71μA	0.78μA	0.15μA	0.13μA	0.11μA
125°C	4.74μA	4.83μA	1.37μA	1.09μA	0.82μA

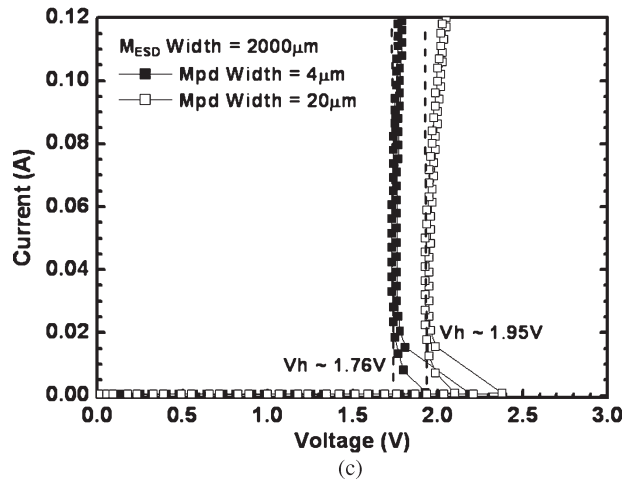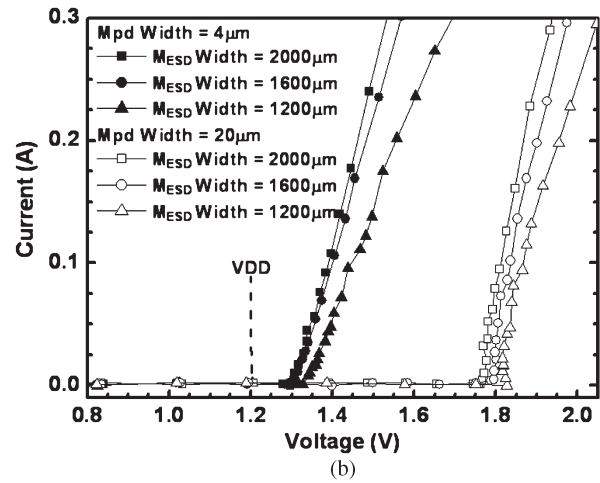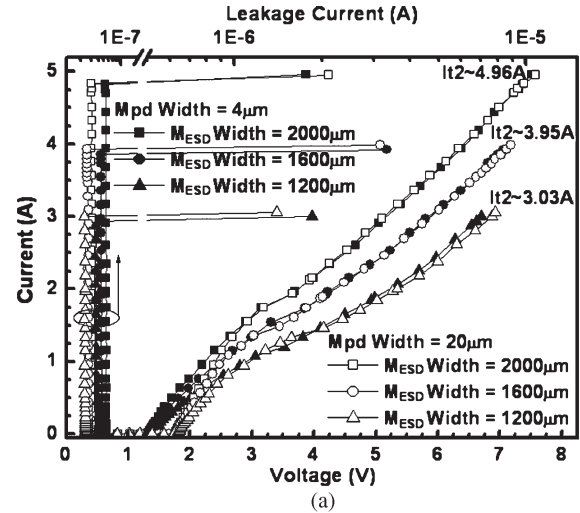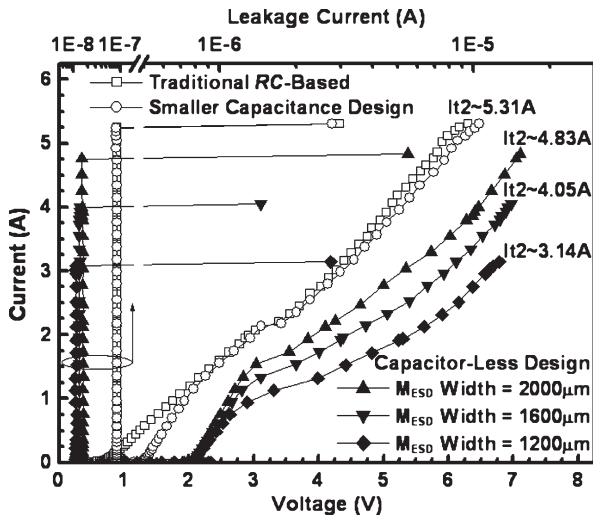| Leakage @ 1.2V	Ultra-Area-Efficient Design					
	Mpd Width = 4μm			Mpd Width = 20μm		
M_{ESD} Width	2000μm	1600μm	1200μm	2000μm	1600μm	1200μm
25°C	49.46nA	38.92nA	29.88nA	23.35nA	21.29nA	19.67nA
75°C	0.34μA	0.26μA	0.22μA	0.22μA	0.19μA	0.15μA
125°C	2.06μA	1.59μA	1.28μA	1.43μA	1.21μA	0.91μA

Fig. 9. TLP measured I–V curves of the power-rail ESD clamp circuits with the traditional RC-based, smaller capacitance, and the capacitor-less designs.

Fig. 10. Measured I–V curves of the proposed power-rail ESD clamp circuits under (a) the TLP measurement, (b) the zoom-in illustration of TLP I–V curves for observing the holding voltages, and (c) the dc I–V measurement by curve tracer.

design, it is still reduced by ∼74%, compared with that of traditional RC-based design. The leakage currents of the power-rail ESD clamp circuits at different temperatures are also listed in Table III. At higher temperatures, it can be observed that the increasing percentage of leakage current of the proposed design is much better than those of the prior art designs.

B. TLP Measurement and ESD Robustness

The TLP generator with a pulsewidth of 100 ns and a rise time of ∼2 ns is used to measure the fabricated power-rail ESD clamp circuits [18]. The measured TLP I–V curves of the prior arts are shown in Fig. 9. The It2 values of the traditional RC-based and the smaller capacitance designs with an M_{ESD} width of 2000 μm are both 5.31 A. However, the It2 of the capacitor-less design is 4.83 A due to the ESD clamp pMOS transistor.

As shown in Fig. 10(a), the It2 of the proposed power-rail ESD clamp circuit can achieve the same level as that of capacitor-less design at the specific M_{ESD} width. To observe the beginning of conduction in Fig. 10(a), the zoom-in illustration of TLP I–V curves is shown in Fig. 10(b). The curves of different Mpd widths start to rise at different voltage levels due to the body effect of M_{ESD}. For the Mpd width of 4 μm, the body effect is worse, and the threshold voltage of M_{ESD} would

be smaller. As a result, the TLP I–V curves for the Mpd width of 4 μm rise at lower voltage level of ∼1.3 V (it is ∼1.8 V for the Mpd width of 20 μm). In addition, the dc I–V curves of the proposed designs are measured (using TEK370 curve tracer) by applying a voltage sweep on the VDD power line to verify the dependence on the body effect of M_{ESD} and the holding voltage

TABLE IV
ESD ROBUSTNESS OF FABRICATED POWER-RAIL ESD CLAMP CIRCUITS

ESD Robustness	Traditional *RC*-Based [14]	Smaller Capacitance [4]	Capacitor-Less Design [16]		
M_{ESD} Width	2000μm (nMOS)	2000μm (nMOS)	2000μm	1600μm	1200μm
It2 (A)	5.31	5.30	4.83	4.05	3.14
HBM (kV)	>± 8	>± 8	>± 8	>± 8	>± 8
MM (V)	+ 650 - 750	+ 650 - 750	+ 500 - 700	+ 400 - 600	+ 300 - 450

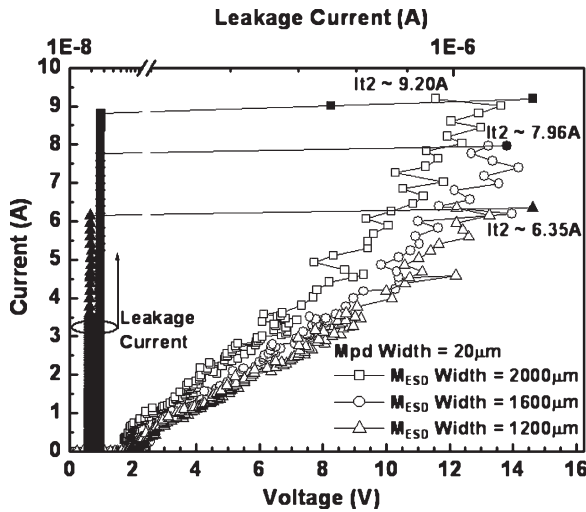| ESD Robustness	Ultra-Area-Efficient Design					
	Mpd Width = 4μm			Mpd Width = 20μm		
M_{ESD} Width	2000μm	1600μm	1200μm	2000μm	1600μm	1200μm
It2 (A)	4.96	3.92	3.00	4.95	3.98	3.06
HBM (kV)	>± 8	>± 8	>± 8	>± 8	>± 8	>± 8
MM (V)	+ 500 - 700	+ 400 - 600	+ 300 - 450	+ 500 - 700	+ 400 - 600	+ 350 - 450

Fig. 11. VF-TLP measured I–V curves of the high area-efficient power-rail ESD clamp circuits with an Mpd width of 20 μm under positive VDD-to-VSS ESD stress.
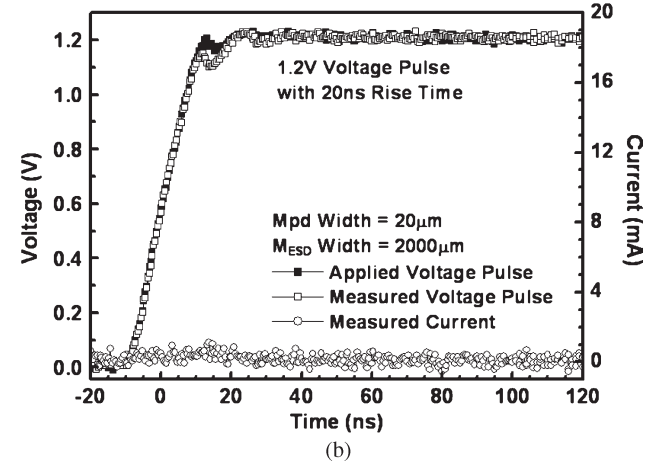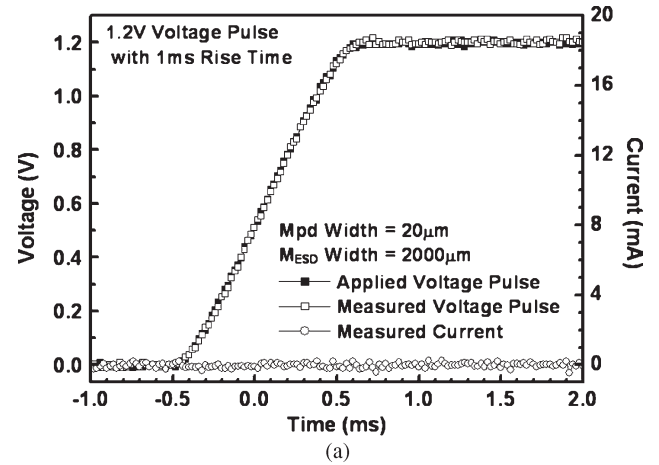

Fig. 12. Measured transient voltage and current waveforms of the high area-efficient power-rail ESD clamp circuit under the 1.2-V power-on transition with rise times of (a) 1 ms and (b) 20 ns.

of the proposed power-rail ESD clamp circuit. In Fig. 10(c), the circuit with the Mpd width of 4 μm surely has lower holding voltage of ~1.76 V due to more serious body effect, and it is high, i.e., ~1.95 V, for the Mpd width of 20 μm when the width of M_{ESD} is kept at 2000 μm. Overall, the measured holding voltages are all higher than the normal circuit operating voltage VDD of 1.2 V no matter what kind of measurement is taken. Hence, the proposed design is free to latchup issue for safely applying in 1.2-V applications [19], [20].

The measured HBM and machine-model (MM) [21] ESD levels under positive and negative VDD-to-VSS ESD stresses are listed in Table IV. The measured HBM (MM) ESD level of the ESD clamp pMOS transistor with the width of 2000 μm is over ±8 kV (+500 V and −700 V). Overall, the measured HBM and MM ESD levels of the proposed power-rail ESD clamp circuits are well proportional to the width of M_{ESD}.

Charged-device model (CDM) is also an important ESD testing standard for ICs. In order to investigate the turn-on behavior of the proposed designs under CDM-like fast-transient condition, the VF-TLP with a pulsewidth of 10 ns and a rise time of 200 ps is used to measure the proposed power-rail ESD clamp circuits. The measured VF-TLP I–V curves of the power-rail ESD clamp circuits with different M_{ESD} widths are shown in Fig. 11, where the width of Mpd is kept at 20 μm.

In Fig. 11, the proposed power-rail ESD clamp circuits can be successfully activated to achieve higher It2 than those measured by TLP measurement due to the shorter pulsewidth of VF-TLP. In addition, the measured It2 from VF-TLP is also well proportional to the width of M_{ESD}.

C. Turn-on Verification

For normal power-on condition, the voltage pulse usually has a rise time on the order of milliseconds. As shown in Fig. 12(a), the measured voltage on VDD power line successfully rises up to 1.2 V in 1 ms without any degradation, and the measured current is near zero. However, some previous studies [4], [11] have demonstrated that the power-rail ESD clamp circuits with RC-based ESD-transient detection circuits were easily mistriggered or into the latch-on state under the fast power-on condition. The proposed power-rail ESD clamp circuit has also been applied with 1.2-V voltage pulse with 20-ns rise time to investigate the immunity against mistrigger under the fast power-on condition, as shown in Fig. 12(b). The measured voltage on VDD power line still can rise up to 1.2 V with tiny deviation in the beginning period of ~5 ns. However, the measured current waveform is smooth at the level near zero. Therefore, the proposed power-rail ESD clamp circuit can be still free from the mistrigger issues.
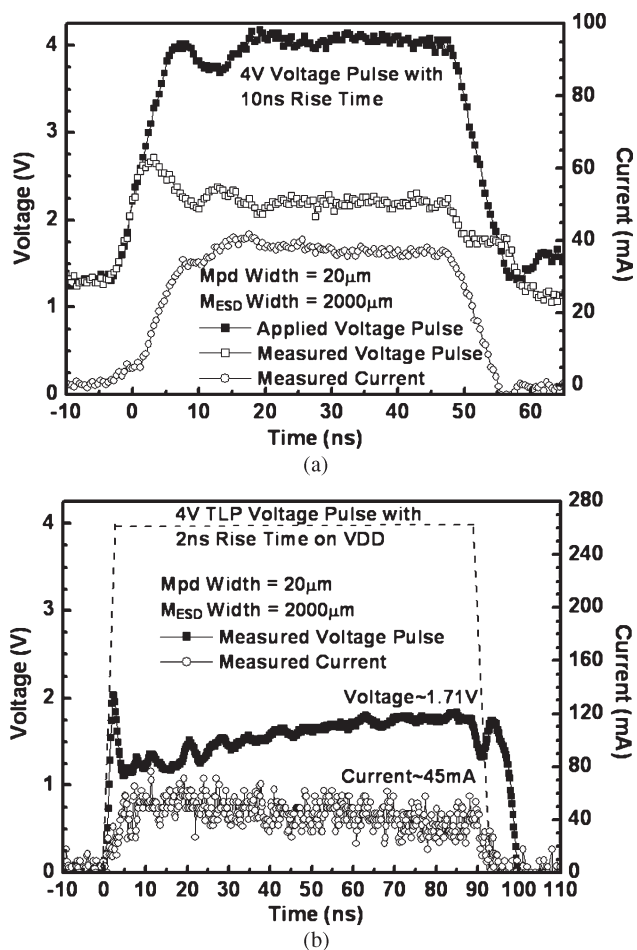
Fig. 13. Measured voltage and current waveforms of the proposed power-rail ESD clamp circuit under (a) transient noise and (b) TLP transition conditions.

The transient voltage with a pulse height of 4 V and a rise time of 10 ns is applied to the VDD power line with 1.2-V normal operation voltage to verify the latch-on issue. As shown in Fig. 13(a), the transient voltage pulse can activate the ESD-transient detection circuit to command M_{ESD} at "ON" state. The applied 4-V voltage pulse is clamped down to a lower voltage level of ∼2.2 V by the proposed power-rail ESD clamp circuit with a discharging current of ∼35 mA. After the transient, the voltage on VDD power line is back to 1.2-V operation voltage, and the current is almost zero.

In order to observe the transient behavior of the proposed power-rail ESD clamp circuit, a TLP voltage pulse with a rise time of 2 ns and a pulse height of 4 V is applied to the VDD power line with the VSS grounded. The TLP voltage pulse can quickly initiate the proposed power-rail ESD clamp circuit. The measured voltage and current waveforms in time domain on VDD power line under 4-V voltage pulse are shown in Fig. 13(b). The applied 4-V voltage pulse can be quickly clamped down to a lower voltage level of ∼1.71 V by the proposed power-rail ESD clamp circuit with the discharging current of ∼45 mA. When the TLP voltage pulse height is increased, the proposed power-rail ESD clamp circuit can discharge more current. The turned-on M_{ESD} can provide a low-impedance path from VDD to VSS to discharge ESD current and clamp down the voltage level. Overall, the proposed high

area-efficient ESD-transient detection circuit can be successfully activated by the voltage pulse with fast-transient edge to turn on the M_{ESD}.

V. Conclusion

The RC-based ESD-transient detection circuit with high area-efficient layout has been proposed and successfully verified in a 65-nm 1.2-V fully silicided CMOS technology. The high area-efficient ESD-transient detection circuit adopts the diode-connected pMOS as an equivalent large resistor and the parasitic diodes as equivalent capacitors to form the equivalent RC-based ESD-transient detection mechanism. According to the measured results, the proposed power-rail ESD clamp circuit has excellent immunity against the transient-induced latch-on or mistrigger issues and good proportionality between the width of M_{ESD} and the ESD robustness. Moreover, the high area-efficient ESD-transient detection circuit saves the layout area by ∼82% compared with the traditional RC-based one. The proposed power-rail ESD clamp circuit is an excellent circuit solution to achieve effective and efficient on-chip ESD protection in advanced nanoscale CMOS process.

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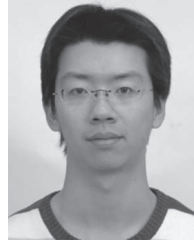
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