Characteristics of Planar Junctionless Poly-Si Thin-Film Transistors With Various Channel Thickness

Horng-Chih Lin, *Senior Member, IEEE*, Cheng-I Lin, Zer-Ming Lin, Bo-Shiuan Shie, and Tiao-Yuan Huang, *Fellow, IEEE*

***Abstract*—N-type junctionless (JL) planar poly-Si thin-film transistors (TFTs), which contain an *in situ* heavily phosphorous-doped channel with thickness ranging from 8 to 12 nm, were fabricated and characterized. The devices exhibit superior current drive and good control over performance variability. From C–V characterization, the ionized dopant concentration in the channel is determined to be around 2×10^{19} cm^{-3} and the fixed charge density to be around -6×10^{12} cm^{-2}. The negative fixed charge density is probably related to the segregation of phosphorous species at the oxide/channel interface. We also observed a reverse short-channel effect from the relationship between the threshold voltage and the channel length. One mechanism considering enhanced phosphorous segregation is proposed to explain this finding.**

***Index Terms*—Fixed charges, junctionless (JL) transistors, poly-Si, short-channel effect, thin-film transistor (TFT).**

I. Introduction

A JUNCTIONLESS (JL) transistor, which is distinctly different from conventional MOSFETs in terms of structure and operation principle, has been recently demonstrated [1], [2]. The JL device employs a heavily doped channel (dopant concentration $\geqq 10^{19}$ cm^{-3} [1]) with doping type the same as that of source/drain (S/D); therefore, the p-n S/D junctions contained in conventional MOSFETs can be eliminated. It can thus skip junction formation issues [3] and greatly simplify fabrication. While early efforts were aimed at providing alternative device technology for applications to extremely scaled CMOS, a nonplanar multigated FinFET [4], [5] structure was employed in the device fabrication. In our previous paper, we demonstrated that excellent JL device performance can be also realized in the fabrication of planar poly-Si thin-film transistors (TFTs) [6] and poly-Si nanowire devices [7]. In this paper, simple and mature *in situ* phosphorous-doped poly-Si deposition processes by low-pressure chemical vapor deposition (LPCVD) were employed in the device fabrication. The fabricated devices exhibit superior current drive with high ON/OFF-current ratios ($> 10^7$) at low operation voltages. These results indicate the feasibility of the JL scheme for large-area electronics [8] as well as 3-D stackable poly-Si-based electronics [9].

With the heavy and homogenous doping concentration throughout S/D and the channel, the operation of the JL devices is drastically different from that of conventional MOSFETs, which rely on the formation of a surface inversion layer between the source and the drain. In contrast, when a JL device is applied with a large gate-overdrive voltage, the current conducts through almost the whole channel region; hence, current drive capability is superior. Nonetheless, the most critical issue for the JL device to properly function is how to turn it off effectively. It is essential that the channel layer must be thin enough to allow full depletion of carriers in the channel by the gate so the device can be effectively turned off. In this paper, we further study the effects of various structural parameters, including the channel thickness and length, on the characteristics of the JL poly-Si TFTs. C–V characterization is also performed to probe the carrier concentration and interface fixed charge density.

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H.-C. Lin is with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, and also with National Nano Device Laboratories, Hsinchu 300, Taiwan (e-mail: hclin@faculty.nctu.edu.tw).

C.-I Lin, B.-S. Shie, and T.-Y. Huang are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan.

Z.-M. Lin is with the Macronix International Co., Ltd., Hsinchu 300, Taiwan.

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II. Device Structure and Fabrication

Fig. 1 shows the structures of planar JL and inversion mode (IM) TFTs characterized in this paper. These devices were fabricated on Si wafers capped with a 200-nm-thick thermal oxide. To reduce the parasitic S/D resistance, 100-nm-thick n$^+$ amorphous-Si was first deposited and patterned to form the S/D pads. For the JL devices, n$^+$ amorphous-Si with thickness of 8, 10, or 12 nm was deposited to serve as the channel. An 8-nm-thick oxide and a 150-nm-thick n$^+$ amorphous-Si layer were subsequently deposited to serve as the gate dielectric and electrode, respectively. All these films were deposited with LPCVD, and the n$^+$ amorphous-Si layers were prepared with an *in situ* phosphorous doping process. From the secondary ion mass spectroscopic measurements, the doping concentration is 10^{20} cm^{-3}. After the

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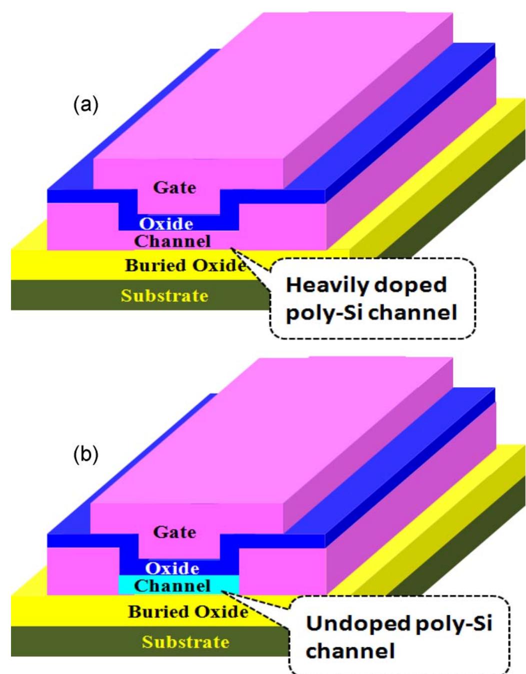

Fig. 1. Three-dimensional view of (a) JL and (b) IM poly-Si TFT fabricated and characterized in this paper. In the structure of the JL device, source, drain, gate, and channel are all composed of n^+ poly-Si.

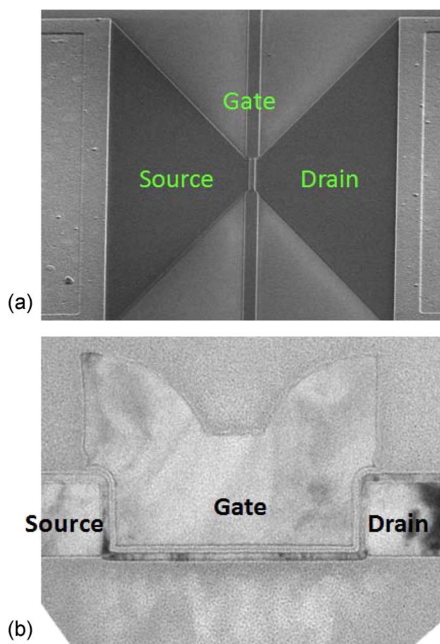

Fig. 2. (a) Top-view SEM and (b) cross-sectional TEM images of a JL device with channel thickness of 10 nm.

definition of the gate electrode, a 200-nm-thick CVD oxide was deposited at 700 °C to passivate the devices. This step also helps recrystallize amorphous-Si and activate the dopants contained in the films. Standard back-end processing was subsequently performed to complete the fabrication. For comparisons, control devices with an undoped channel of 10 nm were also fabricated with the same process flow, except the deposition of the channel layer. Fig. 2(a) and (b) shows the planar scanning electron microscopic (SEM) and transmission electron microscopic (TEM) images of a fabricated device. It can be seen that the film thickness is quite uniform.

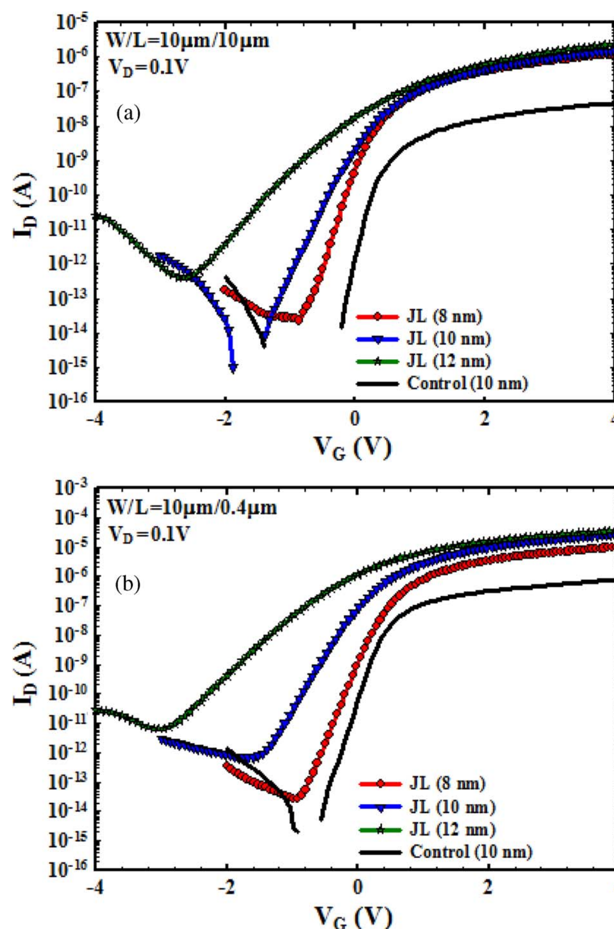

Fig. 3. Typical transfer characteristics of all splits of devices with channel length of (a) 10 and (b) 0.4 μm.

III. Device Structure and Fabrication

A. Fundamental Device Characteristics

Typical transfer characteristics of the fabricated devices with nominal channel length (L) of 10 and 0.4 μm and width (W) of 10 μm are shown in Fig. 3(a) and (b), respectively. It is seen in the figures that the threshold voltage (V_{th}) of the JL devices reasonably decreases with increasing channel thickness. Moreover, JL devices show well-behaved switching characteristics, although the subthreshold slope (SS) is worse than that of the IM one. Fortunately, the SS significantly improves as the channel thickness is reduced. Fig. 4 shows typical transfer characteristics of JL devices measured under $V_D = 0.1$ and 4 V with L of 0.4 μm. As can be seen in the figure, drain-induced barrier lowering significantly increases as the channel thickness is larger than 10 nm. In addition, found is a dramatic rise in the OFF-state leakage as V_D is increased to 4 V. The current is mainly due to gate-induced drain leakage, since it is strongly dependent on $(V_D - V_G)$ and much larger than the gate leakage current. We believe that it is also related to the sharp drain corner [see Fig. 2(b)], which tends to enhance the local electric field as operated in the OFF-state regime and can be reduced by rounding the corner or tapering the sidewall of the S/D pads.

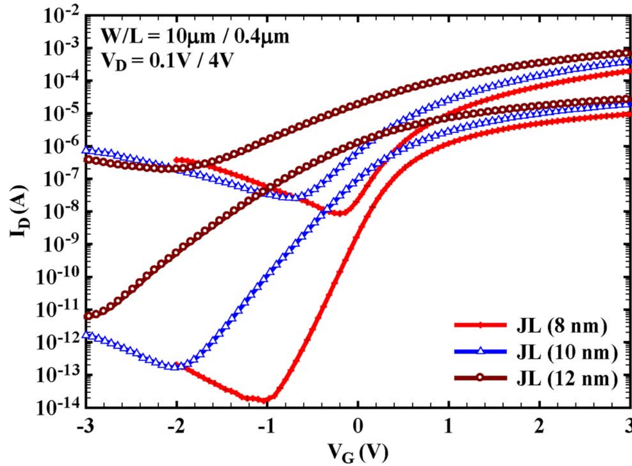

Fig. 4. Typical characteristics of JL devices with channel width of 10 μm and length of 0.4 μm.

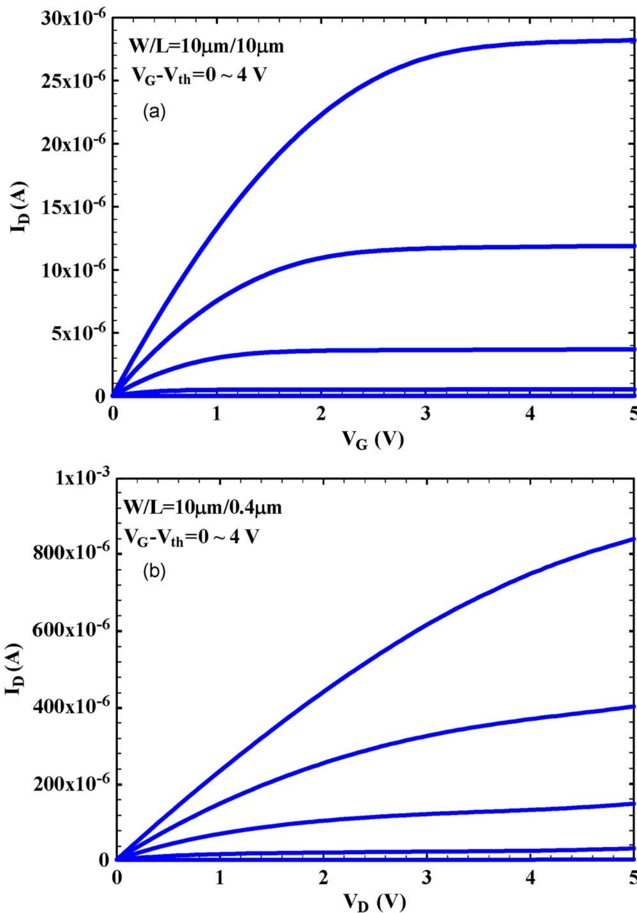

Fig. 5. Output characteristics of JL devices with channel thickness of 10 nm, width of 10 μm, and length of (a) 10 and (b) 0.4 μm.

The most striking feature of the JL TFTs is arguably the drastic increase in ON-current over the undoped-channel counterparts. This is further evidenced with typical output characteristics of the JL and control devices shown in Figs. 5 and 6, respectively. In the figures, we can see that the current enhancement seems to decrease as the channel length is reduced. Fig. 7(a) shows the drain current extracted at $V_G - V_{\rm th} = 4$ V as a function of L for all splits of devices. The current enhancement at a fixed gate overdrive for JL devices with respect to that of the control devices is obvious, particularly for the long-channel devices. Among the JL splits, the current becomes larger as the channel thickness increases, mainly owing to the increase in the cross-sectional area of current conduction. This is confirmed in Fig. 8, in which I_D normalized to channel thickness $(T_{\rm ch})$ as a function of V_G is shown for long-channel JL devices with various $T_{\rm ch}$. Fig. 7(b) shows the enhanced current ratio of the JL devices (with respective to that of the control ones) as a function of channel length. For the devices with L of 10 μm, the current drive can be over 25–40 times larger over the control samples. Such drastic improvement is attributed to the significant reduction in both channel and S/D series resistances (denoted by $R_{\rm ch}$ and $R_{\rm S/D}$, respectively). The extracted resistance values based on a previously developed scheme [10], [11] are shown in Fig. 9. As expected, the $R_{\rm ch}$ of the JL devices is significantly lower than that of the IM ones. Moreover, despite having the same S/D pad structure, $R_{\rm S/D}$ is also reduced when the JL scheme is adopted. This is ascribed to the elimination of the spreading resistance component presenting at the intersection between the S/D junctions and channel of the IM devices [12]. Nonetheless, in Fig. 7(b), we can also see that the enhancement ratio decreases with decreasing L. This can be partly ascribed to the fact that the weight of $R_{\rm ch}$ in affecting the ON-current is reduced in the short-channel regime. Another reason for this trend is the diffusion of dopants into the undoped channel regions of the IM devices, resulting in a shorter effective channel length.

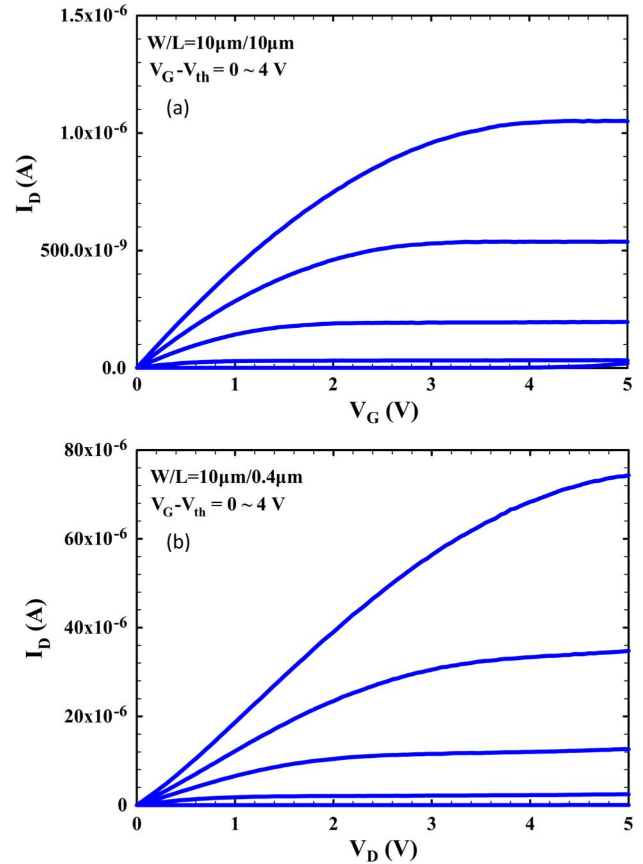

Fig. 6. Output characteristics of control devices with channel thickness of 10 nm, width of 10 μm, and length of (a) 10 and (b) 0.4 μm.

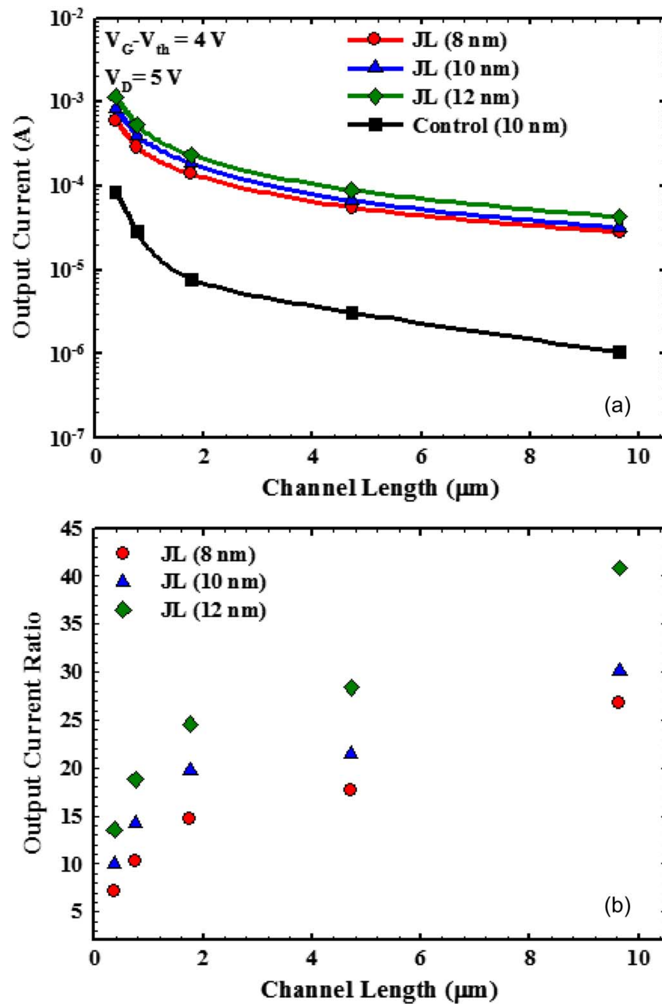

Fig. 7. (a) ON-current extracted at gate overdrive of 4 V for all splits of devices as a function of L. (b) ON-current enhancement ratio of the JL devices over the control ones as a function of L.

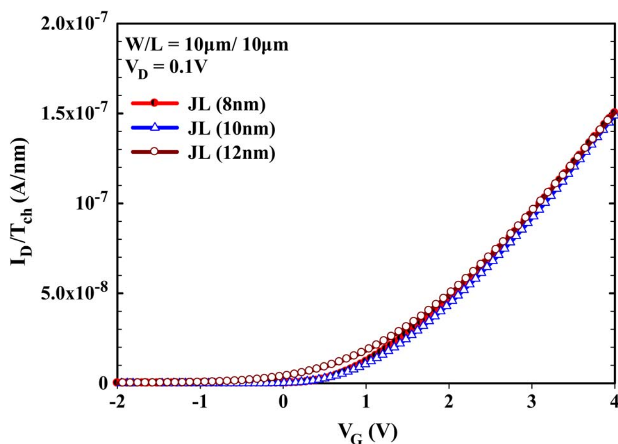

Fig. 8. Transfer curves of JL devices with drain current normalized to the channel thickness.

B. C–V Characterization

For each split of JL devices, C–V characterization was performed under the frequency of 100 or 10 kHz on two devices on the same die with feature sizes of $W \times L$ of 10×10 μm^2 and 20×20 μm^2, respectively, in order to eliminate the parasitic capacitance components associated with the S/D and test pads. The measurement setup is the same as that described in [13]. The Si bulk substrate was grounded during the measurements. The difference between the measured capacitance values of the two devices is divided by the area difference (i.e., 300 μm^2) to obtain the channel capacitance component per unit area. Fig. 10 shows typical C–V characteristics at 100 kHz obtained from the JL split with channel thickness of 10 nm using the above approach. In the figure, it can be seen that the measured capacitance (C) tends to saturate and eventually becomes constant as V_G is sufficiently large—an indication that electrons start to accumulate at the interface between the channel and the gate oxide, and thus, C is constant and equal to $C_{\rm ox}$, which is the gate oxide capacitance per unit area. This occurs as V_G is equal to or larger than the flatband voltage $(V_{\rm FB})$, and the oxide thickness can be extracted from the measured capacitance. On the other hand, as V_G decreases from $V_{\rm FB}$, a surface depletion region begins to appear at the channel surface, and hence, C is equal to the series connection of the gate oxide capacitance and the capacitance attributed by the depletion region in the silicon channel $(C_{\rm dep})$, i.e.,

$$\frac{1}{C} = \frac{1}{C_{\rm ox}} + \frac{1}{C_{\rm dep}} \tag{1}$$

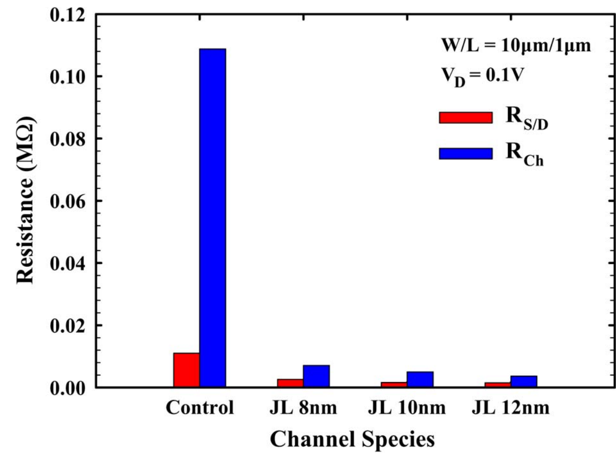

Fig. 9. (a) Extracted channel resistance ($R_{\rm ch}$, for $W/L = 10$ μm$/1$ μm) and S/D resistance $(R_{\rm S/D})$ components for all splits of devices.

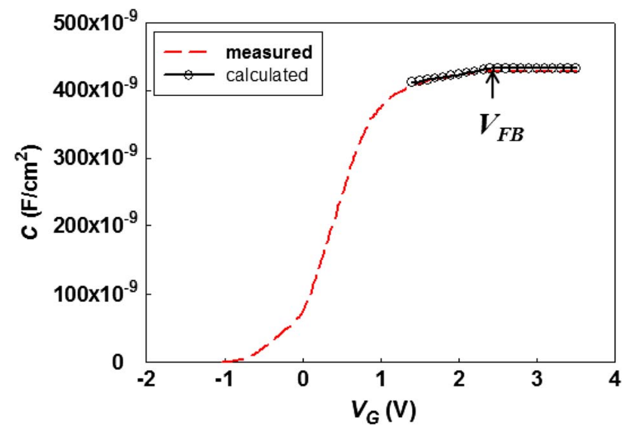

Fig. 10. Capacitance of the channel versus gate voltage obtained from the JL devices with channel thickness of 10 nm.

TABLE I
PARAMETERS EXTRACTED FROM THE C–V RESULTS OF JL DEVICES WITH VARIOUS CHANNEL THICKNESS

Channel thickness (nm)	8	10	12
Gate oxide thickness (nm)	8	8	8.2
Ionized dopant concentration (x10^{19} cm^{-3})	1.7	2.2	2.2
Flat-band voltage, V_{FB} (V)	2.6	2.4	2
Fixed charge density (x10^{12} cm^{-2})	-6.8	-6.5	-5.5

$$C_{\rm dep} = \frac{\varepsilon_{\rm si}}{X_{\rm dep}} \tag{2}$$

where $\varepsilon_{\rm si}$ and $X_{\rm dep}$ are the dielectric constants of silicon and the depletion layer thickness, respectively. It is further assumed that the effective doping concentration in the channel is N_D, which is less than the practical chemical concentration of the incorporated phosphorous species due to the occurrence of precipitation and segregation. By solving the 1-D Poisson equation along the direction perpendicular to the channel, i.e.,

$$\frac{d^2\phi(x)}{dx^2} = \frac{-qN_D^+}{\varepsilon_{\rm si}} \tag{3}$$

where q and N_D^+ are the electronic charge and ionized dopant concentration in the channel, respectively, and N_D^+ is very close to the free-carrier concentration at room temperature [14]. Note that $x = 0$ at the oxide/channel interface and > 0 in the channel. The Poisson equation can be solved with the boundary conditions that both electric field and potential at $x = X_{\rm dep}$ are zero. We can then obtain $X_{\rm dep}$. Thus

$$X_{\rm dep} = -\frac{\varepsilon_{\rm si}}{C_{\rm ox}} + \sqrt{\left(\frac{\varepsilon_{\rm si}}{C_{\rm ox}}\right)^2 - \frac{2\varepsilon_{\rm si}(V_G - V_{\rm FB})}{qN_D^+}}. \tag{4}$$

Note that $X_{\rm dep} = 0$ as V_G is equal to or larger than $V_{\rm FB}$; thus, C is solely contributed by the gate oxide capacitance and remains constant in this region. As V_G decreases from $V_{\rm FB}$, the depletion layer starts to appear and widen with decreasing V_G; hence, the measured capacitance decreases according to (1). Therefore, we can determine the oxide thickness from the constant C value as $V_G > V_{\rm FB}$, where $V_{\rm FB}$ is the V_G corresponding to the point when C starts to deviate from the constant C. Moreover, N_D (and thus free-carrier concentration) can be extracted by fitting the experimental data in the region as $V_G < V_{\rm FB}$ based on (1), (2), and (4). From the extracted $V_{\rm FB}$, the fixed charge density at the oxide/channel interface can be further derived. Fig. 10 shows the results of measurements performed on devices with channel thickness of 10 nm. It can be seen that the theoretical evaluation can well describe the measured data in the region with $V_G > 1.5$ V, and $V_{\rm FB}$ is determined to be 2.4 V. Similar measurement procedures were also executed on the other two splits, and Table I summarizes the major parameters extracted from the JL devices. Note that the gate oxide thickness (8–8.2 nm) is quite close to that observed in the TEM image [see Fig. 2(b)]. $V_{\rm FB}$ is found to be in the range of 2–2.6 V, and ionized dopant concentration ($\sim$carrier concentration) is around 2×10^{19} $\rm cm^{-3}$. It is worth noting that $V_{\rm FB}$ is larger than $V_{\rm th}$—a feature normally seen for JL devices [15]. We estimate the fixed charge density, i.e., $Q_{\rm fix}$, at the oxide/channel interface with the following form [16]:

$$V_{\rm FB} = -\left(\frac{E_g}{2} - \frac{kT}{q}\ln\left(\frac{N_D^+}{n_i}\right)\right) - \frac{Q_{\rm fix}}{C_{\rm ox}}. \tag{5}$$

Here, we simply assume that the Fermi level of the gate electrode is pinned at the conduction band edge since the carrier concentration of the gate is much higher than that in the ultrathin channel. Interestingly, the fixed charge density estimated from $V_{\rm FB}$ is found to be negative and on the order of 10^{12} $\rm cm^{-2}$. Although the origin for such negative fixed charges is not clear, segregation of phosphorous at the interface [17], [18] is postulated to be responsible. It might be also related to the LPCVD *in situ* doping process, which might enhance phosphorous segregation. More efforts are now in progress to understand the nature of the fixed charges.

It should be noted in Fig. 10 that theoretical fitting fails as V_G is smaller than 1.5 V. This is because the remaining neutral region in the bottom of the channel is too thin to serve as a ground plane. As a result, the parasitic capacitance components related to the underlying bulk-Si substrate [13] (e.g., substrate-to gate/S/D capacitance values) would participate in the measurements and make the measured value significantly lower than that estimated with (1).

From the extracted carrier concentration shown in Table I and the channel resistance shown in Fig. 9, the effective mobility of the JL devices can be estimated and found to be 6.5, 5.7, and 6.5 $\rm cm^2/V \cdot s$ for devices with channel thickness of 8, 10, and 12 nm, respectively. The results indicate that the mobility has a weak dependence on the channel thickness. For comparison, the field-effect mobility of the control devices extracted from transconductance is found to be around $1-2$ $\rm cm^2/V \cdot s$. The rather low values are attributed to the ultrathin body and the lack of plasma treatment. Although the field-effect mobility is obtained from the control devices with operation principles different from the JL devices, the information still indicates that, in addition to the abundant carrier concentration, the superior mobility of the JL devices [19] is another factor responsible for the good current drive.

C. Short-Channel Characteristics

Fig. 11(a) and (b) shows SS and $V_{\rm th}$, respectively, as a function of L. For the JL devices, owing to the existence of a depletion layer in the channel when operated in the subthreshold regime, the equivalent oxide thickness is thicker than that of conventional inversion-mode devices. This is the major origin responsible for the observation that the JL devices exhibit larger SS over the control devices. Fortunately, the SS can be dramatically reduced as the channel thickness of the JL devices is reduced. As can be seen in the figure, the SS is smaller than 300 mV/dec and weakly dependent on L as the channel is downscaled to 10 nm or beyond. In Fig. 11(a), $V_{\rm th}$ is defined as V_G at $I_D = 10^{-9} \times W/L$ (A). As L is larger than 1 μm, the $V_{\rm th}$ rolloff is not obvious except for the JL device with the largest channel thickness of 12 nm. Moreover, an interesting reverse short-channel effect is observed for all splits of devices.

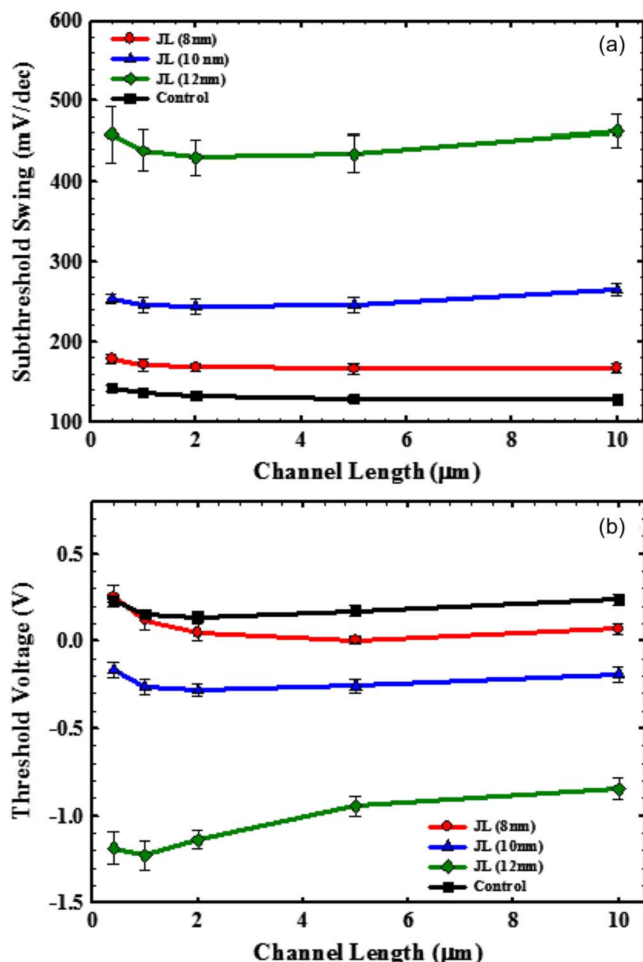

Fig. 11. (a) Subthreshold swing and (b) $V_{\rm th}$ as a function of L. At least 11 devices were measured for each datum point.

The reason behind this observation is postulated to be related to dopant segregation. As shown in the previous section, that a negative fixed charge density presenting at the Si/oxide interface of the JL devices is identified with the C–V measurements and is attributed to the segregation of phosphorous elements. The segregation of phosphorous is expected to be more severe at the S/D edges due to the thick S/D pads, which serve as the reservoir of phosphorous dopants. The excessive dopants would diffuse into the channel and get segregated at the gate oxide interface (see Fig. 12). The density of fixed negative charges is thus higher at the channel edges—the observation of the reverse short-channel effect.

IV. Conclusion

N-type planar JL poly-Si TFTs were fabricated and characterized. The source, drain, gate, and channel of the JL devices are all composed of *in situ* heavily doped poly-Si layers. Impacts drawn from major structural factors such as channel thickness and length on the characteristics of the fabricated devices were explored. The results demonstrate that JL poly-Si TFTs exhibit superior current drive. An interesting finding from C–V characterization is the presence of negative fixed charges at the channel/oxide interface. Although the major reason behind this observation is still under investigation, segregation of phosphorous elements at the interface is postulated to be the main culprit. This paper also observes an interesting reverse $V_{\rm th}$ rolloff phenomenon. Enhanced segregation at the channel edges due to the thick S/D pads is postulated to be responsible for this phenomenon.

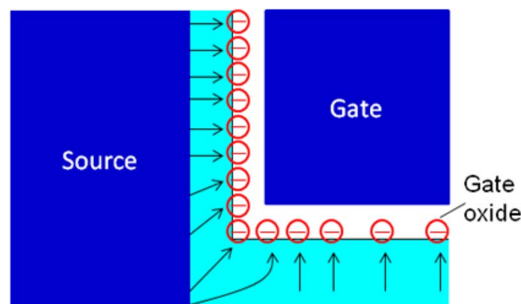

Fig. 12. Enlarged view of the channel region near the source pad, schematically illustrating the generation of negative fixed charges due to phosphorous segregation at the oxide/Si interface. More dopant segregation occurs at the channel edge due to the diffusion of copious phosphorous dopants contained in the thick pads. The arrows indicate the flows of phosphorous species before being segregated.

Acknowledgment

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Horng-Chih Lin (S'90–M'94–SM'01) received the Ph.D. degree in electronics engineering from National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 1994.

In 2004, he joined the NCTU, where he is currently a Professor.

Cheng-I Lin received the B.S.E.E. degree in electrical engineering from National Central University, Taoyuan, Taiwan, in 2007. He is currently working toward the Ph.D. degree at National Chiao Tung University, Hsinchu, Taiwan.

Zer-Ming Lin received the Ph.D. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2011.

In 2011, he joined Macronix International Co., Ltd.

Bo-Shiuan Shie received the M.S. degree from National Tsing Hua University, Hsinchu, Taiwan, in 2009. He is currently working toward the Ph.D. degree at National Chiao Tung University, Hsinchu.

Tiao-Yuan Huang (S'78–M'78–SM'88–F'95) received the Ph.D. degree from The University of New Mexico, Albuquerque, NM, USA, in 1981.

Since 1995, he has been a Professor with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan.