Al_2O_3 Interface Engineering of Germanium Epitaxial Layer Grown Directly on Silicon

Yew Heng Tan, Kwang Sing Yew, Kwang Hong Lee, Yao-Jen Chang, Kuan-Neng Chen, *Senior Member, IEEE*, Diing Shenp Ang, *Senior Member, IEEE*, Eugene A. Fitzgerald, and Chuan Seng Tan, *Member, IEEE*

***Abstract*—The quality of germanium (Ge) epitaxial film grown directly on silicon (Si) substrate is investigated based on the electrical properties of a metal–oxide–semiconductor capacitor (MOSCAP). Different thermal cycling temperatures are used in this study to investigate the effect of temperature on the Ge film quality. Prior to high-k dielectric deposition, various surface treatments are applied on the Ge film to determine the leakage current density using scanning tunneling microscopy. The interface trap density $(D_{\rm it})$ and leakage current obtained from the C–V and I–V measurements on the MOSCAP, as well as the threading dislocation density (TDD), show a linear relationship with the thermal cycling temperature. It is found that the Ge epitaxial film that undergoes the highest thermal cycling temperature of 825 °C and surface treatment in ultraviolet ozone, followed by germanium oxynitride (GeO_xN_y) formation, demonstrates the lowest leakage current of $\sim 2.3 \times 10^{-8}$ A/cm^2 (at -2 V), $D_{\rm it} \sim 3.5 \times 10^{11}$ cm^{-2}/V, and TDD $< 10^7$ cm^{-2}.**

***Index Terms*—Germanium (Ge), interface state density, interfacial layer, oxide.**

I. Introduction

SILICON (Si) integrated circuits have reached the stage whereby their performance growth is unlikely to depend solely on geometrical scaling [1], [2]. Moving forward, it is widely accepted that innovations such as new device structures and new materials have to be integrated on silicon in order to boost the performance of the transistors [3]. Germanium (Ge) has emerged as a suitable material to augment the performance of Si since it has a much higher mobility for both electrons and holes [4]. However, Ge is known to exhibit poor interface quality with high-k dielectrics [5], resulting in degraded carrier mobility, high gate leakage current density (J_g), and large flatband voltage $(V_{\rm fb})$ shift [4]. Hence, surface preparation and interface control on the Ge surface prior to high-k dielectric deposition are a challenging issue that must be resolved in order to realize Ge as a channel material. In addition, Ge integration on Si substrate often results in a defective film due to a 4.2% lattice mismatch, and hence, the threading dislocation density (TDD) needs to be properly optimized.

Germanium oxynitride (GeO_xN_y) is considered a promising interfacial layer for high-k/Ge gate stack since it has better thermal and chemical stability and a higher dielectric constant than native Ge oxides (both GeO and GeO_2) [5], [6]. In addition, the incorporation of nitrogen into Ge oxides could reduce the potential of interdiffusion between the gate dielectric and substrate and/or the gate electrode [7]. Thus, nitride-based dielectrics can be used as an ideal buffer layer for high-k dielectrics and as a gate insulator for Ge-based FETs [8]. In an attempt to further improve the quality of the high-k dielectric, ultraviolet (UV) ozone (UVO) was used to directly oxidize sputtered Zr film to form ZrO_2 [9]. Interspersed *in situ* room-temperature UVO annealing was applied to reduce the leakage current of atomic-layer-deposited HfO_2 [10]. The GeO_xN_y layer could be achieved by various methods such as rapid thermal oxidation (RTO) and consecutive nitridation [11], [12], pretreatment by an inductively coupled ammonia (NH_3) plasma source [13], plasma oxidation followed by *in situ* plasma nitridation [14], and RTO followed by rapid thermal nitridation (RTN) [7]. NH_3 is chosen because of its ability to incorporate more nitrogen into the oxynitride film than other nitridation agents [7]. In most of the reported works, the oxynitride film was deposited on a Ge substrate. Hence, high-quality GeO_xN_y can be obtained by LPCVD and RTN at a relatively high temperature (600 °C and above). In the case of thin Ge film grown on Si substrate (100) (i.e., Ge/Si), using LPCVD or RTN would cause severe Ge/Si interdiffusion that would degrade the quality of the deposited GeO_xN_y. We report a simplified way to deposit GeO_xN_y on Ge/Si using plasma-enhanced chemical vapor deposition (CVD) (PECVD). The Ge/Si samples were first treated in UVO (300 s in O_2 environment) prior to GeO_xN_y deposition by PECVD in NH_3 environment.

In the first part of this paper, the leakage current of various GeO_xN_y layers (that are prepared with several methods) on the Ge epitaxial layer grown directly on Si is studied using scanning tunneling microscopy (STM). Results from this study are used to select the most appropriate interfacial layer in the subsequent metal–oxide–semiconductor (MOS) capacitor (MOSCAP) fabrication. In the second part of this paper, MOSCAP is fabricated by depositing Al_2O_3 high-k dielectric and TiN metal gate on the Ge epitaxial films (with GeO_xN_y

Manuscript received July 17, 2012; revised September 25, 2012; accepted October 12, 2012. Date of publication November 16, 2012; date of current version December 19, 2012. This research was supported by the National Research Foundation Singapore through the Singapore MIT Alliance for Research and Technology's Low Energy Electronic Systems research programme. The review of this paper was arranged by Editor R. Huang.

Y. H. Tan, K. S. Yew, D. S. Ang, and C. S. Tan are with Nanyang Technological University, Singapore 639798 (e-mail: EYHTan@ntu.edu.sg; E080086@e.ntu.edu.sg; edsang@ntu.edu.sg; tancs@ntu.edu.sg).

K. H. Lee and E. A. Fitzgerald are with the Singapore–MIT Alliance for Research and Technology, Singapore 117543 (e-mail: kwanghong@smart.mit.edu; eafitz@mit.edu).

Y.-J. Chang and K.-N. Chen are with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: willysdog@hotmail.com; knchen@mail.nctu.edu.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2012.2225149

interfacial layer) that are prepared at different postgrowth thermal cycling temperatures. Based on the C–V and I–V measurements on the fabricated MOS, the electrical properties of the gate stack such as interface trap density $(D_{\rm it})$ (as determined by the conduction technique [15]) and leakage current are obtained. The postgrowth cyclic annealing temperature on the Ge epitaxial layer is found to have a positive effect on the overall robustness and quality of the gate stack.

II. Experimental

Silicon wafers (diameter = 150 mm, p-type, resistivity = $4-10\ \Omega\cdot$cm) were cleaned using RCA solution, dried, and loaded into N_2-purged load–lock of the ASM Epsilon 2000 reduced-pressure CVD reactor. To initiate the growth, each wafer was transferred to the growth chamber and baked in hydrogen (H_2) at 1000 °C for 2 min to desorb the thin surface oxide that was detrimental to the epitaxy process. The precursor for Ge is germane (GeH_4) diluted in hydrogen (H_2) to a concentration of 10%, and the carrier gas is H_2. The undoped Ge film was grown using the three-step approach, and the details can be found in the previous work [16]. In this approach, thermal cycling was introduced after the epitaxy growth process to enhance the surface mobility in an attempt to reduce the rms roughness and the TDD of the Ge film [9], [16]. The thermal cycling used in this study has a fixed lower bound temperature (T_L) of 680 °C, and the upper bound temperature (T_H) was varied from 725 °C to 825 °C in a step size of 25 °C. The sample was held at T_H for 10 min, and this annealing cycle was repeated eight times. No sample with $T_H \geq 850$ °C was prepared as the Ge film quality was greatly degraded due to excessive thermal budget [17].

Prior to surface treatment, the Ge/Si wafers were precleaned by dipping the sample into dilute HF (1:20) solution at room ambient, followed by six cycles of rinse and drain in deionized water, and subsequently dried by IPA. Three Ge/Si samples $(T_H = 825\ ^\circ\text{C})$ were used in the surface treatment study.

1) The first sample (sample 1) was precleaned for 300 s and immediately loaded into plasma-enhanced CVD (PECVD) chamber. The chamber was pretreated at 300 °C with plasma at 200 W. The GeO_xN_y was formed by setting the process pressure at 400 mTorr in the NH_3 environment, and the final thickness of GeO_xN_y was estimated to be ∼1.8 nm.
2) The second sample (sample 2) was identical to sample 1, except that the sample was first treated in UVO environment for 300 s. The sample was then loaded into the PECVD chamber for NH_3 plasma treatment, and the estimated thickness of GeO_xN_y was ∼2.5 nm.
3) In the third sample (sample 3), a thin GeO_2 layer of ∼2.8 nm was grown between 400 °C and 450 °C for 10 min on the Ge surface using dry oxidation and then loaded into PECVD chamber for NH_3 plasma treatment to form GeO_xN_y, and a thickness of 3.3 nm was obtained.

The leakage current of the aforementioned three samples was measured directly by STM of RHK Technology UHV 3500. To fabricate the MOS capacitors, the surface treatment described in sample 2 was used (the choice of this sample will be apparent and is discussed in the next section). After that, a high-k dielectric (Al_2O_3) with a thickness of 10 nm was deposited by atomic layer deposition at a temperature of 250 °C. Finally, titanium nitride (TiN) of 150 nm was sputtered onto the Al_2O_3 to form the metal contact. These samples were then patterned and etched to form a metal gate contact for electrical characterization. The size of these metal pads ranges from the largest pad of 200 μm × 200 μm to the smallest pad of 50 μm × 50 μm. Finally, the samples underwent a postmetal gate deposition forming gas annealing at 300 °C for 30 min. The schematic of the final MOS capacitor (MOSCAP) is shown in Fig. 1. The MOSCAP samples were fabricated on undoped Ge epitaxial films that were processed at different postgrowth thermal cycling temperatures (from T_L to various T_H).

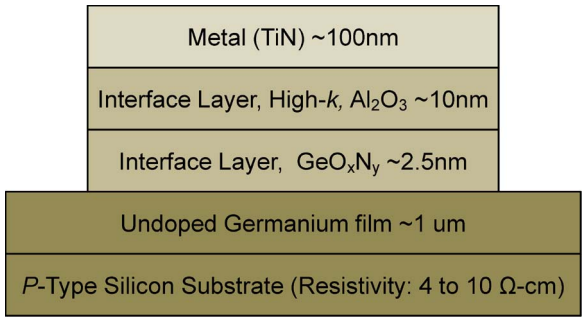


Fig. 1. Schematic of the final MOS capacitor used in this study.

Transmission electron microscopy (TEM) was used to study the layers in the stack of $TiN/Al_2O_3/GeO_xN_y/Ge/Si$ and also to estimate the thickness of each layer. Both capacitance–voltage (C–V) and current–voltage (I–V) measurements were performed on the MOSCAP using the Cascade/Suss Microtec PM8PS probe station with Keithley 4200-SCS semiconductor characterization system. The C–V curve gives direct information about the penetration of the field in the semiconductor (minimum in accumulation, maximum in depletion, etc.) and the related varying charges (majority and/or minority carriers), hence allowing a direct assessment of the field effect. The C–V characteristic of the MOSCAP has been widely used to characterize the semiconductor, oxide, and $Si-SiO_2$ interface [18]. The interfaced state density $(D_{\rm it})$ can be determined using the conductance method [15], and its value can be expressed as

$$D_{\rm it} \approx \frac{2.5}{q}\left(\frac{Gp}{\omega}\right)_{\rm max} \tag{1}$$

where $q = 1.602 \times 10^{-19}$ and $(G_p/\omega)_{\rm max}$ is the measured maximum conductance, and its expression will be defined next. In this paper, the capacitance meter assumes that the device consists of a parallel $C_m - G_m$ equivalent circuit. Assuming that the series resistance is negligible, the equation of G_p/ω can be written as

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{\rm ox}^2}{G_m^2 + \omega^2(C_{\rm ox} - C_m)^2} \tag{2}$$

where G_m is the measured conductance, $C_{\rm ox}$ is the oxide capacitance, and C_m is the measured capacitance.

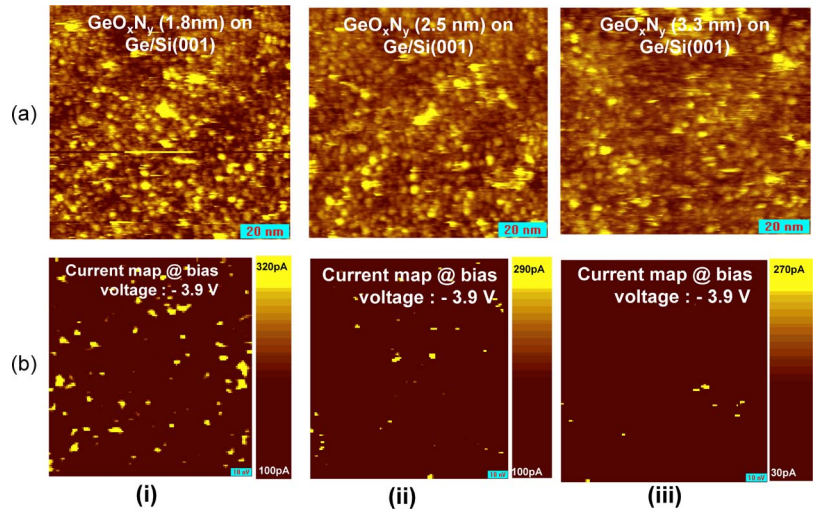


Fig. 2. (Column a) Scanning tunneling microscope images and their (column b) respective current mappings for (i) sample 1—GeO_xN_y (1.8 nm) on Ge/Si (001), (ii) sample 2—GeO_xN_y (2.5 nm) on Ge/Si(001), and (iii) sample 3—GeO_xN_y (3.3 nm) on Ge/Si(001).

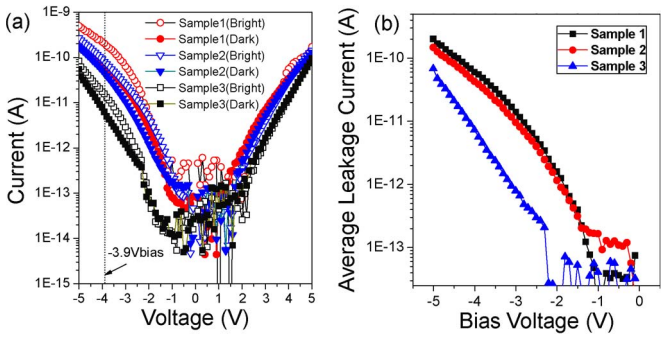


Fig. 3. Combined I–V plots and average leakage current for the three samples are shown in (a) and (b), respectively.

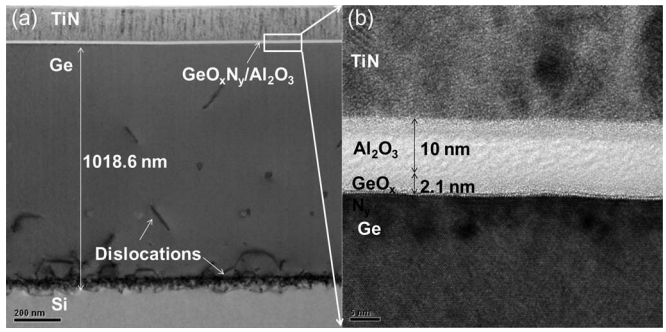


Fig. 4. Cross-sectional TEM bright field images show (a) the gate stack of $TiN/Al_2O_3/GeO_xN_y/Ge/Si$ and (b) the close-up view of $TiN/Al_2O_3/GeO_xN_y/Ge$. The Ge epitaxial film is prepared with a postgrowth thermal cycling temperature of 825 °C.

III. Results and Discussion

Fig. 2(a) shows the constant-current STM topography images of samples 1, 2, and 3, respectively. During topography scanning, a positive bias voltage was applied to the substrate of the samples, and the preset tunneling current was held constant by an electronic feedback circuit. Since the tunneling current was controlled by the vacuum gap between the STM probe and the dielectric surface, a change in the vacuum gap, due to surface roughness/electronic variation when the probe was scanned across the dielectric surface, gives rise to the contrast in the topography image [19], [20]. The bright shades correspond to locations where the STM probe retracts due to surface physical protrusions or a local increase in I_t due to electronic traps, in order to maintain constant tunneling current. The morphology and electronic effects can be distinguished via reference to the corresponding current map [Fig. 2(b)] acquired via constant imaging tunneling spectroscopy (CITS). During topography scanning, the feedback loop was temporarily disabled to allow the local current–voltage (I_t–V_s) characteristic of the dielectric to be measured by applying a voltage ramp [19]. An amorphous structure with rms roughness values of approximately 275, 271, and 280 pm is observed for samples 1, 2, and 3, respectively [Fig. 2(a)(i)–(a)(iii)]. It should be mentioned that the rms value does not reflect the real dielectric physical surface roughness

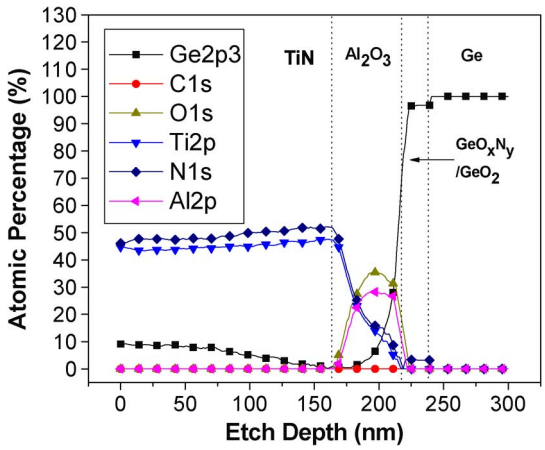


Fig. 5. XPS depth profile shows the distribution of Ge, C, O,Ti, N, and Al along the $TiN/Al_2O_3/GeO_xN_y/Ge$ gate stack. The artificial Ge signal in the TiN is most likely due to the larger X-ray spot size than the TiN pattern which results in the detection of background Ge signal.

since a local leakage site may induce the probe retraction too. The corresponding current map for sample 1 [Fig. 2(b)(i)] shows numerous scattered bright shades within the dark background. The bright shades represent the high-current-leakage sites, while the dark regions represent the least current leakage

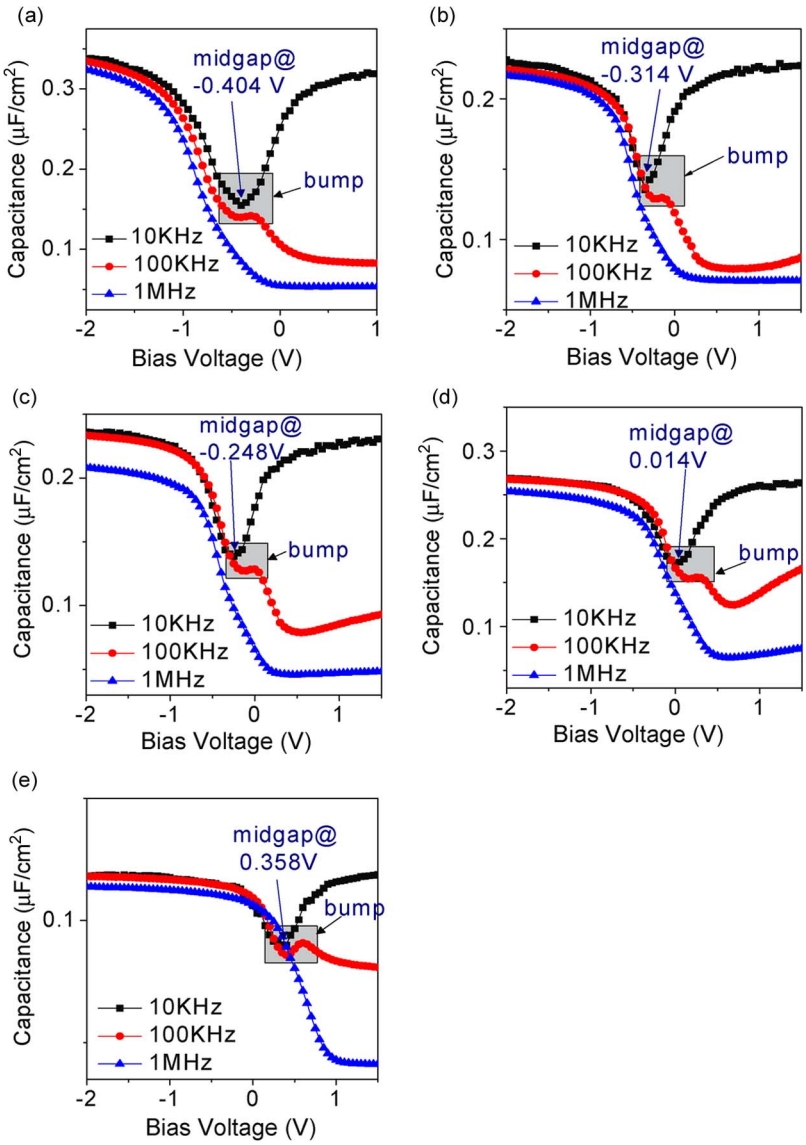


Fig. 6. C–V characteristics of MOSCAPs for (a) sample725 ($T_H = 725\ ^\circ$C), (b) sample750 ($T_H = 750\ ^\circ$C), (c) sample775 ($T_H = 775\ ^\circ$C), (d) sample800 ($T_H = 800\ ^\circ$C), and (e) sample825 ($T_H = 825\ ^\circ$C). The measurements are collected at frequencies and bias voltages ranging from 10 kHz to 1 MHz and -2 to 1.5 V, respectively.

sites. A decrease in the number of bright shades is observed in the current map for sample 2, as shown in Fig. 2(b)(ii). Sample 3, on the other hand, exhibits the lowest density of bright shades in the corresponding current map [Fig. 2(b)(iii)]. The tunneling spectra extracted at the bright shades of respective samples are shown in Fig. 3(a). The tunneling spectra are observed to converge at $V_s = 5$ V due to the normalization. Since electron is most sensitive to the barrier height at the interface of electron injection [20], the tunneling current at negative bias regime represents the electrical state at GeO_xN_y/Ge/Si substrate interface. It is noted that sample 1, with the thinnest GeO_xN_y, has the highest leakage current, while sample 3, with the thickest GeO_xN_y, shows the least leakage current. The leakage current averaged over the scan area of 100 nm $\times$ 100 nm shows a similar observation [Fig. 3(b)].

These results show that sample 2 with an additional UVO treatment prior to GeO_xN_y formation has a lower leakage current than sample 1 because of the formation of thicker interface layer and lower rms roughness. Sample 3 with GeO_2 deposition prior to NH_3 plasma exposure has the thickest interface layer and highest rms roughness, and hence, the lowest current leakage is expected. The drawback of fabricating sample 3 is the long processing time in the furnace, and the thickness of ultrathin oxide is uncontrollable. Hence, for subsequent MOSCAP fabrication, the method described in sample 2 is used. UVO is attractive as it is nontoxic, and the process is carried out in nonvacuum room ambient.

The cross-sectional bright field TEM image in Fig. 4(a) shows that the Ge epitaxial film annealed at a T_H of 825 °C has a thickness of $\sim 1\ \mu$m. The TEM also shows the presence of misfit dislocations closer to the Ge/Si interface, and threading dislocations in the film are clearly seen. The close-up TEM image in Fig. 4(b) shows that GeO_xN_y with a thickness of $\sim$2 nm is formed prior to $\sim$10 nm of Al_2O_3 deposition. As shown in Fig. 4(b), there is no delamination of the films at the interface between GeO_xN_y/Ge and Al_2O_3/GeO_xN_y,

because the surface treatment has provided a suitable surface for dielectric layer deposition. The XPS depth profile of each element from the top surface of the sample from Fig. 4 is shown in Fig. 5. The etch depth is relative as it is calibrated to the etch rate of SiO_2 under the bombardment of Ar ion. Nevertheless, the chemical composition of each layer corresponds to that of the fabricated $TiN/Al_2O_3/GeO_xN_y/Ge$ gate stack. There is no evidence of severe intermixing, hence verifying that the process steps are within the allowable thermal budget.

The C–V characteristics of the MOSCAP for frequency ranging from 10 kHz to 1 MHz for sample725 ($T_H = 725$ °C), sample750 ($T_H = 750$ °C), sample775 ($T_H = 775$ °C), sample800 ($T_H = 800$ °C), and sample825 ($T_H = 825$ °C) are summarized in Fig. 6(a)–(e), respectively. Even though the Ge layer is not intentionally doped during epitaxial growth, a p-type behavior is clearly seen. This observation is a result of background doping due to the residual boron in the CVD reactor. In addition, the valence band offset between Ge and Si favors hole accumulation in the Ge layer. At low frequency (LF), between 10 and 100 kHz, bumps are clearly observed in the C–V plots due to weak inversion of minority carrier response behavior [11], [21], [22]. Ge is a low-bandgap semiconductor, and at low frequencies, Ge/Si MOSCAP would show an admittance contribution due to the presence of interface traps at the midbandgap. This contribution results in a significant exchange of carriers between traps and both the majority and minority carrier bands at the measured frequencies, typically within the range of 1 kHz–1 MHz [11]. This exchange of carriers results in an increase in the capacitance as weak inversion response that causes the typical bump in the LF C–V. At a high frequency (HF) of 1 MHz, frequency dispersion is observed for all the samples, and the measured accumulation capacitance ($C_{\rm ox}$) is lower than that at LF. Since the semiconductor layer consists of an undoped Ge film on a p-type silicon substrate (resistivity of 4–10 $\Omega \cdot$ cm), the carriers in the undoped Ge film might be unable to follow the frequency of the bias voltage even at accumulation. Another possibility may be due to the dislocations introduced along the Ge/Si interface during the Ge epitaxial growth [16] as these could form interface traps along the dielectric/Ge and Ge/Si interfaces that leads to the slow response in the HF and affects the measured capacitance.

As T_H increases from 725 °C to 825 °C, the C–V curves exhibit a progressive shift to the right. The midgap voltage ($V_{\rm midgap}$) becomes more positive from −0.41 to 0.36 V (as indicated on the 10-kHz C–V curve), and correspondingly, the flatband voltage ($V_{\rm FB}$) increases from −0.75 to 0.25 V. As shown in Fig. 7, both the $V_{\rm FB}$ and $V_{\rm midgap}$ are proportionally dependent on T_H. Since the Ge thickness is not a strong factor contributing to the changes in $V_{\rm FB}$ [22] and the MOSCAP fabrication conditions are identical in all samples, the shift is most likely caused by the change in T_H which plays a significant role in the density of TDD in the final Ge film. As T_H increases, a better dielectric/Ge interface with a lower fixed charge is obtained, and this is reflected in the $V_{\rm FB}$ shift.

The G_p/ω value is plotted as a function of frequency f in Fig. 8 for all T_H values used in this experiment. The plots show distinct peak values at around ∼20 kHz, which agree with previously reported observation [23]. Based on these peak values, the interface state density $D_{\rm it}$ is obtained using (1) for all samples annealed at T_H between 725 °C and 825 °C. The TDD and $D_{\rm it}$ values are summarized for all T_H values in Fig. 9. The TDD values are obtained from optical microscope observation after chemical etching on the Ge samples as described in [16]. Higher annealing temperature is often used to reduce the Ge surface roughness and TDD after epitaxial growth. As clearly shown, lower TDD in the Ge film results in lower $D_{\rm it}$ in the MOSCAP.

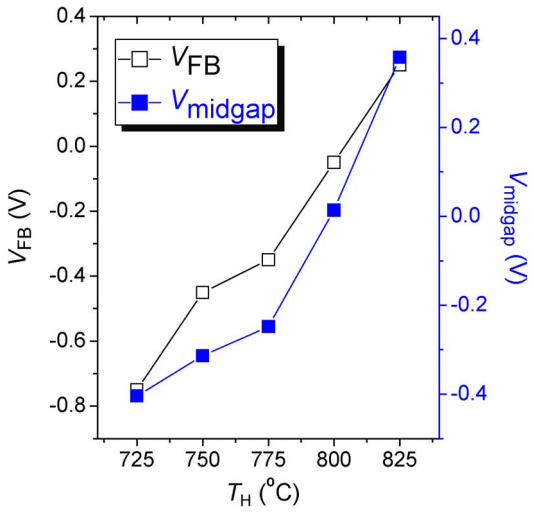


Fig. 7. $V_{\rm FB}$ and $V_{\rm midgap}$ for different T_H values. As shown, both $V_{\rm FB}$ and $V_{\rm midgap}$ vary linearly with T_H.

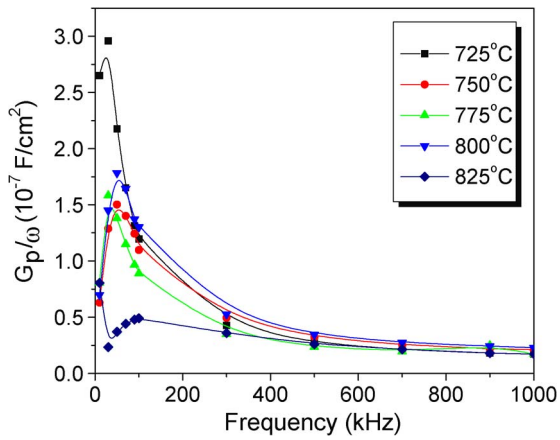


Fig. 8. G_p/ω versus f characteristic is shown for different T_H values.

Fig. 10 shows the combined leakage current density versus the bias voltage of the Ge/Si MOSCAP for bias voltage ranging from −2 to 2 V. The leakage current is reduced when the T_H is increased and the lowest value is realized at 825 °C in the experiment. A reduction of close to five orders of magnitude (10^5) in the leakage current can be observed by comparing sample725 and sample800 at −2 V. These results confirm that the MOSCAP on the Ge epitaxial film annealed at higher thermal cycling temperature presents lower leakage current. This is again attributed to the lower TDD count in the Ge film as the annealing temperature is increased. Higher TDD is often known to lead to higher current leakage [24] and could cause malfunction to the devices. Another possibility is due to

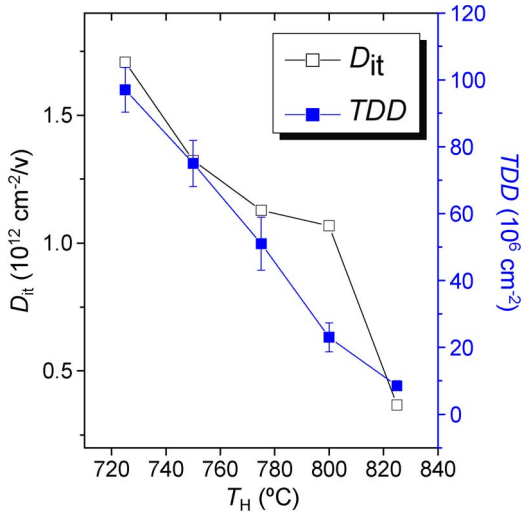


Fig. 9. Relationship of $D_{\rm it}$ and TDD with respect to T_H. As shown, $D_{\rm it}$ and TDD can be greatly reduced at high T_H.

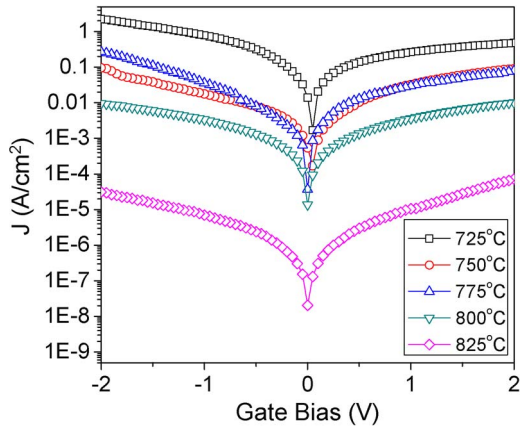


Fig. 10. I–V plots for Ge/Si MOSCAPs for Ge growth with thermal cycling from 725 °C to 825 °C.

the slight difference in the EOT. It appears that the dielectric thickness gets thicker from sample725 to sample825 in Fig. 6. Ideally, all the Ge samples should have identical EOT as they were prepared and deposited at the same time. However, due to the surface conditions (such as roughness and TDD) of the respective Ge film, the GeO_xN_y formation tends to get better (hence, thicker) from sample725 to sample825. Hence, sample825 with a slightly thicker dielectric appears to have a lower maximum capacitance than the other samples.

IV. Conclusion

In summary, the electrical properties (from MOS analysis) of Ge epitaxial film are significantly affected by the postgrowth thermal cycling temperature. The Ge film treated with UVO and subsequent GeO_xN_y nitridation has shown a reasonable leakage current. The MOSCAP fabricated on the Ge film that is cyclic annealed at an upper bound temperature of 825 °C exhibits the lowest leakage current density of $\sim 2.3 \times 10^{-8}$ A/cm^2 (at -2 V), which is improved by five orders of magnitude (10^5) compared with the sample annealed at 725 °C, $D_{\rm it} \sim 3.5 \times 10^{11}$ cm^{-2}/V, and TDD $< 10^7$ cm^{-2}.

Acknowledgment

The authors would like to thank the management and technical staff in the Nanyang Nanofabrication Center, Nanyang Technological University.

References

[1] S. Deleonibus, "Physical and technological limitations of nanoCMOS devices to the end of the roadmap and beyond," *Eur. Phys. J. Appl. Phys.*, vol. 36, no. 3, pp. 197–214, Dec. 2006.
[2] The International Technology Roadmap for Semiconductor. [Online]. Available: www.itrs.net
[3] K. C. Saraswat, C. O. Chui, T. Krishnamohan, D. Kim, A. Nayfeh, and A. Pethe, "High performance germanium MOSFETs," *Mater. Sci. Eng. B*, vol. 135, no. 3, pp. 242–249, Dec. 2006.
[4] Y. Kamata, "High-*k*/Ge MOSFETs for future nanoelectronics," *Mater. Today*, vol. 11, no. 1/2, pp. 30–38, Jan./Feb. 2008.
[5] D. J. Hymes and J. J. Rosenberg, "Growth and materials characterization of native germanium oxynitride thin films on germanium," *J. Electrochem. Soc.*, vol. 135, no. 4, pp. 961–965, Apr. 1988.
[6] T. Maeda, M. Nishizawa, Y. Morita, and S. Takagi, "Role of germanium nitride interfacial layers in HfO_2/germanium nitride/germanium metal–insulator–semiconductor structures," *App. Phys. Lett.*, vol. 90, no. 7, p. 072911, Feb. 2007.
[7] H. Shang, M. M. Frank, F. P. Gusev, J. O. Chu, S. W. Bedell, K. W. Guarini, and M. Ieong, "Germanium channel (MOSFET)s: Opportunities and challenges," *IBM J. Res. Develop.*, vol. 50, no. 4/5, pp. 377–386, Jul. 2006.
[8] T. Maeda, T. Yasuda, M. Nishizawa, N. Miyata, Y. Morita, and S. Takagi, "Ge metal–insulator–semiconductor structures with Ge_3N_4 dielectrics by direct nitridation of Ge substrates," *Appl. Phys. Lett.*, vol. 85, no. 15, pp. 3181–3183, Oct. 2004.
[9] C. O. Chui, S. Ramanathan, B. B. Triplet, P. C. McIntyre, and K. C. Saraswat, "Germanium MOS capacitors incorporating ultrathin high-κ gate dielectric," *IEEE Electron Device Lett.*, vol. 23, no. 8, pp. 473–475, Aug. 2002.
[10] R. D. Clark, S. Consiglio, G. Nakamura, Y. Trickett, and G. J. Leusink, "Optimizing ALD HfO_2 for advanced gate stacks with interspersed UV and thermal treatments—DADA and MDMA variations, combinations and optimization," *ECS Trans.*, vol. 41, no. 2, pp. 79–88, Oct. 2011.
[11] K. Martens, C. O. Chui, G. Brammertz, B. D. Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, "On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 547–556, Feb. 2008.
[12] A. Nayfeh, C. O. Chui, K. C. Saraswat, and T. Yonehara, "Effects of hydrogen annealing on heteroepitaxial-Ge layers on Si: Surface roughness and electrical quality," *Appl. Phys. Lett.*, vol. 85, no. 14, pp. 2815–2817, Oct. 2004.
[13] Q. Xie, J. Musschoot, M. Schaekers, M. Caymax, A. Delabie, X. Qu, Y. Jiang, S. V. D. Berghe, J. Liu, and C. Detavernier, "Ultranthin GeO_xN_y interlayer formed by *in situ* NH_3 plasma pretreatment for passivation of germanium metal–oxide–semiconductor devices," *Appl. Phys. Lett.*, vol. 97, no. 22, p. 222 902, Nov. 2010.
[14] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, "Suppression of ALD-induced degradation of Ge MOS interface properties by low power plasma nitridation of GeO_2," *J. Electrochem. Soc.*, vol. 158, no. 8, pp. G178–G184, 2011.
[15] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley, 1982, pp. 212–220.
[16] Y. H. Tan and C. S. Tan, "Growth and characterization of germanium epitaxial film on silicon (001) using reduced pressure chemical vapor deposition," *Thin Solid Films*, vol. 520, no. 7, pp. 2711–2716, Feb. 2012.
[17] M. Gavelle, E. M. Bazizi, E. Scheld, P. F. Fazzini, F. Cristiano, C. Armand, W. Lerch, S. Paul, Y. Campidelli, and A. Halimaoui, "Detailed investigation of Ge–Si interdiffusion in the full range of $Si_{1-x}Ge_x (0 \leq x \leq 1)$ composition," *J. Appl. Phys.*, vol. 104, no. 11, p. 113 524, Dec. 2008.
[18] J. Tao, C. Z. Zhao, C. Zhao, P. Taechakumput, M. Werner, S. Taylor, and P. R. Chalker, "Extrinsic and intrinsic frequency dispersion of high-*k* materials in capacitance–voltage measurements," *Materials*, vol. 5, no. 6, pp. 1005–1032, Jun. 2012.
[19] K. S. Yew, D. S. Ang, L. J. Tang, K. Cui, G. Bersuker, and P. S. Lysaght, "Scanning tunneling microscopy study of the multi-step deposited and annealed $HfSiO_x$ gate dielectric," *J. Electrochem. Soc.*, vol. 158, no. 10, pp. H1 021–H1 021, Aug. 2011.

[20] Y. C. Ong, D. S. Ang, K. L. Pey, Z. R. Wang, S. J. O'Shea, C. H. Tung, T. Kawanago, K. Kakushima, and H. Iwai, "Electrical trap characterization of the Sc_2O_3/La_2O_3 high-k gate stack by scanning tunneling microscopy," *Appl. Phys. Lett.*, vol. 92, no. 2, p. 022904, Jan. 2008.
[21] C. C. Cheng, C. H. Chien, G. L. Luo, Y. T. Ling, R. D. Chang, C. C. Kei, C. N. Hsiao, J. C. Liu, and C. Y. Chang, "Effects of minority-carrier response behavior on Ge MOS capacitor characteristics: Experimental measurements and theoretical simulations," *IEEE Trans. Electron Devices*, vol. 56, no. 5, pp. 1118–1127, May 2009.
[22] Y. H. Wu, M. L. Wu, J. R. Wu, and Y. S. Lin, "Electrical characteristics of Ge MOS device on Si substrate with thermal SiON as gate dielectric," *Microelectron. Eng.*, vol. 87, no. 11, pp. 2423–2428, Nov. 2010.
[23] D. S. L. Mui, Z. Wang, and H. Morkoc, "A review of III–V semiconductor based metal–insulator–semiconductor structures and devices," *Thin Solid Films*, vol. 231, no. 1/2, pp. 107–124, Aug. 1993.
[24] H. C. Luan, D. R. Lim, K. K. Lee, K. M. Chen, J. G. Sandland, K. Wada, and L. C. Kimerling, "High-quality Ge epilayers on Si with low threading dislocation densities," *Appl. Phys. Lett.*, vol. 75, no. 19, pp. 2909–2911, Nov. 1999.

Yew Heng Tan is currently working toward the Ph.D. degree in the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), Singapore.

In 2001, he joined NTU as a Senior Engineer.

Kwang Sing Yew received the B.Eng. (Hons) degree from the University of Technology Malaysia, Johor Bahru, Malaysia, in 2007. He is currently working toward the Ph.D. degree at Nanyang Technological University, Singapore.

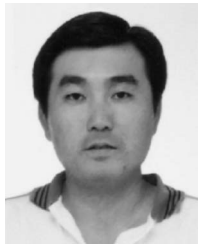
Kwang Hong Lee received the Ph.D. degree in materials science and engineering from Nanyang Technological University, Singapore.

He is currently a Postdoctoral Associate with the Singapore–MIT Alliance for Research and Technology, Singapore.

Yao-Jen Chang received the B.S. degree from Tamkang University, Taipei, Taiwan, in 2008. He is currently working toward the Ph.D. degree in the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan.

Kuan-Neng Chen (M'05–SM'11) received the Ph.D. degree from Massachusetts Institute of Technology, Cambridge.

He is currently a Professor with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan.



Diing Shenp Ang (M'98–SM'08) received the B.Eng. (Hons) and Ph.D. degrees from the National University of Singapore, Singapore.

Since April 2008, he has been an Associate Professor with Nanyang Technological University, Singapore.

Eugene A. Fitzgerald received the Ph.D. degree in materials science and engineering from Cornell University, Ithaca, NY, in 1989.

He is a Lead Principal Investigator with the Singapore–MIT Alliance for Research and Technology, Singapore.

Chuan Seng Tan (S'00–M'07) received the Ph.D. degree in electrical engineering from Massachusetts Institute of Technology, Cambridge, in 2006.

In 2006, he joined Nanyang Technological University, Singapore.