Dependence of Read Margin on Pull-Up Schemes in High-Density One Selector–One Resistor Crossbar Array

Chun-Li Lo, Tuo-Hung Hou, Mei-Chin Chen, and Jiun-Jia Huang

***Abstract*—This paper reports on comprehensive analytical and numerical circuit analyses on the read margin of the one selector–one resistor (1S1R) resistive-switching crossbar array. These analyses are based on the experimental characteristics of the 1S1R cells and provide a valuable insight into their potential for ultrahigh-density data storage. Three read schemes, namely, one bit-line pull-up (One-BLPU), all bit-line pull-up (All-BLPU), and partial bit-line pull-up (Partial-BLPU), are investigated. In contrast to the One-BLPU scheme, the All-BLPU scheme can realize a large crossbar array of 16 Mb, even when the line resistance is nonnegligible because the effective resistance at the sneak current path is substantially less sensitive to the array size. Additionally, the Partial-BLPU scheme can be used to reduce power consumption if random read access is desirable. Finally, the effects of line resistance on the read and write margins are discussed.**

***Index Terms*—Crossbar array, one selector–one resistor (1S1R), read margin, resistive random access memory (RRAM), resistive switching (RS), sneak current.**

I. Introduction

RESISTIVE-SWITCHING (RS) random access memory (RRAM) is regarded as the most promising candidate for the next-generation nonvolatile memories, not only because of its low power consumption, high speed, and excellent reliability but also because of its ultimate scaling potential for crossbar array architectures. However, undesirable sneak current can arise from nearby unselected cells, diminishing read margins and limiting the maximum size of the crossbar array [1]. In unipolar RRAM, this problem is mitigated by connecting a diode in series as a selection device, namely, one diode–one resistor cell [2]–[5]. However, the unipolar conduction of diodes is inapplicable to bipolar RRAM, which is inherently more stable. Complementary RS (CRS) has been proposed by connecting two bipolar RS elements in anti-series to suppress the sneak current [6]–[9], although CRS features a destructive read problem. Recently, a cell structure that comprises one nonlinear bipolar selector and one bipolar RS element [one selector–one resistor (1S1R)] has been proposed [10]–[12]. The maximum size of a single crossbar array with at least a 10% read margin was estimated to be 10 Mb using a conventional one bit-line pull-up (One-BLPU) scheme [11], [12]. However, this estimation may be too optimistic without considering line resistance, which is nonnegligible for large crossbar arrays. Furthermore, read margin improvements have been reported using an all bit-line pull-up (All-BLPU) scheme in a crossbar array with linear [1] and nonlinear [13] cell resistances, suggesting that optimization of the read scheme may play a crucial role in the read margins of crossbar 1S1R arrays with highly nonlinear cell resistance. However, in contrast to the analytical circuit analysis used in [1], [11], and [12], only numerical circuit analysis can predict the read margin using All-BLPU in the 1S1R crossbar array because of the implicit relationship between voltage and nonlinear resistance.

This paper performs comprehensive circuit analyses of a 1S1R RS crossbar array using both analytical solutions and numerical SPICE simulations to investigate the merits of various read pull-up schemes. Additionally, the potential of high-density 1S1R crossbar array based on experimental device characteristics is addressed. The remainder of this paper is organized as follows. Section II describes the modeling framework used to analyze the read margin in the crossbar array using numerical SPICE simulations. The device characteristics of the $Ni/TiO_2/Ni/HfO_2/Pt$ 1S1R cell in [11] were fitted in SPICE using two back-to-back Schottky diodes in series with a variable resistor. To simplify the analyses of various read schemes, the line resistance is first ignored. Section III introduces the analytical and numerical circuit analyses of the linear crossbar arrays using One-BLPU and All-BLPU. Section IV further extends the analyses to nonlinear crossbar arrays using the modeled 1S1R cell proposed in Section II. Although it is unable to yield explicit solutions in the nonlinear array, the complete analytical circuit analysis conducted in this study intuitively elaborates the advantages of All-BLPU. Section V presents a discussion on practical considerations regarding the All-BLPU 1S1R crossbar array, including the optimization of the pull-up conditions. Furthermore, a partial bit-line pull-up (Partial-BLPU) scheme is proposed to optimize the power consumption for random read access. Section VI includes the effects of line resistance to evaluate the potential of high-density 1S1R crossbar arrays using All-BLPU. The experimental 1S1R cell demonstrates its capability of realizing a 16-Mb crossbar array with at least a

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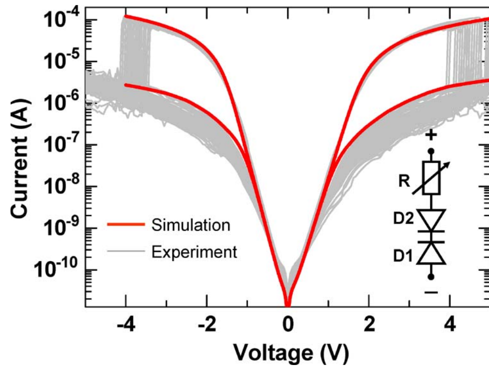

Fig. 1. Experimental and simulated I–V curves of the 1S1R cell in [11]. An equivalent circuit model of two back-to-back Schottky diodes D1 and D2 in series with a variable resistor R is used to reproduce the device characteristics. The saturation current, series resistance, and ideality factor at the reverse bias are 10^{-11} A, 10 kΩ, and 4, respectively, for D1 and 10^{-11} A, 1 kΩ, and 3.2, respectively, for D2.

10% read margin and good immunity to write disturb, which holds promise for future ultrahigh-density storage.

II. Model of RRAM Cell and Crossbar Array

The nonlinear resistance of the Ni/TiO_2/Ni bipolar selector is attributed to the Schottky barriers at the Ni/TiO_2 interfaces [11]. Two Schottky diodes connected in anti-series were used in SPICE to reproduce the nonlinear current–voltage (I–V) characteristics that were dominated by the diode reverse-biased current. The diode parameters of the saturation current, ideality factor at the reverse bias, and series resistance were adjusted in the two Schottky diodes separately to obtain the best fit for the experimental I–V. Furthermore, the Ni/HfO_2/Pt RS element was modeled using a variable resistor with a linear low-resistance-state (LRS) resistance ($R_{\rm LRS}$) of 15 kΩ and a non-linear high-resistance-state (HRS) resistance ($R_{\rm HRS}$) ranging from 1 to 4 MΩ at various biases. A memory array comprising only the variable resistor cells (1R) in a crossbar configuration is a linear crossbar array because of the linear $R_{\rm LRS}$ in 1R. If the variable resistor is connected to the bipolar selector as a 1S1R cell, the LRS resistance becomes highly nonlinear. A crossbar memory array comprising the 1S1R cells is a nonlinear crossbar array.

Fig. 1 shows the measured and simulated I–V curves of the 1S1R cell. The simulated I–V curve at LRS was in excellent agreement with the experimental results. The nonlinear resistance is typically characterized by a nonlinearity factor α [11], [12], where $\alpha(1\ {\rm V}, 2\ {\rm V}) = R_{\rm LRS}(1\ {\rm V})/R_{\rm LRS}(2\ {\rm V}) = 188$ in the 1S1R cell shown in Fig. 1. The measured I–V at HRS showed considerable resistance variation. The I–V curve at HRS was fitted for the smallest resistance ratio ($R_{\rm HRS}/R_{\rm LRS}$), considering only the worst case scenario. The SPICE model used in this study did not attempt to reproduce the switching characteristics of RRAM. Investigating the read interference in the crossbar arrays only requires the accurate resistance values at HRS and LRS. Unless otherwise noted, the following array simulations used the resistance of the proposed 1R and 1S1R memory cells.

Fig. 2(a) shows an $N \times N$ crossbar RRAM array. To read the stored information at the selected bit using One-BLPU, a

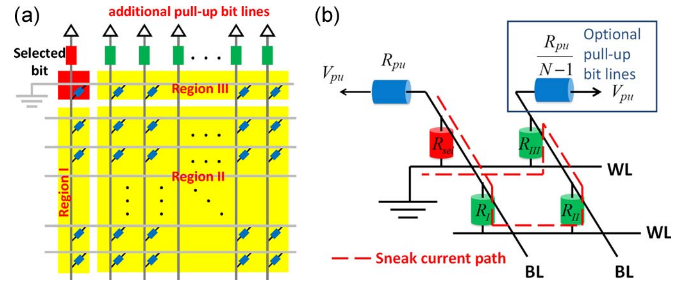

Fig. 2. (a) Schematic of an $N \times N$ crossbar RRAM array. Unselected bits at the sneak current path are divided into three regions. (b) Equivalent circuit of the crossbar array. R_I, $R_{\rm II}$, and $R_{\rm III}$ of the parallel resistor networks in Regions I, II, and III, respectively, are connected in series as the parasitic sneak current path when evaluating $R_{\rm sel}$.

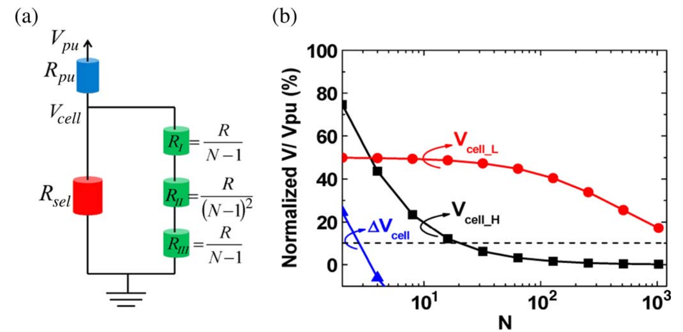

Fig. 3. (a) Equivalent circuit of the linear crossbar array using One-BLPU. (b) Simulation of normalized $V_{\rm cell}$ and $\Delta V_{\rm cell}$ when $R_{\rm sel} = R_{\rm HRS}$ and $R_{\rm sel} = R_{\rm LRS}$ as a function of the number of word (bit) lines N in the linear crossbar array using One-BLPU.

pull-up voltage ($V_{\rm pu}$) of 3 V was applied to the selected bit line while the selected word line was grounded. All unselected bit/word lines remained floating. The voltage on the pull-up resistor ($R_{\rm pu}$) that was connected to the selected bit line was evaluated, and the voltage swing (ΔV) when reading the selected bit resistance ($R_{\rm sel}$) equal to $R_{\rm HRS}$ and $R_{\rm LRS}$ should be higher than the sensitivity limit of the peripheral sensing circuit. In this paper, a read margin criterion with a minimum of 10% $\Delta V/V_{\rm pu}$ was used to determine the maximum crossbar array size [6]. Unless otherwise noted, $R_{\rm pu}$ was equal to $R_{\rm LRS}$ because this was typically close to the optimal pull-up resistance for the maximum read margin [1]. If the multiple or all bit lines are pulled up, these are Partial-BLPU or All-BLPU schemes. To facilitate the analysis in this study, the equivalent circuit of the crossbar array was represented by three resistor networks connected in series as the parasitic sneak current path when evaluating $R_{\rm sel}$, as shown in Fig. 2(b). R_I, $R_{\rm II}$, and $R_{\rm III}$ were the equivalent resistances of Regions I, II, and III, respectively, as shown in Fig. 2(a). This study only examined the worst case read scenario with a minimum read margin. The data patterns in Regions I, II, and III for the worst case scenario are addressed in the following section.

III. Pull-Up Scheme Analysis: Linear Crossbar Array

Fig. 3(a) shows the equivalent circuit of a linear crossbar array using One-BLPU. The cell voltages when the selected

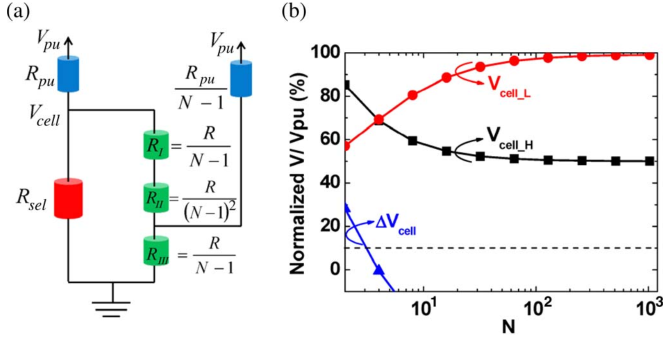

Fig. 4. (a) Equivalent circuit of the linear crossbar array using All-BLPU. (b) Simulation of normalized V_{cell} and ΔV_{cell} when $R_{\text{sel}} = R_{\text{HRS}}$ and $R_{\text{sel}} = R_{\text{LRS}}$ as a function of the number of word (bit) lines N in the linear crossbar array using All-BLPU.

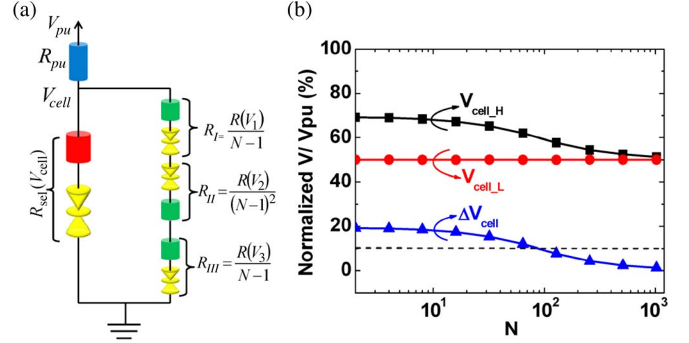

Fig. 5. (a) Equivalent circuit of the nonlinear 1S1R crossbar array using One-BLPU. (b) Simulation of normalized V_{cell} and ΔV_{cell} when $R_{\text{sel}} = R_{\text{HRS}}$ and $R_{\text{sel}} = R_{\text{LRS}}$ as a function of the number of word (bit) lines N in the nonlinear 1S1R crossbar array using One-BLPU. LRS nonlinearity factor $\alpha(1\ \text{V}, 2\ \text{V}) = 188$.

bit was at LRS and HRS are denoted as V_{cell_L} and V_{cell_H}, respectively. For the worse case read scenario, the minimum V_{cell_H} occurred when the effective resistance at the sneak current path (R_S) was at its lowest possible value (i.e., unselected bits were all at their LRS). The maximum V_{cell_L} occurred when R_S was at its highest possible value (i.e., unselected bits were all at their HRS) [1]. Therefore, R_S can be calculated analytically as

$$R_{\text{SL}_H}(m=1) = \frac{2R_{\text{LRS}}}{N-1} + \frac{R_{\text{LRS}}}{(N-1)^2} = R_{\text{LRS}}\frac{2N-1}{(N-1)^2} \quad (1)$$

$$R_{\text{SL}_L}(m=1) = \frac{2R_{\text{HRS}}}{N-1} + \frac{R_{\text{HRS}}}{(N-1)^2} = R_{\text{HRS}}\frac{2N-1}{(N-1)^2} \quad (2)$$

where the subscripts SL_H and SL_L indicate that only linear resistors exist at the sneak current path when $R_{\text{sel}} = R_{\text{HRS}}$ and R_{LRS}, respectively, and m is the number of pull-up bit lines. Because both R_{SL_L} and R_{SL_H} are approximately proportional to $1/N$, the degradation of V_{cell_H} is the chief concern in large arrays. This was confirmed by the numerical SPICE simulation shown in Fig. 3(b), in which V_{cell_H} was reduced rapidly as N increased. The read margin degraded to below 10% for $N = 3$, illustrating the severe sneak current effect.

Fig. 4(a) shows the equivalent circuit of a linear crossbar array using All-BLPU. The minimum V_{cell_H} still occurred when the unselected bits were all at their LRS, yielding the minimum R_S value for the worse case read scenario. However, in contrast to One-BLPU, negative R_S occurred in All-BLPU because of the additional voltage pull-up at the sneak current path. The negative $R_S = -R_{\text{LRS}}$ in parallel with $R_{\text{sel}} = R_{\text{LRS}}$ can significantly increase V_{cell_L} close to V_{pu}, which occurred when unselected bits in Regions I, II, and III were at their LRS, LRS, and HRS, respectively. For the aforementioned data patterns, R_S can be derived analytically from (A1) in the Appendix

$$R_{\text{SL}_H}(m=N) = \frac{R_{\text{HRS}}R_{\text{LRS}}}{R_{\text{HRS}} - R_{\text{LRS}}} \times \frac{N(N+1)}{(N-1)^2} \quad (3)$$

$$R_{\text{SL}_L}(m=N) = -\frac{R_{\text{HRS}}R_{\text{LRS}}}{R_{\text{HRS}} - R_{\text{LRS}}} \times \frac{N\left[N + \left(\frac{R_{\text{LRS}}}{R_{\text{HRS}}}\right)\right]}{(N-1)^2}. \quad (4)$$

R_{SL_H} has a substantially weaker dependence on N as compared with that in (1) and eventually converges to R_{LRS} if $R_{\text{HRS}} \gg R_{\text{LRS}}$. This weaker dependence is understood analogically by suppressing the current flowing through R_I and R_{II} because of the increased V_3 attained using additional pull-up. Therefore, V_{cell_H} decreases more slowly than it does in One-BLPU as N increases. However, negative R_{SL_L} converges to $-R_{\text{LRS}}$ if $R_{\text{HRS}} \gg R_{\text{LRS}}$, increasing V_{cell_L} and degrading the read margin. Therefore, All-BLPU may not efficiently improve the read margin in linear crossbar arrays, as shown by the SPICE simulation displayed in Fig. 4(b). This result contradicts that in [1] because of the actual worst case data patterns considered in this study.

IV. Pull-Up Scheme Analysis: 1S1R Nonlinear Crossbar Array

Nonlinear elements with resistance as a function of voltage increase R_S [13]–[16]. Fig. 5(a) shows the equivalent circuit of a 1S1R nonlinear crossbar array using One-BLPU. Similar to (1) and (2), R_S can be calculated as

$$R_{\text{SNL}_H}(m=1) = \frac{R_{\text{LRS}}(V_1)}{N-1} + \frac{R_{\text{LRS}}(V_2)}{(N-1)^2} + \frac{R_{\text{LRS}}(V_3)}{N-1} \quad (5)$$

$$R_{\text{SNL}_L}(m=1) = \frac{R_{\text{HRS}}(V_1)}{N-1} + \frac{R_{\text{HRS}}(V_2)}{(N-1)^2} + \frac{R_{\text{HRS}}(V_3)}{N-1} \quad (6)$$

where the subscripts SNL_H and SNL_L indicate that nonlinear resistors exist at the sneak current path when $R_{\text{sel}} = R_{\text{HRS}}$ and R_{LRS}, respectively. V_1, V_2, and V_3 are the implicit functions of the voltage on the unselected bits at Regions I, II,

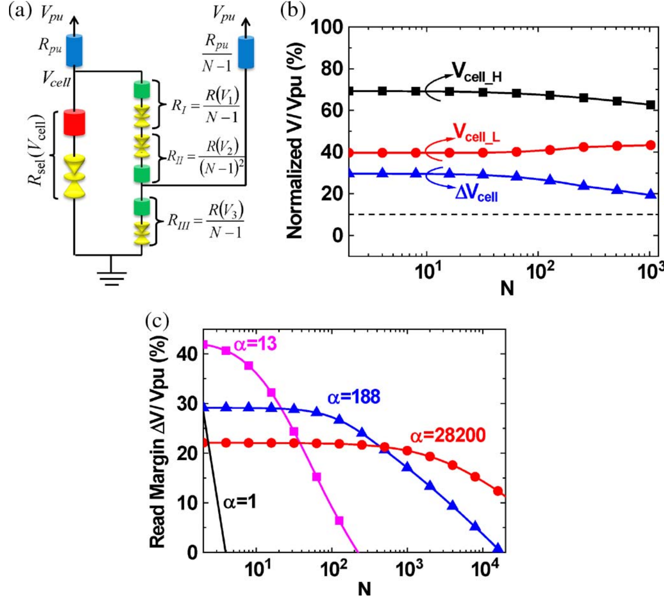

Fig. 6. (a) Equivalent circuit of the nonlinear 1S1R crossbar array using All-BLPU. (b) Simulation of normalized V_{cell} and ΔV_{cell} when $R_{\text{sel}} = R_{\text{HRS}}$ and $R_{\text{sel}} = R_{\text{LRS}}$ as a function of the number of word (bit) lines N in the nonlinear 1S1R crossbar array using All-BLPU. LRS nonlinearity factor $\alpha(1\text{ V}, 2\text{ V}) = 188$. (c) Read margin simulation of the nonlinear 1S1R crossbar array with various $\alpha(1\text{ V}, 2\text{ V})$ as a function of the number of word (bit) lines N.

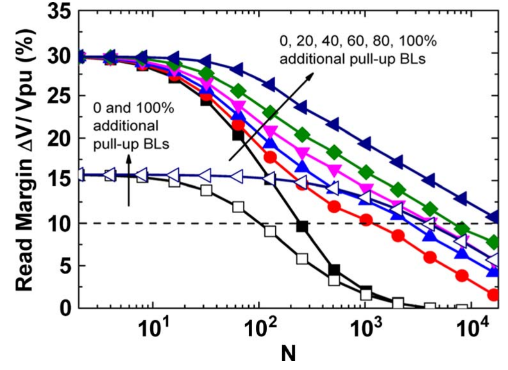

Fig. 7. Worst case read margin simulation of the nonlinear 1S1R crossbar array with various percentages of additional pull-up lines as a function of the number of word (bit) lines N using (hollow) $V_{\text{pu}} = 2$ V and (solid) $V_{\text{pu}} = 3$ V. The 0%, 20%–80%, and 100% additional pull-up BLs represent One-BLPU, Partial-BLPU, and All-BLPU, respectively. The optimal R_{pu} value for each array size is determined numerically to maximize the read margin.

and III, respectively. Because of the nonlinear resistance and because V_1, V_2, and V_3 were all less than V_{cell}, R_{SNL_H} in (5) was much greater than R_{SL_H} in (1). The SPICE simulation shown in Fig. 5(b) confirmed that there was a larger read margin compared to that of the linear crossbar array shown in Fig. 3(b) or Fig. 4(b).

To further enhance the read margin, All-BLPU was used to increase R_{SNL} in this study. Fig. 6(a) shows the equivalent circuit of a 1S1R nonlinear crossbar array using All-BLPU. Using the similar data patterns in (3) and (4), R_{SNL} can be derived from (A1) in the Appendix as (7) and (8), shown at the bottom of the page, where $\alpha(V_1, V_3) = R_{\text{LRS}}(V_1)/R_{\text{LRS}}(V_3)$, $\alpha(V_2, V_3) = R_{\text{LRS}}(V_2)/R_{\text{LRS}}(V_3)$, and $k_3 = R_{\text{HRS}}(V_3)/R_{\text{LRS}}(V_3)$. V_1, V_2, and V_3 are implicit functions with values that can only be accurately determined using numerical simulations. In addition, (7) and (8) can be reduced to (3) and (4), respectively, for a linear crossbar array with $\alpha(V_1, V_3) = \alpha(V_2, V_3) = 1$. Furthermore, because of the additional pull-up bit lines, V_3 was significantly larger than V_1 and V_2. When $\alpha \gg 1$ in a nonlinear crossbar array, $|R_{\text{SNL}}|$ in (7) and (8) was significantly larger than $|R_{\text{SL}}|$ in (3) and (4). Therefore, the read margin was efficiently enhanced in All-BLPU using 1S1R cells. The SPICE simulation shown in Fig. 6(b) confirmed the significant enhancements of the read margin by combining the 1S1R nonlinear crossbar array and All-BLPU, which was in good agreement with the analytical analysis. Fig. 6(c) shows the influence of α on the calculated read margin. Various α values were modeled choosing appropriate fitting factors of the nonlinear selector. A larger α enhanced read margin at large N, as predicted in (7) and (8). When N was small, the smaller read margin with larger α was caused by the smaller $R_{\text{HRS}}/R_{\text{LRS}}$ ratio at V_{pu} that was used in the simulation. The read margin at small N was determined by the $R_{\text{HRS}}/R_{\text{LRS}}$ ratio at the selected bit rather than R_S because of the negligible sneak current.

V. Additional Practical Considerations and Partial-BLPU

The analyses in Sections III and IV clearly elucidate the advantages of the 1S1R nonlinear crossbar array and the All-BLPU read scheme. This section further addresses additional practical considerations of the read margin analysis, including the selection of V_{pu} and R_{pu}, and an alternative Partial-BLPU scheme.

The selection of a V_{pu} value can affect α and, therefore, the read margin. In theory, an optimized V_{pu} can be determined numerically according to the nonlinear characteristic of the 1S1R cell. However, the upper bound of V_{pu} must prevent any bit from read disturb during a potential full V_{pu} drop. Therefore, V_{pu} should not be greater than 4 V according to the switching voltages shown in Fig. 1. Fig. 7 shows the comparison of the read margins using $V_{\text{pu}} = 2$ and 3 V. Furthermore, rather than using a fixed R_{pu}, the optimal value of R_{pu} for each array size can be chosen numerically to maximize the read margin.

$$R_{\text{SNL}_H}(m = N) = \frac{R_{\text{HRS}}(V_{\text{cell}})R_{\text{LRS}}(V_3)}{R_{\text{HRS}}(V_{\text{cell}}) - R_{\text{LRS}}(V_3)} \times \frac{N(N-1) + 2(N-1)\alpha(V_1, V_3) + 2\alpha(V_2, V_3)}{(N-1)^2} \tag{7}$$

$$R_{\text{SNL}_L}(m = N) = -\frac{R_{\text{HRS}}(V_3)R_{\text{LRS}}(V_{\text{cell}})}{R_{\text{HRS}}(V_3) - R_{\text{LRS}}(V_{\text{cell}})} \times \frac{N(N-1) + (N-1)\alpha(V_1, V_3)\left(k_3^{-1} + 1\right) + \alpha(V_2, V_3)\left(k_3^{-1} + 1\right)}{(N-1)^2} \tag{8}$$

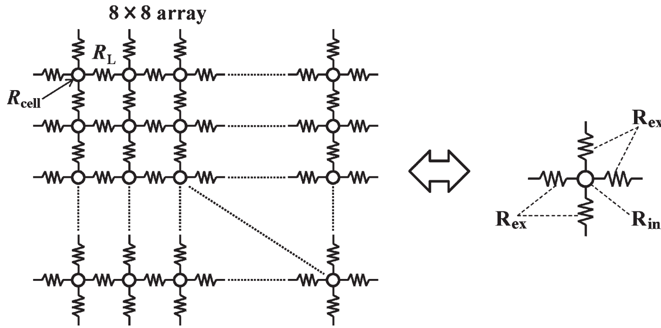

Fig. 8. Equivalent circuit of an 8 × 8 array including all line components. The equivalent unit cell, including one $R_{\rm in}$ and four $R_{\rm ex}$, can be used to expand to large arrays by a power of 8^2.

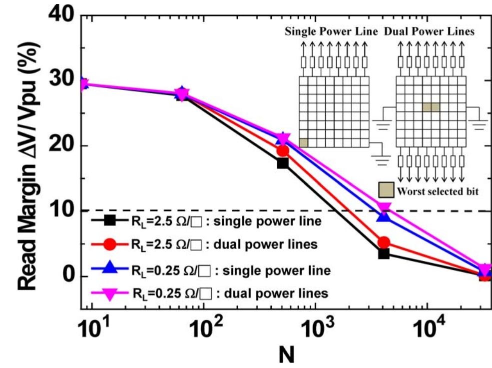

Fig. 9. Worst case read margin simulation of the nonlinear 1S1R crossbar array with nonnegligible line resistance using All-BLPU and a $V_{\rm pu}$ of 3 V. The inset shows the bias schemes using a normal single power line and dual power lines.

Finally, Partial-BLPU is examined with fewer than 100% of the pull-up bit lines. Considering the power consumption per bit, All-BLPU is extremely efficient regarding the simultaneous readout of all bits on the same word line, similar to the page-read operation in NAND Flash for mass data storage. However, fewer pull-up bit lines reduce the power consumption when random read access is desired. Considering the actual worst case read scenario and optimal $R_{\rm pu}$, the read margins of pulling up 0%, 20%, 40%, 60%, 80%, and 100% additional bit lines are shown in Fig. 7 using $V_{\rm pu} = 3$ V. For the given $\alpha(1\ \text{V}, 2\ \text{V}) = 188$ and a minimum of a 10% read margin, All-BLPU substantially increased the maximum array size compared to One-BLPU. Partial-BLPU showed a moderate improvement in the read margin compared to One-BLPU. Therefore, an appropriate number of additional pull-up bit lines can be determined for the desired array size depending on the application.

VI. Effect of Line Resistance

In large crossbar arrays, the voltage drops along the word lines, and bit lines are not negligible. Delivering insufficient voltage to the selected bit can cause problems in the read and write operations. Although Liang and Wong investigated the effects of the line resistance using complete numerical circuit simulation previously [16], the array size they studied was small because of the increasing difficulty of numerical convergence in large arrays. In this paper, an approximated method was used to estimate the line resistance effects of large 1S1R crossbar arrays.

A realistic 8 × 8 crossbar array, including all parasitic line resistors (R_L), can be regarded as a four-port resistor network if all of the word/bit lines at the same port are equally biased. A four-port network was simplified to an equivalent circuit comprising an internal resistor ($R_{\rm in}$) and four external resistors ($R_{\rm ex}$), as shown in Fig. 8. $R_{\rm in}$ was set as being equal to the total resistance of an ideal 8 × 8 array without R_L. The effect of R_L was summed up into the four $R_{\rm ex}$, which were extracted after numerically calculating the total resistance of the 8 × 8 array with R_L. The simple equivalent circuit represents a new unit cell in a 64 × 64 array using an 8 × 8 expansion. Further expansion to 512 × 512, 4096 × 4096, and 32 768 × 32 768 arrays was accomplished using a similar method. This method was based on the four-port network approximation and exhibited some discrepancy in the bias scheme from the exact One-BLPU or All-BLPU but was verified to slightly underestimate the read margin for a conservative projection.

The line resistance effect on the read margin of the All-BLPU 1S1R array is shown in Fig. 9. The R_L values of 0.25 and 2.5 $\Omega/\square$ were investigated. The read margin was measured at the worst selected bit where the least voltage was delivered on the corner farthest from $V_{\rm pu}$ (3 V) and the ground, as shown in the inset of Fig. 9. Because of the high nonlinearity of the 1S1R array, there was little degradation in the 64 × 64 array that differed significantly from the early analysis of the linear crossbar array [16]. A smaller R_L and using dual power lines mitigated the effects of line resistance. The worst bit was moved to the middle of the array using the dual power lines, as shown in the inset of Fig. 9. However, the decrease in the read margin caused by the addition of line resistance became substantial in the 4096 × 4096 (16 Mb) array. The best read margin for the 16-Mb array had a 30% decrease as compared to the one without line resistance but satisfied the sensing criterion of the minimal 10% $\Delta V/V_{\rm pu}$. In addition to the read margin, a practical crossbar array size is limited by the requirement of read speed. An 8-Gb phase-change random access memory that was fabricated using 20-nm CMOS technology has recently demonstrated very high read bandwidth using a similar 8-Mb crossbar subarray [17]. Although a complete RC analysis must be performed in the future, a reasonable read speed can be expected for the 16-Mb 1S1R crossbar array.

In contrast to the read operation, the write operation is typically less problematic in a crossbar array without line resistance using a V/2 or V/3 write scheme. A sufficient voltage margin between the selected bit (V) and the unselected bits (V/2 or V/3) effectively suppresses the write disturb. However, voltage delivery becomes location dependent in large arrays with nonnegligible R_L. The selection of write voltage must ensure that the cell voltage is sufficient for RS at the worst selected bit but must prevent write disturb at the best unselected bit where the most voltage is delivered. For the switching voltages that ranged from |3.5| to |5| V (Fig. 1), a write voltage greater than 5.8 V but less than 7 V can meet both criteria in a 4096 × 4096 1S1R array using a V/2 and dual-power-line write scheme, as shown in Fig. 10. Further improvements are expected if a V/3 write scheme is used.

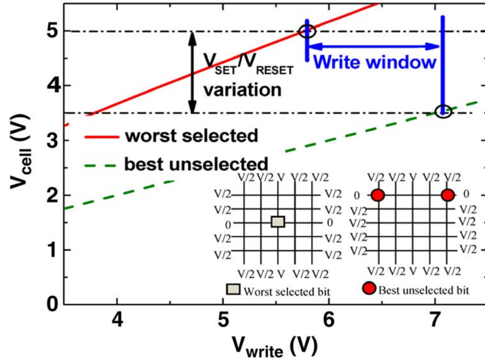

Fig. 10. Dependence of the write voltage on the actual voltage delivered to the worse selected bit and the best unselected bit in a 4096 × 4096 1S1R array. The inset shows the V/2 and dual-power-line write scheme and the measured locations of the worst selected and the best unselected bits.

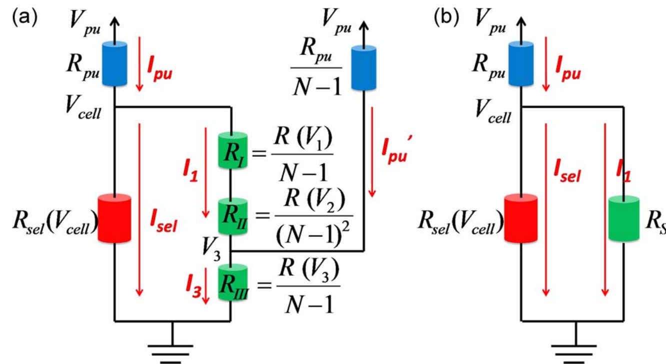

Fig. 11. (a) Equivalent circuit of the general crossbar array used for the analytical calculation of All-BLPU. (b) Simplified equivalent circuit of that in (a) to calculate the effective resistance R_S at the sneak current path.

VII. Conclusion

The read margin in the crossbar RRAM depended strongly on the nonlinear resistance of the memory cell and the read pull-up schemes. For a primitive linear crossbar array, the resistance of the sneak current path, rather than the selected bit resistance, dominated the readout, even when employing an All-BLPU scheme with a read margin that is less dependent on the array size. This problem was mitigated using the 1S1R array because of its highly nonlinear cell resistance. However, the degradation of the read and write margins in the large crossbar array with nonnegligible line resistance must be carefully evaluated. After combining the advantages of All-BLPU and the nonlinear 1S1R array, a high-density array with a size of 16 Mb, at least a 10% read margin and good immunity to write disturb was simulated using the experimental device parameters, confirming a feasible crossbar array architecture and read scheme for ultrahigh-density data storage. Furthermore, regarding random read access, Partial-BLPU can be used to balance the maximum array size and power consumption.

Appendix

The equivalent circuit of a general crossbar array using All-BLPU is shown in Fig. 11(a). V_{cell} and I_1 are obtained by solving the seven Kirchhoff's equations simultaneously. Fig. 11(a) can be further simplified to Fig. 11(b) for easy comparison with One-BLPU. The effective resistance R_S at the sneak current path with the number of pull-up bit lines $m = N$, as shown in Fig. 11(b), is represented as

$$R_S(m=N) = \frac{V_{\text{cell}}}{I_1} = \frac{R_{\text{sel}}(V_{\text{cell}})}{(N-1)^2 R_{\text{pu}}\left(R_{\text{sel}}(V_{\text{cell}}) - R(V_3)\right)} \times \left[(N-1)\left(R_{\text{pu}} + R(V_3)\right) R(V_1) + \left(R_{\text{pu}} + R(V_3)\right) R(V_2) + N(N-1) R_{\text{pu}} R(V_3)\right]. \quad \text{(A1)}$$

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