Characterisation of a suspended nanowire channel thin-film transistor with sub-100 nm air gap

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A novel suspended nanowire (NW) channel thin-film transistor (TFT) with sub-100 nm air gap has been fabricated and characterised. With a simple and low-cost over-etching-time-controlled reactive ion etching technique and a buffered-oxide etch wet-etching process, a suspended NW of 27 nm and an air gap of 10 nm were achieved. The resultant suspended-NW-channel TFTs showed an ultra-low subthreshold swing (52 mV/dec) and considerable hysteresis window (3.7 V). Finally, the impacts of device dimensions on the characteristics of suspended NW TFTs were also investigated.

1. Introduction: The CMOS-MEMS process has recently received increasing attention [1–3] owing to its capability to increase the functionality of IC chips. In addition to forming passive devices [2, 3], active transistors featuring a suspended subject, such as the suspended-gate metal-oxide-semiconductor field effect transistor (SG-MOSFET) [4, 5] and nanoelectromechanical non-volatile memory (NEMory) [6], have become highly attractive for the future nanoscale low-power ICs [7]. Specifically, owing to the existence of an air gap between the control gate and channel, the device depicts an extremely low-gate leakage current as it is operated in the off state [8]. In addition, unlike the conventional MOSFETs, the suspended devices utilise the mechanical switch to achieve the sub-60 mV/dec subthreshold swing (SS) at 300K [4].

However, one major issue associated with the previous works is the high operation voltage, which is typically larger than 10 V and thus not compatible with the modern CMOS circuitries. This is because of the thick air gap (>100 nm) formed in the structure. Theoretically, the operation voltage can be reduced by reducing the gap, but practically it is difficult to achieve considering the deep laterally etched structure [1–7]. To address the issues, a novel suspended nanowire (NW) channel device with smaller air gap was recently proposed by our group [9]. In the devices, the formation of NWs adopting the sidewall spacer-etching techniques developed by our group [10, 11] is easy without using advanced lithography such as e-beam and DUV exposure tools. Furthermore, a sub-100 nm air gap can be achieved by a simple wet-etching step. Such a thin air-gap thickness is beneficial for reducing the operation voltage. In this study, we further investigate the influences of the air-gap thickness on the characteristics of the suspended NW channel thin-film transistor (TFTs).

2. Device structures and fabrication: The top view of a completed device with major structural parameters is shown in Fig. 1. Key process flows are illustrated in Figs. 2*a*–*e*, corresponding to the cross-sectional views cutting along the device centre after each specific step. The fabrication began on Si substrate capped with a thermal oxide. First, an n^+ doped poly-Si layer was deposited by low-pressure chemical vapour deposition (LPCVD) at 550°C and defined as the gate electrode (Fig. 2*a*). An SiN layer and a sacrificial tetraethyl orthosilicate (TEOS) oxide layer were then deposited, respectively, followed by the deposition of a 100 nm amorphous Si. Afterwards, a solid-phase crystallisation (SPC) treatment was then performed to transform the Si film from amorphous into polycrystalline phase (Fig. 2*b*). With a photolithography step and a reactive ion etching (RIE) step, the source/drain (S/D) regions and sidewall NWs were defined simultaneously (Fig. 2*c*). Thereafter, an additional photoresist (PR) layer was covered on the channel region, followed by the phosphorous S/D ion implantation at 15 keV with a dose of 5×10^{15} cm^{-2} (Fig. 2*d*). Note that the PR-covered region defines the channel length of the device, as shown in Fig. 1. A 400 nm passivation oxide layer was deposited on the wafer by LPCVD at 700°C. To physically suspend the NW channels, a wet-etching process was performed to remove the sacrificial TEOS oxide layer between the NW channels and the silicon nitride gate dielectric layer. As a result, an air gap was formed and the suspended NW channel TFTs were accomplished (Fig. 2*e*). Fig. 3*a* is the scanning electron microscopic (SEM) image of a fabricated device showing the formation of the

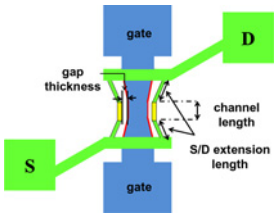

Figure 1 *Top view of the device with suspended NW channels*

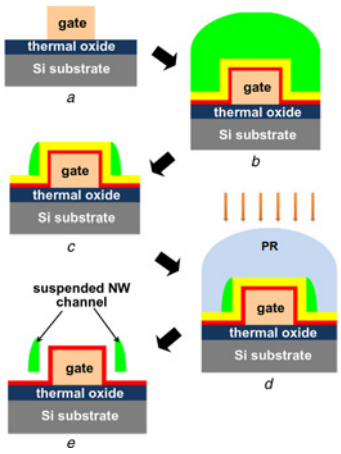

Figure 2 *Key process flows of suspended NW channel TFT*
a Formation of *in situ* doped poly-Si gate
b Deposition of silicon nitride, TEOS and α-Si channel with SPC
c Formation of S/D regions and sidewall spacer NW channels by RIE
d Channel region definition and S/D implantation
e Air-gap formation

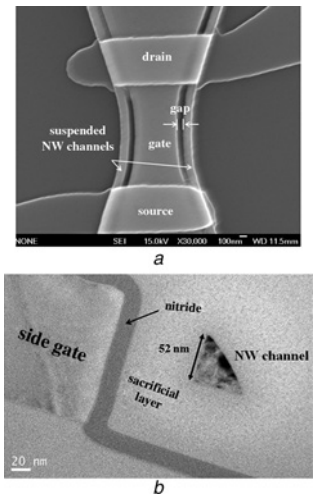

Figure 3 *Images of the air gap and NW channel*
a SEM image of a fabricated device showing the air gap
b TEM image of the cross-sectional profile of a NW channel

air gap. Fig. 3*b* is the transmission electron microscopic (TEM) image of the cross-sectional profile of a NW channel taken before the TEOS layer is stripped.

3. Basic electrical characteristics: Fig. 4 compares transfer characteristics between devices with and without stripping the TEOS oxide. The devices have channel length of 1.0 μm. The original gate dielectric is composed of 30 nm oxide/20 nm nitride; therefore the nominal air gap in the suspended NW channel device is 30 nm. In Table 1, major characteristics of the two devices are summarised, and the one without stripping the TEOS oxide is denoted as the conventional device. In this work, threshold voltage (V_{th}) is defined as the gate voltage at a drain current of 1 nA. It is seen that the suspended NW device exhibits much lower SS, smaller V_{th}, and higher drive current (I_{ON}), even though the estimated nominal equivalent oxide thickness (EOT) of the suspended device (128 nm) is much thicker than that of the conventional one (41 nm). These findings, together with the ultra-low SS of 52 mV/dec, which is lower than the theoretical limit of 60 mV/dec for the conventional MOSFETs, evidence the mechanical mechanism of the suspended channel modulated by the gate bias.

4. Effects of the NW length: Figs. 5*a* and *b* show the hysteresis characteristics of the suspended NW channel devices with different channel length and S/D extension length, respectively. In these Figures, the gate voltage (V_G) was first swept forward from a negative value to a positive one, and then backward to return to the negative initial value. As has been pointed out in our previous work [9], pull-in of the NW channels is mainly triggered by the attractive

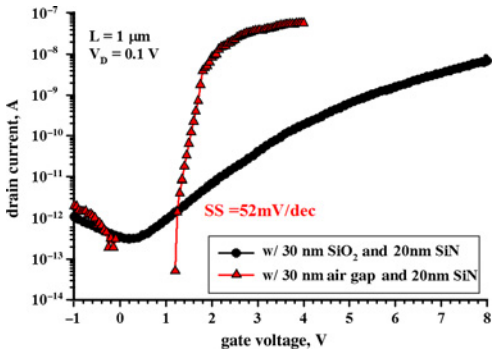

Figure 4 *I_D–V_G curves of conventional TFT and suspended-NW-channel TFT*

Table 1 Summary of the major characteristics of the conventional and suspended devices (extracted from *I* to *V* curves shown in Fig. 4)

	EOT, nm	SS,[a] mV/dec	V_{th},[b] V	I_{on}, nA	I_{off},[e] pA
Suspended NW Channel device	128	52	1.67	57.6[c]	0.12
Conventional NW Channel device	41	928	4.83	11.5[d]	0.34

[a]Minimum value in the subthreshold regime
[b]Defined as the V_G at drain current of 1 nA
[c]Extracted at V_G of 4 V
[d]Extracted at V_G of 8 V
[e]Extracted at V_G of 0 V

electrostatic force exerted by the applied gate voltage. However, as the central NW channels get connected with the gate nitride, additional components, such as the van der Waal force [12], become significant and should be taken into account. As a result, in the backward sweeping the NW channels tend to be pulled out and separate from the gate nitride at a voltage smaller than the pull-in one. This explains the hysteresis characteristics. In Fig. 5*a*, for the devices with a given S/D extension length of 0.5 and 100 nm air gap, as the channel length increases from 0.4 to 5.0 μm, the V_{th} in the forward sweeping, hysteresis window and the ON current all decrease accordingly. On the other hand, for the two devices shown in Fig. 5*b* with the same channel length (2 μm) but different S/D extension length (0.25 or 0.5 μm), the aforementioned trends occur only to the one with a longer S/D extension. Since the total length of the NW is the sum of the channel and extension regions, the above findings are postulated to be related to the increase in elastic constant with decreasing NW length. According

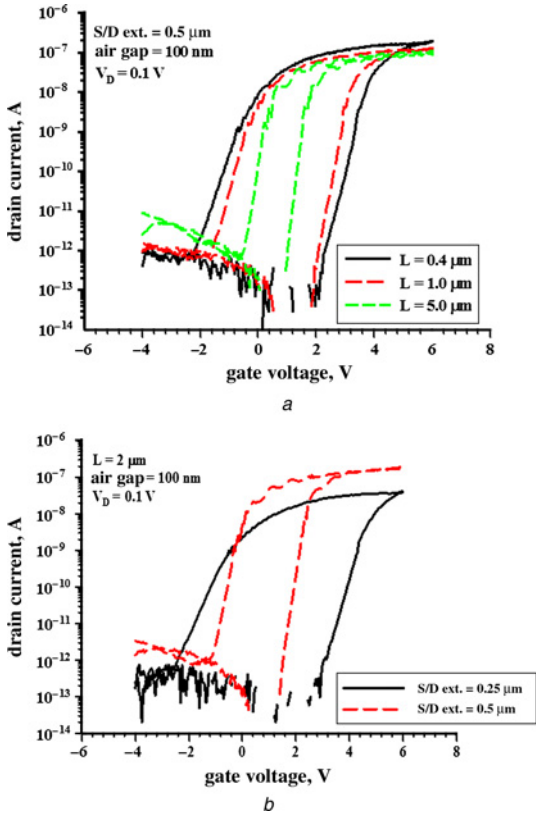

Figure 5 *Hysteresis curves of the suspended-NW-channel TFTs*
a With channel length of 0.4, 1 and 5 μm, respectively
b With S/D extension length of 0.25 and 0.5 μm, respectively

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to one previous work [12], elastic constant is inversely proportional to the cubic power of the length of the suspended subject. Therefore for a device with a shorter channel length or S/D extension length, it needs a larger electrically attractive force to overcome the elastic force. This leads to a larger V_{th} as observed in these Figures.

In Fig. 5*b*, the one with extension length of 0.25 μm presents a lower ON current, although its total NW length is longer than the other device characterised in this Figure. As has been pointed out in our previous work [9], the contact of the NW channel with the gate nitride during operation occurs mainly in the channel centre, rather than the whole channel. The above difference in the two devices can thus be attributed to the reduced length of the 2 μm-long undoped suspended channels in contact with the gate nitride in the ON state for the device with shorter (0.25 μm) S/D extension. An air gap remains in the isolated NW regions, resulting in a larger EOT and thus limiting the drive current.

5. Effects of the air gap: Impacts of the air-gap thickness on device performance are exhibited in Fig. 6*a*, where devices with four different air-gap thicknesses (10, 30, 80 and 100 nm) are characterised and compared. Clearly, the air-gap thickness strongly affects the electrical characteristics of the devices with suspended NW channels. A thinner gap corresponding to a smaller electrostatic force attracting the suspended channels results in smaller V_G, as shown in Fig. 6*b*. Besides, smaller displacement of NWs leads to a smaller elastic recovery force causing easier occurrence of the pull-out process, that is, a larger V_{th} in the reverse sweeping. This implies the hysteresis window generally increases as the gap thickness increases. Compared with the SG-FET with high pull-in voltage (>10 V) [13], the suspended-NW-channel devices with sub-100 nm gap thickness indeed depict a much reduced threshold voltage (e.g. 1.11 V for t_{gap} = 10 nm), which is compatible with modern CMOS circuitries.

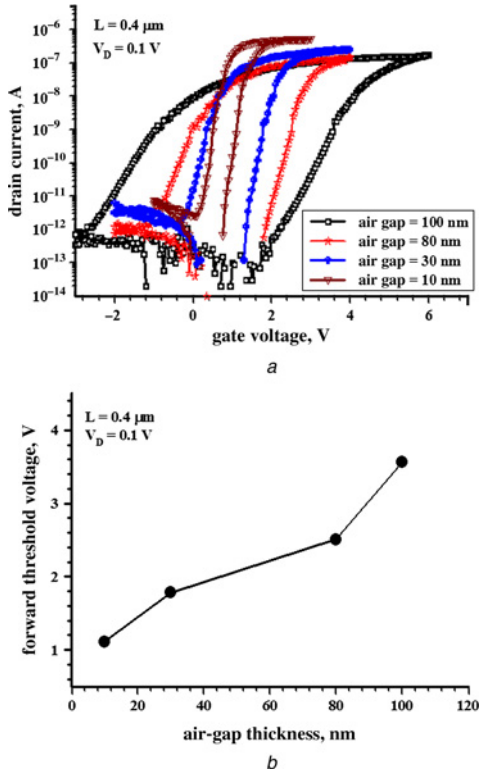

Figure 6 *Impacts of the gap thickness on the fabricated devices with four different NW thicknesses*
a Hysteresis curves of the suspended NW channel TFTs with gap thickness of 100, 80, 30 and 10 nm, respectively
b Plot of forward V_{th} against gap thickness for the suspended NW channel TFTs

This is attributed to the reduction in initial air-gap thickness as well as the use of tiny NW as the suspended object.

6. Conclusion: In this study, we characterised a novel suspended-NW-channel device with major attention paid to the effects of device structural parameters. As compared with the case without an air gap, superior characteristics including steeper SS and lower V_{th} are achieved with the proposed devices. We have also studied how the geometric structural dimensions such as channel length, S/D extension length, and air gap affect the device characteristics. These results show that, as the air gap is shrunk below 100 nm, the proposed device with a small V_{th} compatible with modern CMOS circuitries is feasible.

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