The Design of Double-Positive-Feedback Voltage-Controlled Oscillator

Zue-Der Huang and Chung-Yu Wu, *Fellow, IEEE*

***Abstract*—A 24 GHz 1.4-mW double-positive-feedback voltage-controlled oscillator (DPF-VCO) has been designed and realized in a 0.13 μm CMOS process. In the proposed DPF-VCO, the concept of double positive feedback loops is adopted to enhance the VCO performance and the current-mode output technique is used to obtain the output current signal. The fabricated DPF-VCO consumes only 0.78 mA, 0.97 mA, and 1.17 mA under the supply voltage of 1, 1.1, and 1.2 V, respectively, and the corresponding measured phase noise is -104 dBc/Hz, -112 dBc/Hz, and -115 dBc/Hz at 1 MHz offset frequency. The best FOM of the proposed DPF-VCO is -201 dBc/Hz.**

***Index Terms*—Colpitts, double-positive-feedback voltage-controlled oscillator (DPF-VCO), negative resistance, phase noise.**

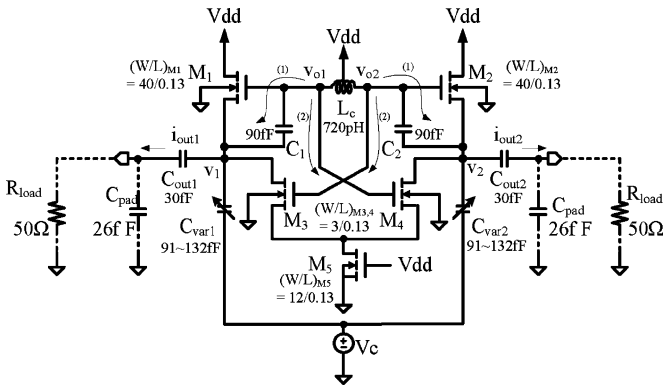

Fig. 1. Circuit diagram of the proposed DPF-VCO.

I. Introduction

THE fast growth of wireless applications in recent years has driven intense effort to design highly-integrated, high-performance, low-cost, and low-power radio-frequency integrated circuits (RFICs). In the modern design of RF transceivers, a fully-integrated frequency synthesizer to produce a precise local oscillator (LO) signal for channel selection is required. Therefore, a VCO with low voltage, low phase noise, and low power is essential.

Recently, many VCOs operated at K-band (17 to 29 GHz) have been reported in [1]–[5]. In order to have good performance of phase noise and low power consumption, multi-feedback-loop technique has been presented and utilized in VCOs. In [3], a differential Clap-VCO is demonstrated with the phase noise of -110.5 dBc/Hz at 1 MHz. The power consumption is 5.4 mW and the FOM is -188.7 dBc/Hz. In [4], the capacitive feedback loop is used to increase its small signal gain to have good phase noise of -111 dBc/Hz at 1 MHz and can be operated at 20 GHz. In [6]–[8], the technique of transformer feedback and inductive feedback are also proposed. With the transformer feedback, the quality factor can be improved to enhance the phase noise performance and reduce the power consumption.

The goal of this letter is to design a new double-positive-feedback VCO (DPF-VCO) to achieve better phase noise and lower power consumption. With the double positive feedback loops, the two negative resistance circuits of the VCO can increase the negative resistance with the shared dc bias current to reduce the power consumption. The NMOS cross-coupled pair makes the circuit differential to prevent the start-up problem occurred in some VCOs as discussed in [9]. The proposed DPF-VCO has been designed and fabricated by using 0.13 μm CMOS technology. The performance of the DPF-VCO is verified through the experimental results. The fabricated VCO consumes only 0.78 mA, 0.97 mA, and 1.17 mA under the voltage of 1, 1.1, and 1.2 V, respectively. The corresponding measured phase noise is -104 dBc/Hz, -112 dBc/Hz, and -115 dBc/Hz at 1 MHz offset frequency. The best FOM of the proposed VCO is -201 dBc/Hz.

In Section II, the proposed DPF-VCO is presented and analyzed. In Section III, the measurement results of the fabricated DPF-VCO are demonstrated. Finally, the conclusion is given in Section IV.

II. Circuit Realization of DPF-VCO

The circuit diagram of the proposed DPF-VCO is shown in Fig. 1 where the concept of combining a differential Colpitts with a cross-coupled pair structure is adopted to increase the negative resistance under low supply voltage. The bias current is reused to maintain low power consumption under lower supply voltage. The circuit is composed of two single-ended Colpitts oscillators and one NMOS cross-coupled core. As shown in Fig. 1, $(M_1, C_1, C_{\rm var1})$ and $(M_2, C_2, C_{\rm var2})$ form two single-ended Colpitts structures to provide the primary negative resistance. (M_3, M_4) is the NMOS cross-coupled pair to contribute the secondary negative resistance in the DPF-VCO. M_5 is to supply the dc bias current and Vc is the controlled voltage to tune the frequency of VCO through the varactors $C_{\rm var1}$ and $C_{\rm var2}$. The resonant frequency of the VCO is determined by the LC tank of $(L_{\rm C}, C_{1,2}, C_{\rm var1,var2})$ with inductance of 0.48 nH and quality factor of 17.

Manuscript received March 28, 2011; accepted May 02, 2011. Date of publication June 09, 2011; date of current version July 07, 2011. This work was supported by the National Science Council of Taiwan under Grant NSC 96-2221-E-009-179. and CIC, National Applied Research Laboratories, Taiwan, for the fabrication of chip.

The authors are with the Nanoelectronics and Gigascale Systems Laboratory, Department and Insititute of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: zuederhu.ee93g@nctu.edu.tw).

Digital Object Identifier 10.1109/LMWC.2011.2156776

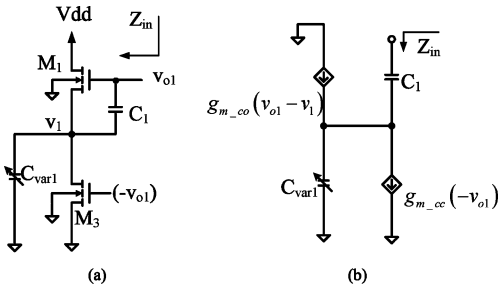

Fig. 2. (a) Half circuit of DPF-VCO for negative resistance calculation (b) the small-signal model of half circuit for negative resistance calculation.

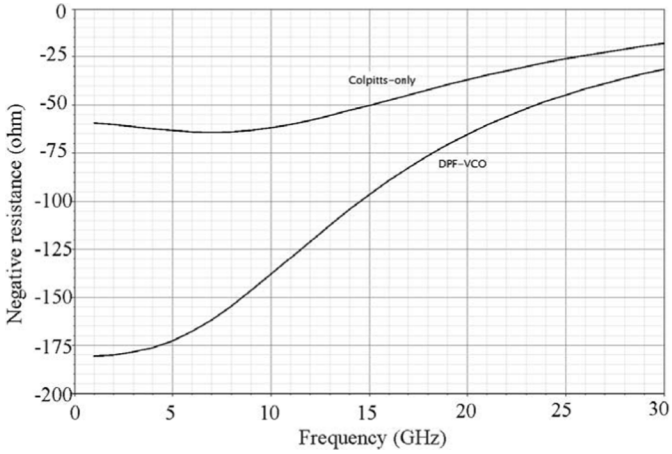

Fig. 3. Spectre-RF simulated negative resistance of Colpitts-only structure and DPF structure.

In Fig. 2(a), the half circuit of DPF-VCO for negative resistance calculation is shown and its small-signal model is presented in Fig. 2(b). From Fig. 2(b), the input impedance can be calculated as

$$Z_{in} = \frac{sC_1 + sC_{\text{var1}} + g_{m\_co}}{s^2 C_1 C_{\text{var1}} - sC_1 g_{m\_cc}} = -\frac{g_{m\_co} + j\omega\left(C_1 + C_{\text{var1}}\right)}{\omega^2 C_1 C_{\text{var1}} + j\omega C_1 g_{m\_cc}} \quad (1)$$

where g_{m_co} and $g_{\text{m\_cc}}$ are the transconductance of M_1 and M_3, respectively. From (1), the real part and imaginary part of Zin can be derived as

$$\text{Re}\{Z_{in}\} = -\left(\frac{g_{m\_co}C_{\text{var1}}}{\omega^2 C_1 C_{\text{var1}}^2 + C_1 g_{m\_cc}^2} + \frac{g_{m\_cc}\left(C_1 + C_{\text{var1}}\right)}{\omega^2 C_1 C_{\text{var1}}^2 + C_1 g_{m\_cc}^2}\right) \quad (2)$$

$$\text{Im}\{Z_{in}\} = -\left(\frac{\omega^2 C_{\text{var1}}\left(C_1 + C_{\text{var1}}\right) - g_{m\_cc}g_{m\_co}}{\omega^3 C_1 C_{\text{var1}}^2 + \omega C_1 g_{m\_cc}^2}\right). \quad (3)$$

The g_{m_co} and g_{m_cc} for this circuit are 8.16 mS and 1.862 mS, respectively. The calculated negative resistance from (2) at 24 GHz is $-50.6\ \text{ohm}$. The comparison of simulated negative resistance by SpectreRF between DPF-VCO and single-ended Colpitts VCO is presented in Fig. 3. As can be seen in Fig. 3, the simulated negative resistance of the DPF-VCO at 24 GHz is much greater than that of Colpitts-only structure under the same dc power consumption.

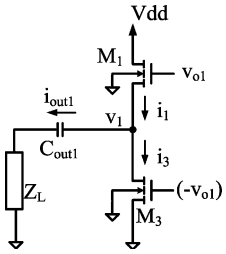

Fig. 4. Simplified half circuit of DPF-VCO for RF current outputs.

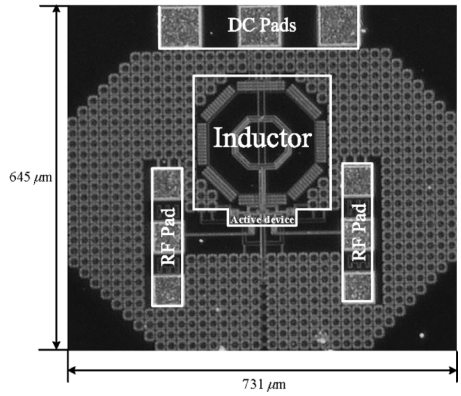

Fig. 5. Chip photo of the proposed VCO.

In this design, the output currents are generated through $M_1(M_3)$ and $M_2(M_4)$ that are controlled by the $v_{ol}(v_{o2})$ and $v_{o2}(v_{o1})$, respectively. By neglecting C_1 in Fig. 2(a), the simplified half circuit of DPF-VCO that only contains M_1, M_3, and can be shown in Fig. 4. Under the assumptions of infinite output resistance r_o of the transistor in Fig. 4 and low impedance of C_{out1} at high frequency, both effects are neglected to simplify the derivation. By applying the small-signal model, the RF current i_{out1} is the difference of the two currents of i_1 and i_3 and the relationship can be shown as

$$i_1 - i_{out1} - i_3 = g_{m\_co}\left(v_{o1} - v_1\right) - i_{out1} - g_{m\_cc}\left(-v_{o1}\right) = 0 \quad (4)$$

and the i_{out1} can be expressed as

$$i_{out1} = v_{o1}\left(g_{m\_co} + g_{m\_cc}\right)\left(1 - \frac{g_{m\_co}}{g_{m\_co} + \frac{1}{Z_L}}\right). \quad (5)$$

As can be seen from (5), when load impedance Z_L is smaller, the output current is larger.

III. Experimental Results

The proposed 24 GHz DPF-VCO was fabricated in 0.13-μm 1P8M CMOS technology and the chip photo are shown in Fig. 5 and the circuit occupies $0.073\ \text{mm}^2$ for the active region.

The maximum measured tuning range is 7% which is from 22 to 23.6 GHz as the controlled voltage Vc is varied from 0 V to the supply voltage of 1.2 V. The measured tuning curves of the fabricated VCO with different supply voltages and controlled voltages are shown in Fig. 6. Fig. 7 shows the output spectrum which is around $-23\ \text{dBm}$ and its center frequency is at 23.5 GHz at a 1.2 V supply voltage. The measured phase noise at 1 MHz offset versus different supply voltage is shown in

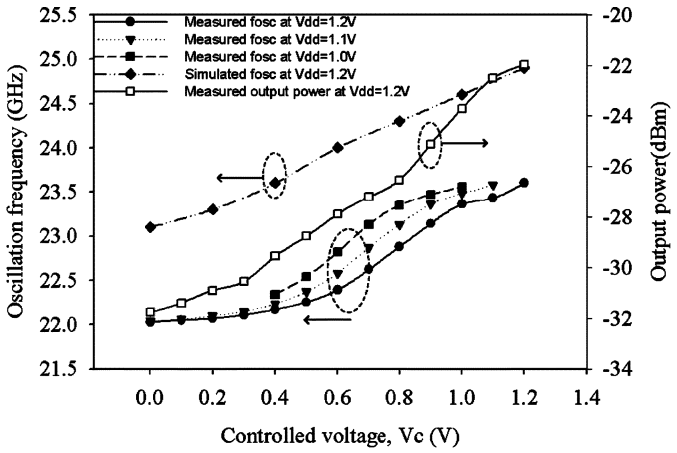

Fig. 6. Measured tuning range of VCO at $\mathrm{Vdd} = 1.2$ V, 1.1 V, and 1 V, respectively, with the controlled voltage varied from 0 to Vdd.

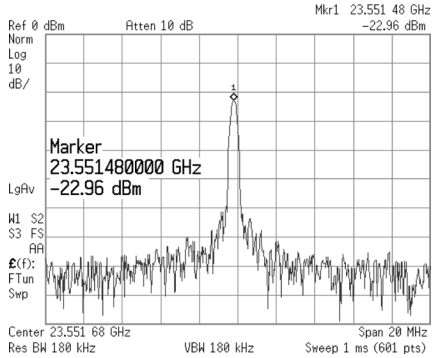

Fig. 7. Measured output spectrum of VCO.

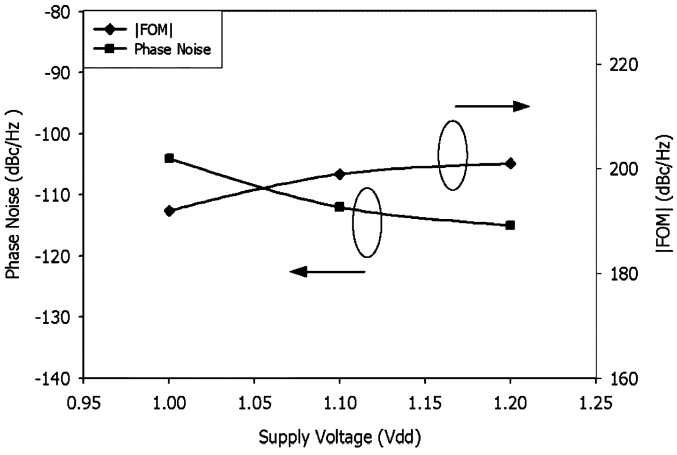

Fig. 8. Measured phase noise at 1 MHz frequency offset and $|\mathrm{FOM}|$ of the stand-alone DPF-VCO versus different supply voltages.

Fig. 8. As shown in Fig. 8, the phase noises are -115, -112, and -104 dBc/Hz under different supply voltages of 1.2 V, 1.1 V, and 1 V, respectively. In Fig. 8, the figure-of-merit (FOM) [2] of the fabricated DPF–VCO at 1 MHz offset frequency is also calculated as -201, -199, and -192 dBc/Hz, respectively. The current consumption is 1.17 mA under 1.2 V supply voltage and 0.78 mA under the lowest supply voltage of 1 V.

TABLE I
PERFORMANCE COMPARISONS OF VCOS

	This work			[3]	[4]	[5]
Process (CMOS)		0.13		0.13	0.18	0.13
Vdd (V)	1.2	1.1	1.0	0.9	1.8	1.2
Pnoise @1MHz	-115	-112	-104	-110.5	-111	-117
f_{osc} (GHz)	22.8	22.8	22.9	18.8	19.9	18
Tuning range	7 %	6.9 %	5.3 %	9 %	2.5 %	5.5 %
Pout (dBm)	-23	-27	-29	-19	-3	-10
Power (mW)	1.4	1.1	0.78	5.4	32	14.4
Area (mm^2)	0.47	0.47	0.47	0.564	0.43	0.12
FOM (dBc/Hz)	-201	-199	-192	-188.67	-182	-189

The measured performance of the VCO is summarized in Table I, along with the comparisons with the previously published CMOS K-band VCOs. As can be seen from Table I, the proposed DPF-VCO has the advantages of low phase noise and low power consumption.

IV. CONCLUSION

In this work, a DPF-VCO has been designed and fabricated by the 0.13 μm 1P8M CMOS technology process. For the DPF-VCO, the double-positive-feedback concept has been adopted to lower the phase noise and reduce the power consumption. From the experimental results, the DPF-VCO only consumes 1.17 mA under the voltage of 1.2 V and 0.78 mA under the lowest supply voltage of 1 V. The best measured phase noise is -115 dBc/Hz at 1 MHz offset frequency and the FOM of VCO is -201 dBc/Hz.

REFERENCES

[1] J. Kim *et al.*, "A 20 GHz phase-locked loop for 40 Gb/s serializing transmitter in 0.13 μm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2005, pp. 144–147.

[2] D. Ozis, N. M. Neihart, and D. J. Allstot, "Differential VCO and passive frequency doubler in 0.18 μm CMOS for 24 GHz applications," in *Proc. IEEE RFIC Symp. Dig. Papers*, Jun. 2006, pp. 33–36.

[3] S.-L. Jang, Y.-J. Song, and C.-C. Liu, "A differential clapp-VCO in 0.13 μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 6, pp. 404–406, Jun. 2009.

[4] H.-H. Hsieh and L.-H. Lu, "A low-phase-noise K-band CMOS VCO," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 10, pp. 552–554, Oct. 2006.

[5] G. L. G. de Mercey, "A 18 GHz rotary travelling wave VCO in CMOS with I/Q outputs," in *Proc. Eur. Solid-State Circuits Conf.*, Sep. 2003, pp. 489–492.

[6] M.-D. Tsai, Y.-H. Cho, and H. Wang, "A 5 GHz low phase noise differential Colpitts CMOS VCO," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 5, pp. 327–329, May 2005.

[7] N.-J. Oh and S.-G. Lee, "11 GHz CMOS differential VCO with back-gate transformer feedback," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 11, pp. 733–735, Nov. 2005.

[8] J.-A. Hou and Y.-H. Wang, "A 7.9 GHz low-power PMOS Colpitts VCO using the gate inductive feedback," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 4, pp. 224–226, Apr. 2010.

[9] R. Aparicio and A. Hajimiri, "A noise-shifting differential coltpitts VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1728–1736, Dec. 2002.