A Flexible IGZO Thin-Film Transistor With Stacked TiO_2-Based Dielectrics Fabricated at Room Temperature

Hsiao-Hsuan Hsu, Chun-Yen Chang, and Chun-Hu Cheng

***Abstract*— This letter demonstrates the feasibility of full room temperature InGaZnO thin-film transistor (TFT) using trilayer gate dielectric on flexible substrate. Through integrating high-κ $SiO_2/TiO_2/SiO_2$ (STS) gate-stack as well as InGaZnO channel thickness modulation, the resulting flexible indium–gallium–zinc oxide (IGZO)/STS TFTs show low threshold voltage of 0.5 V, small subthreshold swing of 0.129 V/decade, high field effect mobility of 76 cm^2/Vs, and good I_{ON}/I_{OFF} ratio of 6.7×10^5, which have the potential for the application of high-resolution flexible display.**

***Index Terms*— High-κ, indium–gallium–zinc oxide (IGZO), thin-film transistor (TFT), TiO_2.**

I. Introduction

THE indium–gallium–zinc oxide (IGZO) [1]–[4] thin-film transistor (TFT) has shown high potential to provide large drive current, especially required for driving high-resolution light-emitting diode. The amorphous IGZO TFTs give several advantages over poly-silicon TFT including high mobility and low-thermal budget for TFT process, which offer highly integrated capability with high-resolution flexible display. Although various high-κ gate dielectrics are proposed [5]–[9] for low-temperature flexible TFT fabrication, they cannot overcome the defect issues including low dielectric constant (κ value) and high-intrinsic leakage, even using commercial HfO_2 ($\kappa \sim 16$) [3] and ZrO_2 ($\kappa \sim 18$) dielectrics [9]. In addition to large operating voltage, IGZO flexible TFTs still suffer from high subthreshold swing (SS) and low-device mobility that is most critical for high-speed and high-resolution display application. To investigate these issues on low-temperature flexible device, we fabricate a high-performance α-IGZO TFT using high-κ $SiO_2/TiO_2/SiO_2$ (STS) dielectric on polycarbonate (PC) substrate at room temperature (RT). The high-κ TiO_2 has a very high-κ value of > 40 [10], which can benefit the driving current and lower down the operating voltage. This flexible IGZO TFT shows a small SS of 0.129 V/decade, a low threshold voltage (V_t) of 0.5 V and a high field effect mobility (μ_{FE}) of 76 cm^2/Vs, which is much better than other reported low-temperature (or RT) TFT devices [5]–[9].

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H.-H. Hsu and C.-Y. Chang are with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan (e-mail: bluejerry723@hotmail.com).

C.-H. Cheng is with the Department of Mechatronic Technology, National Taiwan Normal University, Taipei 10610, Taiwan.

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II. Experiments

The TFT device with bottom gate structure is fabricated on the 300-nm thick insulating SiO_2 grown on a PC flexible substrate. PC substrate has a very small root mean square (rms) of 0.34 nm that is close to that (rms = 0.22 nm) on glass substrate. A 30-nm thick TaN bottom gate electrode is initially formed by sputtering and patterning. Subsequently, an optimized dielectric stack of STS with a total thickness of 80 nm (16/56/8 nm) is deposited by electron beam evaporation. The control samples of TiO_2 and $HfO_2/TiO_2/HfO_2$ (HTH) are also deposited for comparison. Such a physical vapor deposition is preferred for the gate dielectric deposition of TFT because of its low-thermal budget, especially on plastic substrates [11]. After depositing gate dielectric stack, a 23-nm thick IGZO active layer with an atomic ratio of In:Ga:Zn:O = 2:2:1:7 is deposited using radio frequency sputtering in a gas mixture with 30% O_2 in argon ambient. Finally, 300 nm thick Al is thermally evaporated onto the active region to form source and drain contact electrodes. The metal-insulator-metal (MIM) capacitors of TiO_2 and SiO_2 are also fabricated side-by-side to characterize the gate capacitance and leakage current. The TFT devices with channel size of 521×32 μm are characterized by current–voltage (I–V) and capacitance–voltage (C–V) measurements, respectively.

III. Results and Discussion

Fig. 1(a) shows the photograph and cross-sectional view of TEM images of IGZO/STS gate-stack. The IGZO channel and TiO_2 dielectric are examined by fast Fourier transform, where the diffractograms exhibit amorphous phases. The amorphous IGZO without crystallization can reduce interface traps between IGZO channel and high-κ dielectric that may affect transistor properties, especially for flexible device with low-temperature fabrication. In Fig. 1(b), the corresponding EDX confirms that the composition ratio of amorphous IGZO film is close to that of sputter target. The vacancy control of In-rich IGZO is critical in enabling RT-processed TFT that operates at high drive current; moreover, a low channel leakage (high channel resistivity) obtained by a reduced channel thickness can be used to reach a low OFF-state current.

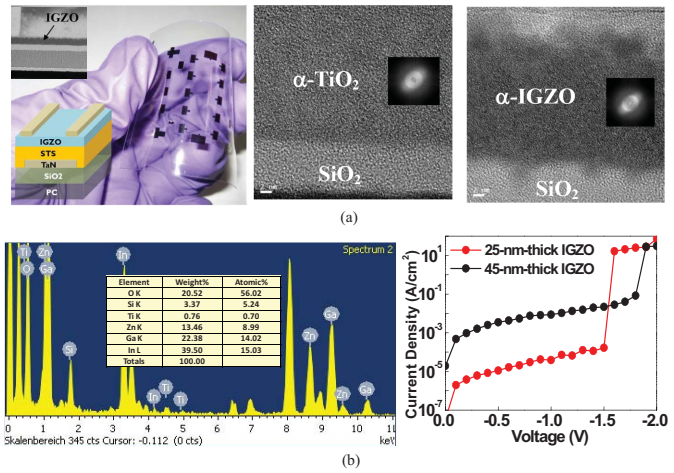

Fig. 1. (a) Photograph and cross-sectional TEM images of IGZO/STS TFT devices on flexible PC. (b) EDX analysis and I–V characteristics of MIM capacitors with 25 and 45-nm thick IGZO layers.

Fig. 2(a) shows the C–V and I–V characteristics of Al/[TiO_2, SiO_2, and STS]/TaN MIM capacitors with different thicknesses on flexible PC. The high-capacitance density of 3.4 fF/μm^2 is measured for 95-nm thick TiO_2 MIM capacitors with RT process, giving a very high-κ value of 37. The large gate capacitance density can benefit transistor characteristics especially for increasing drive current and lowering operation voltage. In addition, the large gate leakage of 1.2×10^{-5} A/cm^2 at -1 V is further decreased by $\sim$28$\times$ after inserting thin SiO_2 buffer layers with large conduction offset (ΔE_C) of 4.27 eV [12]. This RT-evaporated thin SiO_2 (rms $\sim$ 6.3 A) without plasma damage caused by sputtering [13] can effectively reduce interface state near IGZO.

More noteworthy is the finding that the gate leakage of TiO_2 becomes less temperature dependent when film annealing is processed below 300 °C. As shown in Fig. 2(b), the RT TiO_2 with similar capacitance equivalent thickness (CET) of 6 nm only exhibits 1.7$\times$ increase in gate leakage at -1 V compared with 200 °C annealed condition. This result is also supported by good CET scaling trend that is favorable for reaching high-capacitance density at RT TFT process.

In Fig. 3, XPS spectra show that the Si 2p peaks centered at the binding energy of 103.7 eV correspond to the oxidation state of Si^{4+}, which is close to that of stoichiometric SiO_2 with binding energy of 103.8 eV [14]. The binding energy of 99.2 eV is contributed by Si substrate. The film quality of RT SiO_2 is verified by a 14-nm thick MIM capacitor with a low leakage current of 4×10^{-6} A/cm^2 at -1 V [Fig. 2(a)]. As for higher κ TiO_2 film, the Ti $2p_{3/2}$ and Ti $2p_{1/2}$ peaks located at 459.3 and 465.1 eV, respectively, correspond to the Ti^{4+} oxidation state [15]. Beside, the O 1s peak of TiO_2 dielectric could be deconvoluted into two doublets with binding energies of 530.9 and 532.4 eV by Gaussian function, indicating that higher binding energy of 532.4 eV is attributed to the formation of O–H and O = C bonds. Although the titanium-terminated surface may result in a degraded mobility because of high-interface vacancy defects at the IGZO/TiO_2 interface, the interface trap issue can be reduced by the insertion of smooth SiO_2 buffer layer. Additionally, the valence band offset

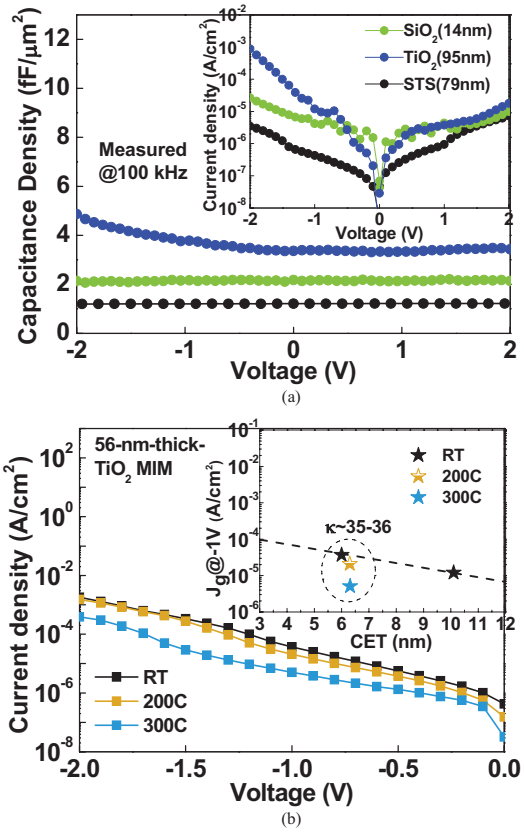

Fig. 2. (a) C–V and I–V characteristics of MIM capacitors using SiO_2, TiO_2, and STS dielectrics. (b) I–V characteristics of 56-nm thick TiO_2 MIM capacitor with different annealed conditions. Inset: corresponding CET verse gate leakage (CET-J_g) characteristics.

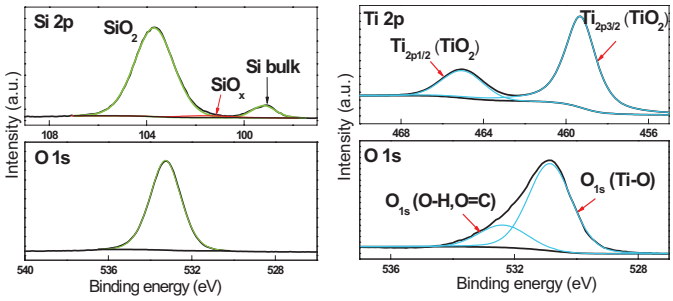

Fig. 3. Core-level XPS spectra of SiO_2 and TiO_2 dielectrics.

(ΔEv) of 0.2 eV [16] provides better hole blocking capability than high-temperature stable SiN ($\Delta Ev \sim 0.15$ eV) [17] and ZrO_2 ($\Delta Ev \sim 0$) [18]. Thus, the RT TiO_2-based dielectric integrity on IGZO is evaluated from the aspects of bandgap engineering and material analysis that is much different to our understanding on high-κ dielectrics for high-temperature CMOS application.

In Fig. 4(a), we present the transfer I_d–V_g characteristics of IGZO TFTs using gate dielectrics of TiO_2, STS, and HTH on flexible PC. From the measured results, the IGZO/TiO_2 TFT has a low-operating voltage of 1 V, but suffers small I_{ON}/I_{OFF} ratio of $< 10^3$ because of large gate leakage. In contrast, well-behaved transistor output characteristics are observed in IGZO/STS TFT. The low subthreshold gate swing calculated from I_d–V_g curve is 0.129 V/decade under a low drive voltage

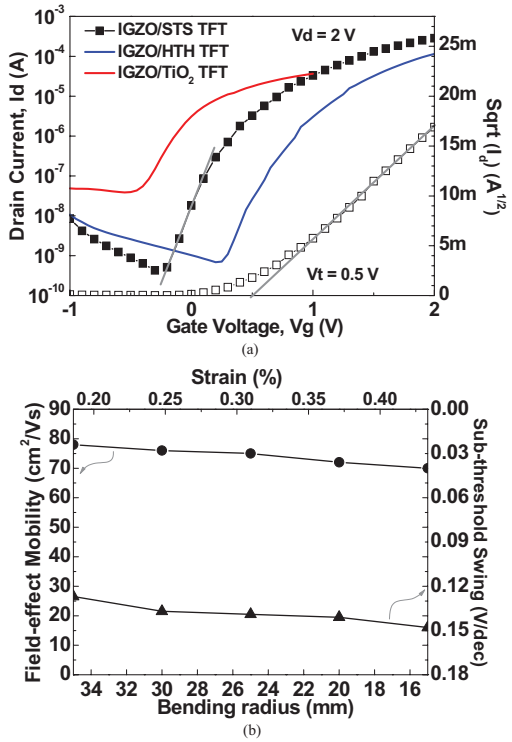

Fig. 4. (a) I_d–V_g characteristics of IGZO TFT devices with gate dielectrics of TiO_2, STS, and HTH. (b) Field-effect mobility and SS as a function of bending radius for IGZO/STS TFT. The square root of drain current as a function of gate voltage for threshold voltage extraction by linear extrapolation.

$(V_g–V_t) < 2$ V. In addition to the small SS, a I_{ON}/I_{OFF} ratio of 6.7×10^5, a low V_t of 0.5 V, and a high μ_{FE} of 76 cm^2/Vs are achieved simultaneously in IGZO/STS TFT. Such good performance is even comparable with Si-based IGZO TFT. Another control IGZO TFT using RT HfO_2 buffer layers also show larger V_t of 0.95 V and lower drive current, which is ascribed to poor quality HfO_2 film processed at RT. These results explain that a comprehensive consideration on gate-stack process is important to implement a fully RT-fabricated flexible TFT.

To further evaluate bending flexibility, we perform bending test with the radius from 35 to 15 mm, as shown in Fig. 4(b). The transistor characteristics under bending shows slightly degraded SS and device mobility that demonstrates the feasibility of IGZO/STS TFT for flexible display application. Therefore, the RT flexible TFT device with good transistor characteristics can be attributed to the combined effect of improved TiO_2-based dielectric stack and IGZO thickness modulation that allows for flexible device fabrication even at RT.

IV. Conclusion

The stacked STS dielectric was successfully integrated with a-IGZO TFTs on flexible PC substrate at RT process. The flexible IGZO/STS TFTs showed a low V_t of 0.5 V and small SS of 0.129 V/decade, and high μ_{FE} of 76 cm^2/Vs at a low-operation voltage of 2 V.

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