In-Plane Gate Transistors for Photodetector Applications

Yu-An Liao, Wei-Hsun Lin, *Student Member, IEEE*, Yi-Kai Chao, Wen-Hao Chang, *Member, IEEE*, Jen-Inn Chyi, *Fellow, IEEE*, and Shih-Yen Lin, *Senior Member, IEEE*

***Abstract*— In-plane gate transistors (IPGTs) with 20-μm channel widths are fabricated on samples with n-(InGa)As sheet resistance embedded in undoped GaAs matrix. A trade-off between effective current modulation and high saturation drain current is obtained by optimizing the doping density of the sheet resistance. The mechanism responsible for the transistor behaviors of the devices is due to the channel electron depletion related to the population of mobile surface electrons under different gate biases. The photocurrent measurements demonstrate that the IPGT architecture is a feasible approach for the applications of photodetectors.**

***Index Terms*— Detectors, in-plane gate transistors (IPGTs).**

I. Introduction

UNLIKE traditional high-electron-mobility transistors (HEMTs) with gates above the channels, in-plane gate transistors (IPGTs) have provided an alternate choice for the fabrications of HEMTs [1]–[3]. It is generally accepted that nanometer-sized channels are required to avoid high threshold voltages. In this case, nanofabrication techniques such as e-beam lithography are always required for the fabrications of such devices [1]–[3]. In one of the previous publications, room-temperature transistor behaviors of IPGTs fabricated using repeated atomic-force microscopy (AFM) anode oxidation for electrical isolations are also demonstrated [4], [5]. Although the device architecture has greatly simplified the fabrication procedures of HEMTs, the adoption of either e-beam or AFM systems is still disadvantageous for further fabrication procedure simplification. In another publication, IPGTs with micrometer-sized channel widths are fabricated by using standard photolithography [6]. The operation mechanism responsible for the device is the 2-D electron gas depletion resulted from mobile surface electrons manipulated by the external gate voltages. Therefore, if the same mechanism could also be applied to the sheet resistance such as n-(InGa)As layers embedded in undoped GaAs, the IPGT architecture can be easily applied to detectors in the near-infrared range simply by changing the In compositions.

In this letter, drain current modulations are observed for an n-GaAs sheet resistance embedded in undoped GaAs matrix at room temperature with channel width of 20 μm. With appropriate doping density of the n-GaAs layer, the drain current can be turned off under acceptable negative gate biases. The photocurrent measurements of devices with n-GaAs and n-$In_{0.1}Ga_{0.9}As$ channels exhibited extended absorption wavelengths for the latter one.

II. Experiments

The samples with 50-nm n-GaAs layers embedded in undoped GaAs matrix are prepared by RIBER C21 solid-state molecular beam epitaxy system. The structure consists of a 30-nm undoped GaAs capping layer, a 50-nm Si-doped GaAs layer, and a 300-nm buffer layer grown on a semi-insulating GaAs substrate. Three samples with doping densities for the n-type GaAs 1×10^{18}, 5×10^{17}, and 1×10^{17} cm^{-3} are prepared, which are referred as Samples A, B, and C, respectively. The device is fabricated through the standard procedures including photolithography, wet etching, and metal evaporation using a thermal coater. The channel width is 20 μm with 7-μm trenches to separate drain or source and gate terminals. The channel length is 5 μm. The etching depth of the isolating trench is 750 nm, which has penetrated through the n-GaAs channels.

III. Results and Discussions

The room-temperature I_D–V_{GS} curves of the three devices with different n-GaAs doping densities are shown in Fig. 1(a). As shown in the figure, because of its highest doping density in the channel, Device A cannot be switched off at gate bias -10.0 V. With reduced 5×10^{17} cm^{-3} doping density, Device B has revealed standard transistor behaviors in the gate bias ranging from -10 to 5 V. For Device C, because of its lowest doping concentration in the n-GaAs layer, the lowest saturation drain current is observed. The results suggest that the main mechanism responsible for the current modulation of the devices is the population of surface mobile electrons [6]. The number of mobile surface electrons is highly correlated with the exposed GaAs area to the atmosphere. In this case, if the doping density is too high as the case of Device A,

Manuscript received March 20, 2013; accepted April 12, 2013. Date of current version May 20, 2013. This work was supported in part by the National Science Council, Taiwan under Grant NSC 101-2628-E-001-001 and Grant Nano-project founded by Academia Sinica, Taiwan. The review of this letter was arranged by Editor J.-M. Liu.

Y.-A. Liao and W.-H. Chang are with the Department of Electrophysics, National Chiao-Tung University, Hsinchu 300, Taiwan.

Y.-K. Chao is with the Institute of Optoelectronic Sciences, National Taiwan Ocean University, Keelung 20224, Taiwan.

J.-I. Chyi is with the Department of Electrical Engineering, National Central University, Jhongli, 32001, Taiwan.

W. H. Lin and S.-Y. Lin are with the Research Center for Applied Sciences, Academia Sinica, Taipei 11529, Taiwan (e-mail: shihyen@gate.sinica.edu.tw).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2013.2258456

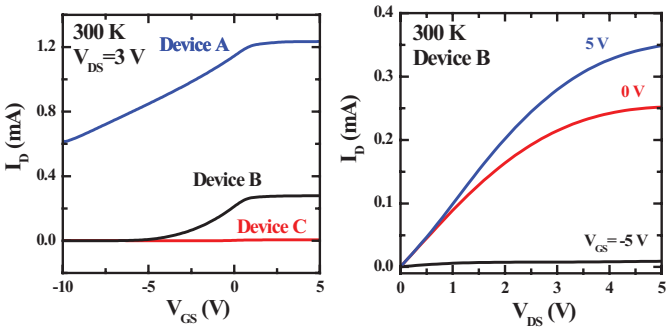

Fig. 1. (a) Room-temperature I_D–V_{GS} curves of Devices A, B, and C. (b) Room-temperature drain current I_D versus drain-source voltage V_{DS} curves of Device B at V_{GS} 5, 0, and −5 V.

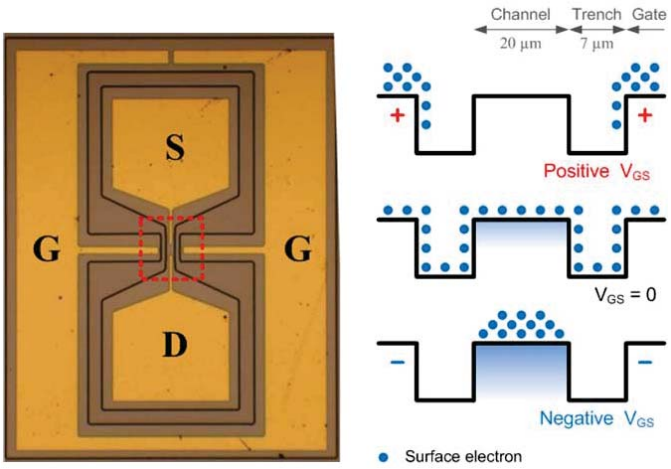

Fig. 2. Top-view picture and the schematic cross-sectional diagram of the IPGTs.

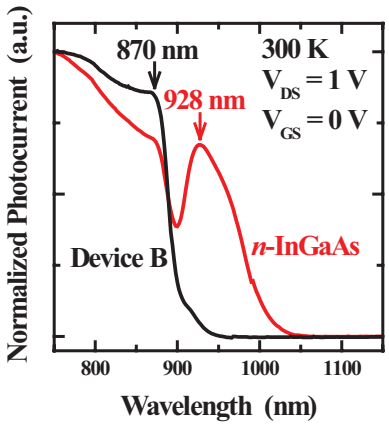

Fig. 3. Normalized photocurrents of Device B and another device with 20-nm $In_{0.1}Ga_{0.9}As$ channel n-type doped to 1×10^{18} cm^{-3} operated at $V_{DS} = 1$ V and $V_{GS} = 0$ V at room temperature.

the device will not be able to be switched off. On the other hand, the too low doping density as the case of Device C would result in depressed saturation drain currents. Therefore, a tradeoff between current modulation and saturation current should be done by optimizing the doping density in the n-GaAs channel.

In addition, Fig. 1(a) shows the drain current saturation occurred at $V_{GS} = 1.2$ V for Device B, which states that the channel is slightly depleted when no gate bias is applied. In this case, the positive gate bias would attract the surface electrons accumulated on the top of the channels such that the maximum drain current does not occurred at $V_{GS} = 0$ V. The room-temperature drain current I_D versus drain-source voltage V_{DS} curves of Device B at V_{GS} 5, 0, and −5 V are shown in Fig. 1(b). As shown in the figure, drain current saturation is observed for the device at higher drain-source voltages. The operation mechanisms of IPGTs are similar to the current flow in a sheet resistance with gate-controllable doping densities. In this case, the phenomenon should be attributed to the drift velocity saturation of semiconductors at high lateral electrical fields [7]. In addition, the figure shows the switchoff behavior of the device at an acceptable V_{GS} of −5 V considering its large channel width 20 μm. The results are consistent with the previous assumption that the channels are not depleted directly by the applied in-plane electric field. The population of mobile electrons is the main mechanism determining the ON–OFF behaviors of IPGTs.

To further explain the operation mechanisms of the devices, the top-view picture and the schematic cross-sectional diagram of the device are shown in Fig. 2. Considering the wide channel width and the low gate biases, the limited in-plane electric fields should not be the main mechanism responsible for the drain current modulation. The main mechanism should be the population of mobile surface electrons on the GaAs surface under different gate bias conditions. As shown in the figure, when negative biases are applied to the gate terminals, the mobile surface electrons will be repelled and accumulated on the top of the n-GaAs channels. Since the distance between the surface electrons and the channels is only 30 nm, the accumulated surface electrons could effectively deplete the n-GaAs channels. In this case, the drain current would be greatly depressed as the cases of Devices B and C. At $V_{GS} = 0$ V, the surface electrons should uniformly distribute on the GaAs surfaces. In the case, although part of the electrons in the channels will be depleted, significant drain currents could still be observed given high enough doping densities in the n-GaAs layers as the case of Devices A and B. When positive voltages are applied to the gate terminals, the mobile surface electrons will be attracted to the gate terminals. Hence, higher drain current are observed as the less surface electrons resident in the areas above the channel. This phenomenon is observed in Devices A and B since the maximum drain currents occur at $V_{GS} > 0$ V.

One of the possible applications of the IPGTs is in high-speed phototransistors. The operation speed of the detector is limited by the material mobility instead of the RC time constant of p-n junctions. With the uncovered channel area to provide large photon absorption region, optimized signal-to-noise ratios may be obtained by applying negative gate biases to depress the dark currents. The detection wavelengths may be extended to the near-infrared range by changing different materials as the channel. To investigate this possibility, another device is prepared by replacing the 50-nm n-GaAs channels in Devices A, B, and C with 20-nm $In_{0.1}Ga_{0.9}As$ channel

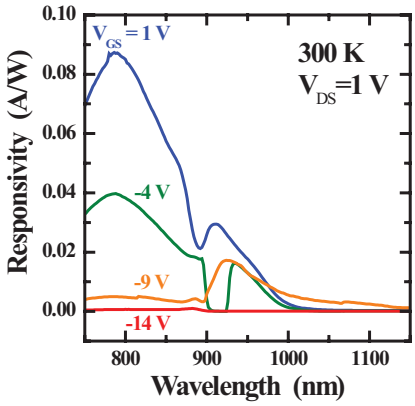

Fig. 4. Room-temperature spectral response curves of the device with 20-nm $In_{0.1}Ga_{0.9}As$ channel n-type doped to 1×10^{18} cm^{-3} operated at $V_{DS} = 1$ V and different gate biases.

n-type doped to 1×10^{18} cm^{-3}. The choice of thinner channel thickness is to avoid strain relaxation resulted from lattice-mismatched InGaAs layers grown on GaAs substrates. The normalized photocurrents of the device and Device B are shown in Fig. 3. The measurements conditions are $V_{DS} = 1$ V and $V_{GS} = 0$ V at room temperature. The photocurrent measurements are done by irradiating the devices with a chopped tungsten-halogen lamp light source by using an optical chopper. A Standard Research Systems SR830 lock-in preamplifier coupled with a SR570 current preamplifier is used to record the corresponding photocurrents of the devices. The drain and gate voltages are supplied by SR570 and the other common-ground power supply. For Device B, the cutoff absorption wavelength is ~870 nm, which is close to the GaAs bandgap at room temperature. The results demonstrated the potential of the IPGT architecture for photodetector applications. For the device with the n-InGaAs channel, except for the photocurrent corresponding to GaAs absorption, additional peak absorption at ~928 nm is observed. Although the results demonstrated the possibility of extended wavelength detection of IPGTs by changing the channel materials, the two separate absorption regions corresponding to GaAs and InGaAs suggest that the photocurrent does not come merely from the n-InGaAs channel.

To further investigate the operation mechanisms of the device with n-InGaAs channels, the spectral response curves of the device with a 20-nm n-$In_{0.1}Ga_{0.9}As$ channel operated under different gate biases are shown in Fig. 4. The results are obtained by calibrating the incident powers of the light source with a Thorlabs PM100D power meter. As shown in the figure, the responsivities of the device are one–two orders of magnitudes lower than the conventional InGaAs PIN diodes. A possible reason for this phenomenon is the thin absorption region of the device. Also shown in the figure is that with decreasing gate biases to -9 V, the photocurrent corresponding to the GaAs absorption will gradually disappear.

At $V_{GS} = -14$ V, the photocurrent corresponding to the InGaAs absorption will also disappear. The main device parameter changing with the gate biases is the amount of mobile surface electrons accumulated on the top of the channel. The results suggest that the photo-excited electrons in the top undoped 30-nm GaAs would still contribute to the observed photocurrents of the device. In this case, at $V_{GS} = -9$ V, although the electric field built by the accumulated surface electrons is still too weak to fully deplete the n-InGaAs channel, it is sufficient to deplete the top GaAs layer. With the gate bias further reduced to -14 V, the increasing accumulated surface electrons would build large electric field to deplete n-InGaAs channel. The results would be the first disappearance of photocurrents corresponding to GaAs absorption and then the other part to InGaAs absorption with decreasing gate biases. However, since the top GaAs layer is undoped, more detailed investigations should be done to explore how the photo-excited electrons in that layer would flow to the conducting InGaAs layer and contribute to the photocurrent.

IV. Conclusion

We investigated IPGTs with an n-GaAs sheet resistance and 20-μm channel widths. Well current modulation was observed for the sheet resistance with appreciate doping densities in the channel region. The phenomena is due to the channel electron depletion resulted from the population of the mobile surface electrons repelled to the top of the channel with negative gate biases. The photocurrent measurements demonstrated that employing IPGTs with sheet resistance can be an alternative approach for application of high-speed phototransistors.

References

[1] A. D. Wieck and K. Ploog, "In-plane-gated quantum wire transistor fabricated with directly written focused ion beams," *Appl. Phys. Lett.*, vol. 56, no. 10, pp. 928–930, 1990.

[2] J. Nieder, A. D. Wieck, P. Grambow, H. Lage, D. Heitmann, K. V. Klitzing, and K. Ploog, "One-dimensional lateral-field-effect transistor with trench gate-channel insulation," *Appl. Phys. Lett.*, vol. 57, no. 25, pp. 2695–2697, 1990.

[3] H. W. Schumacher, U. F. Keyser, U. Zeither, R. J. Haug, and K. Eberl, "Nanomachining of mesoscopic electronic devices using an atomic force microscope," *Appl. Phys. Lett.*, vol. 75, no. 8, pp. 1107–1109, 1999.

[4] T. H. Chung, W. H. Liao, and S. Y. Lin, "The fabrication of nano-mesas and nano-metal contacts by using atomic force microscopy lithography," *J. Appl. Phys.*, vol. 108, no. 9, pp. 094316-1–094316-5, 2010.

[5] T. H. Chung, S. H. Chen, W. H. Liao, and S. Y. Lin, "In-plane gate transistors fabricated by using atomic-force microscopy anode oxidation," *IEEE Electron Device Lett.*, vol. 31, no. 11, pp. 1227–1229, Nov. 2010.

[6] T. H. Chung, W. H. Lin, Y. K. Chao, S. W. Chang, and S. Y. Lin, "In-plane gate transistors with 40μm wide channel width," *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1129–1131, Aug. 2012.

[7] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. New York, NY, USA: Wiley, 2007, pp. 36–38.