Device and Circuit Performance Estimation of Junctionless Bulk FinFETs

Ming-Hung Han, Chun-Yen Chang, *Life Fellow, IEEE*, Hung-Bin Chen, Ya-Chi Cheng, and Yung-Chun Wu, *Member, IEEE*

***Abstract*— The design and characteristics of junctionless (JL) bulk FinFET devices and circuits are compared with the conventional inversion-mode (IM) bulk FinFET using 3-D quantum transport device simulation. The JL bulk FinFET shows better short channel characteristics, including drain-induced barrier lowering, subthreshold slope, and threshold voltage (V_{th}) roll-off characteristics at supply voltage (V_{DD}) 1 V. Analyses of electron density and electric field distributions in ON-state and OFF-state also show that the JL devices have better ON–OFF current ratios. Regarding design aspects, the effects of channel doping concentration (N_{ch}) and Fin height (H)/width (W) on device V_{th} are also compared. In addition, the V_{th} of the proposed JL bulk FinFET can be easily tuned by an additional parameter, substrate doping concentration (N_{sub}). Inverter performance and static random access memory (SRAM) circuit performance are also compared using a coupled device-circuit simulation. The high-to-low delay time (t_{HL}) and low-to-high delay time (t_{LH}) of the inverter with JL bulk FinFET are smaller than the inverter with IM bulk FinFET. The JL bulk FinFET SRAM cell also provides a similar static transfer characteristic to those of IM bulk FinFET SRAM cell, which show large potential in digital circuit application.**

***Index Terms*— 3-D simulation, FinFET, inverter circuit, junctionless, short channel, static random access memory (SRAM).**

I. Introduction

THE scaling of the channel lengths in conventional metal-oxide semiconductor field-effect transistors (FETs) shrinks to the order of nanometers; several critical challenges, such as the need to reduce short channel effect (SCE), to deliver a higher ON-current, to reduce power consumption, and to eliminate intrinsic parameter fluctuations, must be addressed [1]–[6]. Numerous approaches for addressing these issues have been introduced in the past decade. These include the use of high-k/metal-gate technology to suppress the direct tunneling current in gate oxides, to enhance mobility using strain, and to develop multigate structure such as FinFET and nanowire structures to reduce SCE [7]–[14]. Recently, the concept of the junctionless (JL) nanowire transistor, which contains a single doping species at the same level in its source, drain, and channel, is investigated [15]–[28]. The JL device is basically a gated resistor, that is, it is a resistor with a gate that controls the carrier density and hence the current flow. Normally, the JL device works like a low-resistance resistor, and the application of a gate voltage allows the semiconductor film of carriers to be depleted, thereby modulating its conductivity. Ideally, it should be possible to completely deplete the semiconductor film of carriers, in which case the resistance of the device approaches to infinite. The advantages of JL devices include: 1) avoidance of the use of an ultrashallow source/drain junction, which greatly simplifies the process flow; 2) low thermal budgets owing to implant activation anneal after gate-stack formation is eliminated; and 3) the current transport is in the bulk of the semiconductor, which reduces the impact of imperfect semiconductor/insulator interfaces. Although a JL device with bulk substrate, which provides the absence of an SOI wafer to lower the cost, and improves scalability and full compatibility with the industry standard bulk CMOS process flow, is also proposed [25]–[28], there still lacks a comprehensive study of both n-type and p-type Si bulk substrate JL devices in performance estimating and device design. Additionally, most of the studies focused on the device performance estimation of JL transistors, but few addressed the circuit application of such device.

This paper comprehensively investigates the device and circuit performances of JL bulk FinFET and compares it to the conventional inversion-mode (IM) bulk FinFET by using 3-D quantum transport device simulation. This paper is structured as follows. In Section II, the simulation method and the setting of the parameters for studying the characteristics of devices and circuits are introduced. In Section III, the performances of IM and JL devices and circuits are compared and design of the JL bulk FinFET devices is presented. Finally, Section IV summarizes the conclusion.

II. Simulation Methodology

Fig. 1(a) shows the structures of the simulated devices and the relevant parameters. The tested devices have an HfO_2 high-k gate oxide with an equivalent oxide thickness (EOT) of 1 nm, a gate length (L_g) of 15 nm, a Fin height (H) of 10 nm, a Fin

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M.-H. Han, C.-Y. Chang, and H.-B. Chen are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: minghunghan@gmail.com; cyc@mail.nctu.edu.tw; chenlays@hotmail.com).

Y.-C. Cheng and Y.-C. Wu are with the Department of Engineering and System Science, National Tsing Hua University, Hsinchu 300, Taiwan (e-mail: citygirl0831@hotmail.com; ycwu@ess.nthu.edu.tw).

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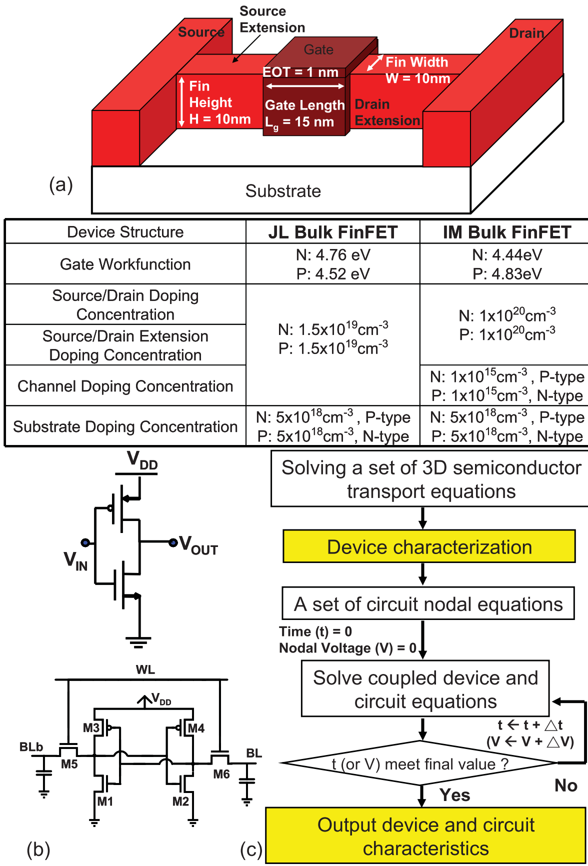

Device Structure	JL Bulk FinFET	IM Bulk FinFET
Gate Workfunction	N: 4.76 eV P: 4.52 eV	N: 4.44eV P: 4.83eV
Source/Drain Doping Concentration	N: 1.5×10^{19}cm^{-3} P: 1.5×10^{19}cm^{-3}	N: 1×10^{20}cm^{-3} P: 1×10^{20}cm^{-3}
Source/Drain Extension Doping Concentration		
Channel Doping Concentration		N: 1×10^{15}cm^{-3}, P-type P: 1×10^{15}cm^{-3}, N-type
Substrate Doping Concentration	N: 5×10^{18}cm^{-3}, P-type P: 5×10^{18}cm^{-3}, N-type	N: 5×10^{18}cm^{-3}, P-type P: 5×10^{18}cm^{-3}, N-type

Fig. 1. (a) Device structure and parameters of simulated JL bulk FinFET and IM bulk FinFET. (b) Inverter and SRAM circuit simulated in this paper. (c) Flowchart for the coupled device-circuit approach.

width (W) of 10 nm, and a source/drain extension length of 15 nm. The gate material is TiN with a work-function of 4.76 and 4.52 eV for n-type and p-type JL bulk FinFET, and 4.44 and 4.83 eV for n-type and p-type IM bulk FinFET, in which different work-functions can be tuned by Al incorporation [6], [29]–[32], as shown in Fig. 1(a). The doping concentrations in the source/drain/channel in both n-type and p-type JL bulk FinFETs are set to 1.5×10^{19} cm^{-3}. The opposite substrate doping type with 5×10^{18} cm^{-3} concentrations is used in the JL bulk FinFET, which can be obtained easily by the typical well-implantation process. The design of IM bulk FinFET is based on the prediction of the International Technology Roadmap for Semiconductors 2011 and fabricated devices proposed in [2] and [11]–[14]. In both n-type and p-type IM bulk FinFETs, the source/drain and source/drain extension doping concentrations are constant with 1×10^{20} cm^{-3}, and the channel doping is opposite type with 1×10^{15} cm^{-3} concentrations. No gate to source/drain extension overlaps is assumed; the effective channel length equals gate length to enable a fair comparison. A well doping with opposite type 5×10^{18} cm^{-3} is used in substrate to reduce SCE. To obtain accurate numerical results for a nanometer-scale device, the device is simulated by solving 3-D quantum transport equations using the commercial tool, the Synopsys Sentaurus device [33]. In quantum transport equations, a density gradient model is used in the simulation, as listed below [33], [34]

$$n = N_C F_{1/2}\left(\frac{E_{F,n} - E_C - \Lambda_n}{kT_n}\right)$$
$$\Lambda_n = -\frac{\gamma \hbar^2}{12 m_n}\left[\nabla^2 \ln n + \frac{1}{2}(\nabla \ln n)^2\right] \quad (1)$$

where n is electron concentration, N_C is effective density of states of conduction band (E_C), $F_{1/2}$ is Fermi–Dirac integral, m_n is effective mass of electron, and T_n is electron temperature. The corresponding parameters are also used for holes. The mobility model used in device simulation is according to Mathiessen's rule, expressed as follows:

$$\frac{1}{\mu} = \frac{D}{\mu_{\text{surf_aps}}} + \frac{D}{\mu_{\text{surf_rs}}} + \frac{1}{\mu_{\text{bulk_dop}}} \quad (2)$$

where $D = \exp(x/l_{\text{crit}})$, x is the distance from the interface, and l_{crit} is a fitting parameter. The mobility consists of three parts: 1) surface acoustic phonon scattering ($\mu_{\text{surf_aps}}$); 2) surface roughness scattering ($\mu_{\text{surf_rs}}$); and 3) bulk mobility with doping-dependent modification ($\mu_{\text{bulk_dop}}$). The details are described in [33] and [35]. Additionally, the bandgap narrowing model, the band-to-band tunneling model, and Shockley–Read–Hall recombination with the doping-dependent model are also considered. The direct tunneling model is not utilized because high-k/metal-gate technology is used. Fig. 1(b) shows the CMOS inverter and static random access memory (SRAM) used as test circuits to estimate circuit characteristics. As no well-established compact model of JL devices is available, a coupled device-circuit simulation approach is used [36]; Fig. 1(c) shows the flow chart. First, an initial guess for bias condition of device is assumed, and the device characteristics in the test circuit are estimated by solving the device transport equations. The obtained result is the initial guess for the coupled device-circuit simulation. The nodal equations of the tested circuits are then formulated according to the Kirchhoff current law. Coupling the formulated circuit equations to the device transport equations obtains a large matrix containing both circuit and device equations. Solving the large matrix then obtains the device and circuit characteristics simultaneously. The coupled simulation is solved iteratively until the solution converges in each bias condition and each time step.

III. Results and Discussion

A. Device Characteristics Comparison

Fig. 2(a) shows the plots of the $I_{\text{ds}} - V_{\text{gs}}$ curves of the n-type and p-type devices of interest. For a fair comparison, linear threshold voltages (V_{th}) are adjusted to about ±300 mV by tuning gate work-function. Without applying channel engineering or strain technology, the proposed n-type JL bulk FinFET has an ON-current of 322 μA/μm (at $V_{\text{gs}} = 1$ V, $V_{\text{ds}} = 1$ V) and an OFF-current of 1.7 nA/μm (at $V_{\text{gs}} = 0$ V, $V_{\text{ds}} = 1$ V). The subthreshold slope (SS) is 73.1 mV/dec, and drain-induced barrier lowering (DIBL), defined as the difference in V_{th} between $V_{\text{ds}} = 0.05$ V and $V_{\text{ds}} = 1$ V, equals only 40.4 mV. The p-type JL bulk FinFET performs similarly. In Fig. 2(b), the plot of V_{th} roll-off characteristics shows that,

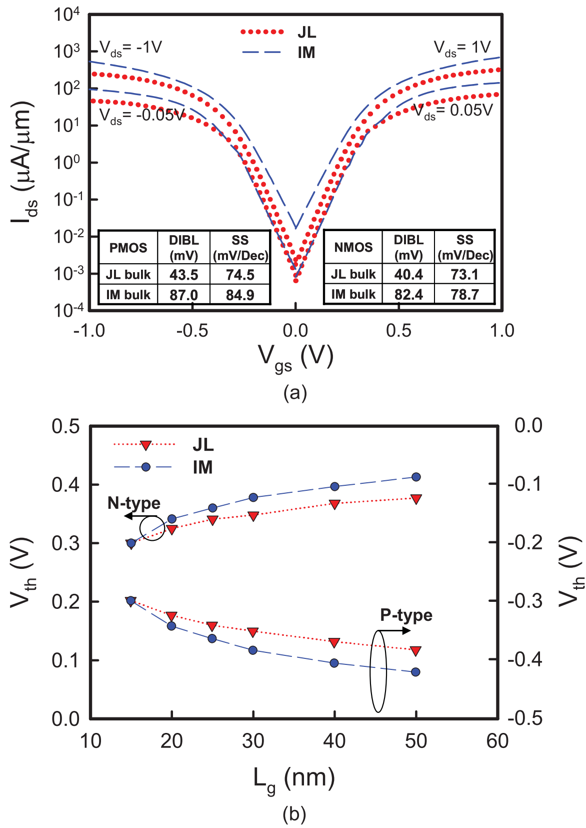

Fig. 2. (a) $I_{ds} - V_{gs}$ curves of the n-type and p-type transistors; the SS and DIBL are shown in the inset. (b) Threshold voltage (V_{th}) of n-type and p-type transistors for different L_g.

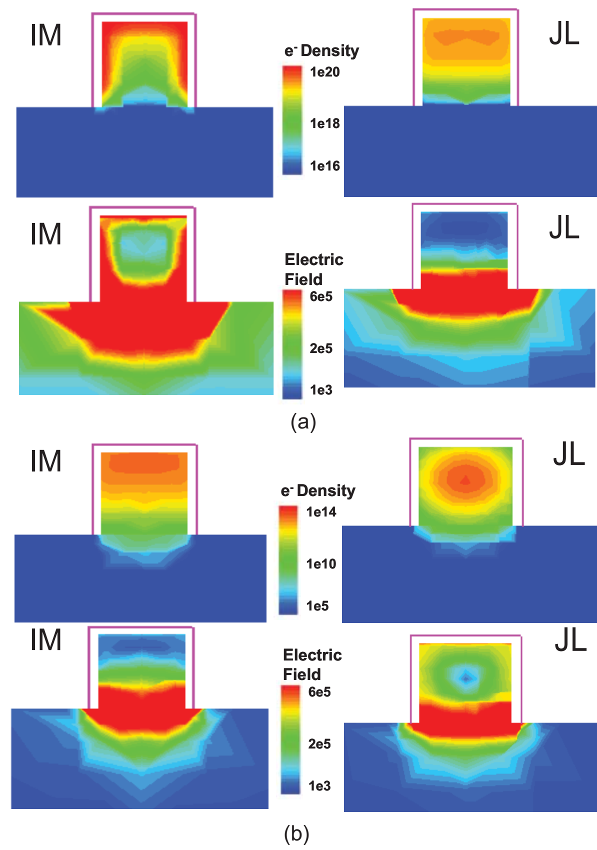

Fig. 3. Electron density (top) and electric field (bottom) distributions in the channel when n-type JL and IM devices operate at (a) ON-state ($V_{gs} = 1$ V) and (b) OFF-state ($V_{gs} = 0$ V) with $L_g = 15$ nm, $H = W = 10$ nm, and EOT = 1 nm.

when gate length is reduced from 50 to 15 nm, the V_{th} shifts in the JL device is only 80 mV, which is significantly smaller than in IM devices. Comparisons of the simulated DIBL and SS [Fig. 2(a) inset] and V_{th} roll-off [Fig. 2(b)] show that the short channel characteristics of the JL devices are superior to those of the IM devices at gate lengths L_g as low as 15 nm. The reason for these simulation results can be explained by the charge sharing model [1]. In conventional IM devices, some of the depletion charge is balanced by the source and drain at the end of the channel. The severity of this phenomenon, which is known as the SCE, increases when the channel length is short. In contrast, JL devices do not have a concentration gradient between the source/channel and channel/drain to produce a junction. Therefore, the charge is controlled by the gate alone, which substantially reduces SCEs. To compare conduction mechanisms, Fig. 3 shows the electron density and electric field distributions in the center of the channel region of JL and IM devices at ON-state ($V_{gs} = 1$ V) and OFF-state ($V_{gs} = 0$ V). Fig. 3(a) shows that, although the maximum electron density is higher in the IM device than in the JL device, the peak electron density and the peak electric field are both located at the silicon/oxide interface in IM devices. In contrast, the electrons are concentrated in the middle of the channel region in JL bulk FinFET because they are repelled by the electric field at the channel/oxide interface [16]–[18], [24]–[28], and the electric field is smallest in the same region. Hence, the electrons in JL devices exhibit bulk conduction, which prevents surface scattering and high field degradation of the current. The ON current of JL device is smaller than that of IM device because of the lower doping used ($\sim 10^{19}$ cm^{-3}, compared with 10^{20} cm^{-3} used in IM device) and induced lower electron density in JL device, as shown in Figs. 2(a) and 3(a). Additionally, if we consider real device fabrication, the doping level in JL device may have relatively large series resistance. However, the ON current and resistance can be improved by using raised source/drain, additional doping in source/drain regions, and accumulation-mode operation [11]–[14], [19]. Fig. 3(b) shows the plots of the characteristics of the devices in OFF-state, which substantially differ from those in ON-state. Although the electron densities are concentrated in the middle of the channel in both JL and IM devices, the much higher electric field and lower electron density in the JL devices block the current conduction and improve OFF-current. Fig. 4 shows the output performance of the JL bulk FinFET; the characteristics are quite similar to those of conventional IM MOSFETs [1]–[14].

B. Device Design

Fig. 5 shows the V_{th} and ON–OFF current ratio of the JL bulk FinFET at varying channel doping concentrations N_{ch}. As drain current is directly proportional to channel doping concentration [16], and as channel doping also affects the

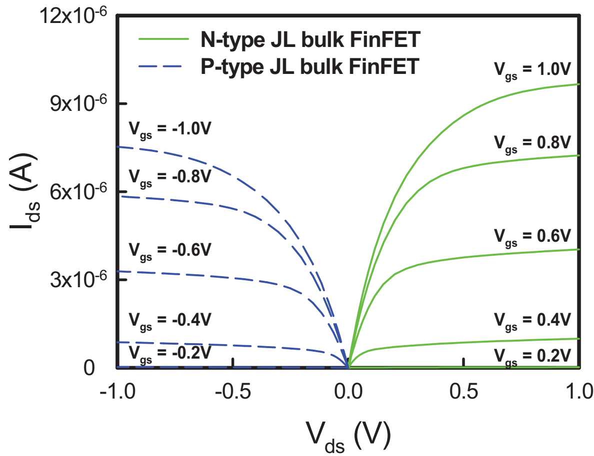

Fig. 4. $I_{ds} - V_{ds}$ curves of the n-type and p-type JL bulk FinFET with $L_g = 15$ nm, $H = W = 10$ nm, EOT = 1 nm, $N_{ch} = 1.5 \times 10^{19}$ cm^{-3}, and $N_{sub} = 5 \times 10^{18}$ cm^{-3}.

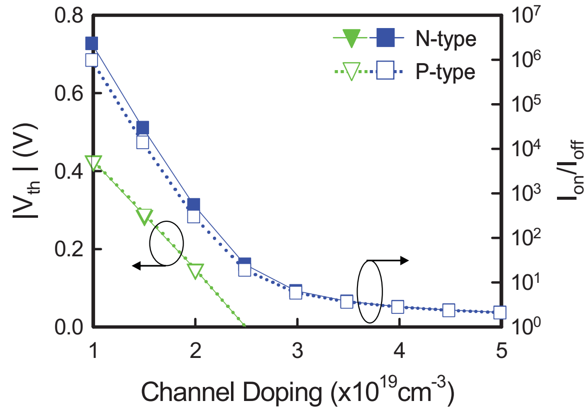

Fig. 5. Threshold voltages and ON/OFF current ratios of JL bulk FinFET for different channel doping concentrations with $H = W = 10$ nm and $N_{sub} = 5 \times 10^{18}$ cm^{-3}.

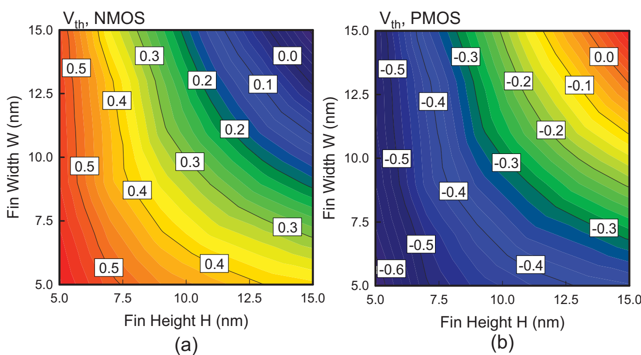

Fig. 6. Contour plot of threshold voltages of (a) n-type and (b) p-type JL bulk FinFET for different Fin heights H and Fin widths W with $N_{ch} = 1.5 \times 10^{19}$ cm^{-3} and $N_{sub} = 5 \times 10^{18}$ cm^{-3}.

size of depletion region of channel/substrate junction and vary the effective channel thickness in JL bulk FinFET, the N_{ch} substantially affects the device performance, the increase of N_{ch} degrades I_{ON}/I_{OFF} although it improves ON current and resistance. When N_{ch} exceeds 2.5×10^{19} cm^{-3}, the threshold voltage becomes negative, and the ON–OFF current

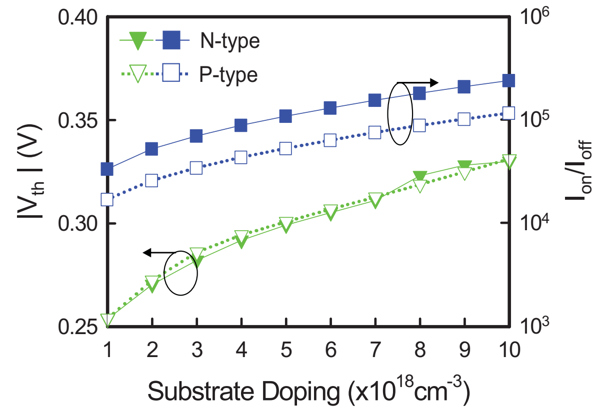

Fig. 7. Threshold voltages and ON/OFF current ratios of JL bulk FinFET for different substrate doping with $H = W = 10$ nm and $N_{ch} = 1.5 \times 10^{19}$ cm^{-3}.

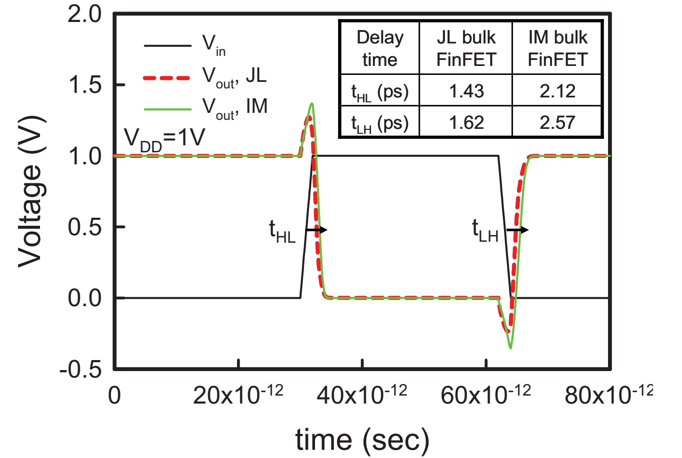

Fig. 8. Timing characteristics of JL and IM bulk FinFET CMOS inverter circuits, in which the definitions of high-to-low delay time (t_{HL}) and low-to high delay time (t_{LH}) are indicated. The inset shows the extracted t_{HL} and t_{LH} values.

ratio decreases to <100. Therefore, the JL bulk FinFET design should carefully consider N_{ch}. Fig. 6 shows the contour plots of V_{th} as a function of Fin height H and Fin width W in both n-type and p-type JL bulk FinFETs. As the channel region needs fully depleted when the JL devices are turned off, device performance can be effectively tuned by adjusting channel thickness and width. The V_{th} changes from 0.6 to 0 V and from −0.6 to 0 V in n-type and p-type JL devices, respectively, when H and W are increased from 5 to 15 nm. Additionally, once one of H or W keeps small, the V_{th} becomes insensitive to the other factor. Fig. 7 shows the V_{th} and ON–OFF current ratio of the JL bulk FinFET versus substrate doping concentration (N_{sub}). Like channel doping concentration, Fin height/width, gate oxide thickness, and gate workfunction [1]–[32], V_{th} is easily tunable by adjusting the N_{sub}. The range of modulation of V_{th} is ∼30% as the N_{sub} varies from 10^{18} cm^{-3} to 10^{19} cm^{-3}.

C. Circuit Performances

Fig. 8 shows the timing characteristics of the input and output signals of an inverter circuit and defines the

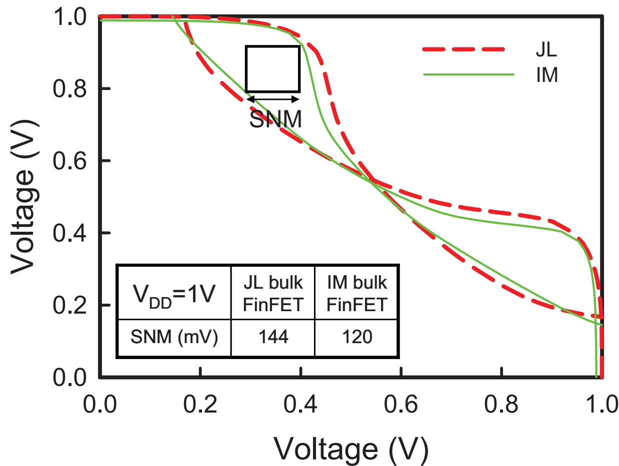

Fig. 9. Static transfer characteristic curves of JL and IM bulk FinFET 6T-SRAM cells, in which the definition of SNM is indicated. Inset: extracted SNM values.

high-to-low delay time (t_{HL}) and low-to-high delay time (t_{LH}). When input signal transits from low voltage to high voltage, the n-type device starts to turn on, thus the t_{HL} is dependent on the threshold voltage and the intrinsic delay of the n-type devices. Similarly, t_{LH} is dependent on the threshold voltage and intrinsic delay in p-type devices when the input signal transits from high voltage to low voltage. Therefore, the t_{HL} is usually smaller than t_{LH}. As the physics of intrinsic delay substantially differ between JL and IM devices [16], neither inverter can be considered superior. However, using the parameter setting in this paper, the simulated JL bulk FinFET inverter circuit shows strikingly similar timing characteristics, and the t_{HL} and t_{LH} values in the JL CMOS inverter are smaller than those observed in the IM CMOS inverter. To evaluate potential applications of the JL digital circuit, the performance of an SRAM cell is compared between a JL bulk FinFET and an IM bulk FinFET SRAM cell. Generally, an SRAM cell operates in three different states: 1) standby; 2) write; and 3) read. Due to the cell being most vulnerable to noise during read operations [37]–[39], the stability of a SRAM cell is often related to the static noise margin (SNM). The SNM is defined as the highest dc noise voltage at which the cell state does not flip during a read access. Fig. 9 shows the static transfer characteristics and the definition of SNM. The JL bulk FinFET SRAM also shows static transfer characteristics very similar to those of the IM bulk FinFET SRAM. Moreover, the SNM of 144 mV observed in the JL bulk FinFET SRAM is better than the 120 mV observed in the IM.

IV. Conclusion

The 3-D quantum transport device simulations of electrical and physical characteristics in this paper showed that the JL bulk FinFET had a higher ON–OFF current ratio and better short channel characteristics compared with the conventional IM bulk FinFET. The electron density and electric field distributions in ON-state indicated that the JL bulk FinFET exhibited bulk conduction and did not suffer from surface scattering and high field degradation. On the other hand, as the JL device had a much higher electric field and lower electron density in OFF-state compared with the IM device, the JL device had a lower OFF-current. Regarding device design, the device characteristic changes with channel doping concentration (N_{ch}), Fin height (H), Fin width (W), and substrate doping concentration (N_{sub}) were performed. As N_{ch} directly affected current and effective Fin height in the proposed JL bulk FinFET, N_{ch} significantly affected V_{th} and ON–OFF current ratio. The V_{th} of the JL device was also dependent on H and W because of the full depletion condition to turn off the device. Once H was sufficiently thin, the effect of W decreased, and vice versa. Additionally, the JL bulk FinFET offered an additional design parameter, the N_{sub}, for controlling device performance. The circuit performance comparisons showed that the inverter and SRAM cell made by JL bulk FinFET had similar timing and static transfer characteristics, comparable to those with the IM device and had potential applications in digital circuit design.

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Ming-Hung Han is currently pursuing the Ph.D. degree within the Institute of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan.

His current research interests include modeling and simulation of semiconductor nanodevices and circuits, high voltage power CMOS, and Si-based solar cells.

Chun-Yen Chang (F'88–LF'05) has contributed to the fields of microelectronics, microwave, and optoelectronics, including the establishment of the first Si planar center in 1964 at National Chiao Tung University, Hsinchu, Taiwan, the first MOSFET in 1966, and the first LED in 1970.

Hung-Bin Chen is currently pursuing the Ph.D. degree within the Institute of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan.

His current research interests include junctionless nanodevices, high voltage power CMOS, and flash memory.

Ya-Chi Cheng is currently pursuing the Ph.D. degree with the Department of Engineering and System Science, National Tsang Hua University, Hsinchu, Taiwan.

Her current research interests include fabrication and simulation in junctionless thin-film transistors and gate-all-around nanodevices.

Yung-Chun Wu (M'11) is an Associate Professor with the Department of Engineering and System Science, National Tsing Hua University, Hsinchu, Taiwan. His current research interests include nanoelectronic devices, flash memory devices, and solar cells.