Epitaxial Germanium on SOI Substrate and Its Application of Fabricating High I_{ON}/I_{OFF} Ratio Ge FinFETs

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***Abstract*— Integrating germanium (Ge) thin film on silicon-on-insulator (SOI) substrate and fabricating Ge fin field-effect transistors (FinFETs) are demonstrated in this paper. Directly grown Ge film on a high-resistivity thin SOI substrate provides a good platform for fabricating advanced Ge devices. The SOI structure could effectively suppress junction leakage; therefore, high I_{ON}/I_{OFF} ratio ($\sim 5 \times 10^5$, at $V_D = 0.1$ V) of the drain current is achieved. Tri-gate structure provides better short-channel control abilities for the Ge FinFETs, and the drain-induced barrier lowering and threshold voltage (V_{TH}) shift can be maintained at the level of ~110 mV/V and ~0.1 V, respectively, for Ge n-channel FinFET with $L_{channel} = 120$ nm and $W_{Fin} = 40$ nm. Multifin Ge FinFET with $L_{channel} = 170$ nm and $W_{Fin} = 50$ nm is also illustrated. Both $N-$ and $P-$FinFETs possess high I_{ON}/I_{OFF} ratio over 10^4. Besides, the subthreshold swing could be reduced around 25% after forming gas annealing.**

***Index Terms*— Epitaxial Ge on silicon on-insulator (SOI) substrates, fin field-effect transistors (FinFETs), forming gas annealing, Ge CMOS, germanium.**

I. Introduction

HIGH-MOBILITY materials have been widely investigated to pursue the feasibility of them replacing traditional Si CMOS technology. Ge has been considered a promising candidate for fabricating CMOS devices due to its higher electron and hole mobilities than Si. Besides, lower operating voltage can be used because of its lower energy bandgap ($E_g = 0.66$ eV), allowing for green electronic applications. High-performance Ge planar n- and p-MOSFETs with different passivation methods were demonstrated in the previous reports [1]–[4]. Source current (I_S) always depicts better OFF-state behavior than drain current (I_D). This is due to the fact that Ge possesses lower bandgap and high intrinsic carrier concentration (n_i). Both contribute to the reverse junction leakage as the drain is biased. To overcome this problem, an SOI-like structure such as the germanium-on-insulator (GeOI) prepared by condensation [5], [6] and smart-cut [9] method could effectively suppress the bulk leakage current. By fabricating Ge MOSFETs on GeOI substrates, excellent OFF-state behavior and high rectifying ratio of I_D could be achieved [5]–[8]. Furthermore, high intrinsic dielectric constant of Ge ($\kappa \sim 16.1$) will make ultrasmall Ge channel devices suffer from severe short-channel effects (SCEs) and then increase the difficulties for the sub-14-nm applications. Therefore, the device structure with strong SCE immunity shall be employed. For Si technology, ultrathin-body SOI FETs and tri-gate FETs are known to be able to effectively suppress the SCEs. But, ultrathin-body SOI FETs need a much thinner Si channel than tri-gate (or Fin) FETs to have the same sound electrostatic integrity in the channel. So, the tri-gate structure is more suitable for the sub-14-nm devices. For the Ge devices, p-channel gate-all-around FETs [10]–[12] and FinFETs [13], [14] have been realized with well-behaved short-channel performance. Nevertheless, the n-channel FETs encountered more difficulties, including larger interface states [15], dopant loss [16], and Fermi-level pinning [17].

In this paper, we integrate the Ge thin film on the thin SOI substrate by epitaxial method and fabricated Ge FinFETs with the gate-last processing. The nFET of $L_{channel} = 120$ nm and $W_{Fin} = 40$ nm depicts high I_{ON}/I_{OFF} ratio ($> 10^5$), excellent drain-induced barrier lowering (DIBL) (110 mV/V), and subthreshold swing (SS) (144 mV/dec). The dependence of SCE on fin width is briefly discussed. The forming gas annealing (FGA) effect on the improvement of device characteristic is also presented. Finally, the multifin Ge n- and p-FinFETs are also fabricated with a 50-nm fin width. The results demonstrate the possibility of realizing advanced Ge CMOS structure on the Si-based platform.

II. Experimental

A. Substrate Preparation

(100)-oriented SOI substrates with 10- to 20-ohm-cm resistivity were used as the starting substrates. The 50-nm Si device layer was trimmed down to 20 nm by wet oxidation

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and wet etching. Then, the wafers were cleaned by standard cleaning with HF-last process and loaded into an ultrahigh-vacuum CVD chamber immediately. The 60-nm Ge layer was grown at 420 °C with germane (GeH_4) precursor. Last, *in situ* postdeposition annealing (PDA) was performed at 900 °C for 10 min at high vacuum ambient (5×10^{-9} torr) to reduce dislocations. X-ray diffraction spectrum and transmission electron microscopy (TEM) were used to identify the crystallinity of the grown Ge thin films.

B. Device Fabrication

Ge FinFETs were accomplished by the gate-last processing. A 60-cycle atomic layer deposition (ALD)-Al_2O_3 layer was deposited as the screen oxide to avoid the channeling effect, and the source/drain implantation regions were defined by e-beam lithography, which indicates that there was a dummy photoresist gate between the source and drain. The channel length (L_{channel}) was defined as the dummy photoresist gate length. Phosphorus (for NFET) and boron (for PFET) were implanted at a dose of 1×10^{15} cm^{-2} and an implant energy of 20 keV. After removing the photoresist and screen oxide, a 100-nm plasma-enhanced CVD (PECVD)-SiO_2 was deposited, and the dopant activation was carried out. The n-type and p-type dopants were activated at 600° C for 10 s and at 500 °C for 10 s in N_2 ambient, respectively.

Active area, including the fin region, was also defined by e-beam lithography. Then, the PECVD oxide was used as a hard mask, and Ge active area was etched by Cl_2/HBr-based reactive ion etching (RIE). In order to eliminate the damages created during RIE, the wafer was carefully dipped in dilute H_2O_2 (1:10) for 5 s. After removing the capped oxide, the wafer was cleaned by dilute HF (1:20) to reduce the native oxide, and a thermal GeO_2 was grown at 520 °C for 30 s in O_2 ambient as the surface passivation layer. A 60-cycle ALD-Al_2O_3 layer was used as the gate dielectric, followed by the gate region lithography and Pt/Ti deposition. Therefore, the metal gate definition was performed by the lift-off process. At the back-end of line, source drain contacts were defined, and Pt/Ti was used as the contact metal.

Fig. 1(a) shows the schematic structure of the Ge FinFET. The Al_2O_3/GeO_2 bilayer dielectric with Pt/Ti lift-off gate was used as the gate stack. The source/drain area was approximately ~650 μm^2 each side. In order to reduce the mismatch during the lithography alignment, the implantation region was set to be larger than the active area. Similarly, the gate-to-source/drain overlap was 300 nm on each side to make sure that the metal gate could align to the channel region. Fig. 1(c) shows the cross-sectional TEM image of Ge FinFET along A-A' in Fig. 1(a). The Ge fin height (H_{Fin}) was 60-nm, which equaled the epitaxial film thickness, and the fin width (W_{Fin}) was around ~40 nm. A 20-nm Si seed layer was still under the Ge fin. The thickness of Al_2O_3 and GeO_2 was ~5.5 and ~1.5 nm, respectively.

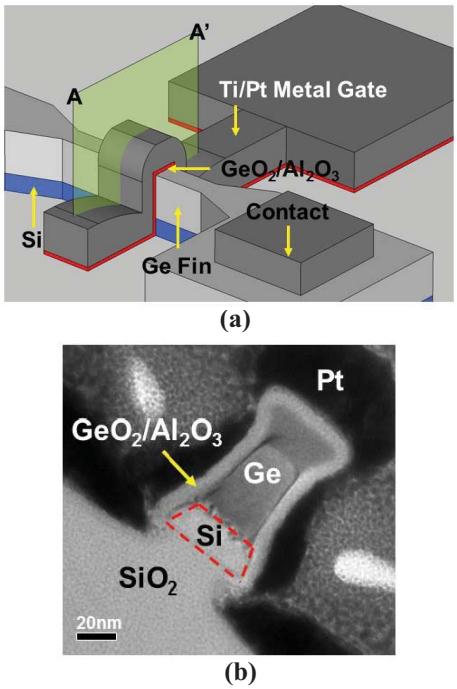

Fig. 1. (a) Schematic view of the Ge FinFET structure fabricated and (b) cross-sectional TEM image of the Ge fin along A-A' in (a). Fin height of Ge region is 60 nm, and the fin width is 40 nm. The gate stack is $Pt/Ti/Al_2O_3/GeO_2$.

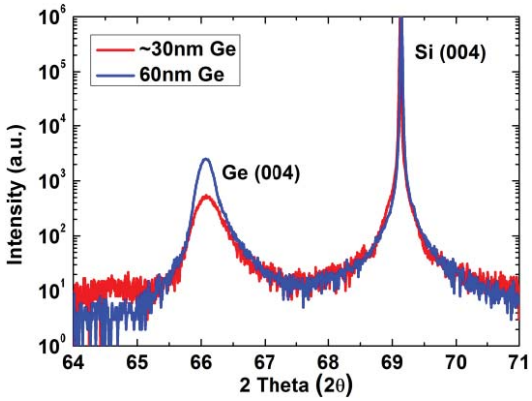

Fig. 2. XRD spectra of ~30- and 60-nm epitaxial Ge films on the SOI substrates.

III. Results and Discussion

A. Characterization of the Epitaxial Ge Film

Fig. 2 shows the XRD analysis of the epitaxial Ge on the SOI substrates with two different thicknesses. We can see that the Ge (004) peak is near 66°, since the substrates were annealed at 900 °C at the final step, indicating that the strain in the film is fully relaxed during the high-temperature PDA. The XRD intensity will be affected by the film thickness; therefore, the Ge (004) peak is higher in the 60-nm epitaxial Ge film. The full-width at half-maximum value of the 60-nm Ge film is 0.228, which is lower than that of the 30-nm Ge film (0.365). This means the 60-nm Ge film has better crystallinity.

In order to further identify the quality of the epitaxial films, the TEM was used. The cross-sectional TEM images are shown in Fig. 3(a)–(c). We can see that the film roughness is deteriorated for the 30-nm Ge film. The maximum thickness variation is around 20 nm. We speculate that the strain in the films is large after the epitaxial Ge growth. During PDA, the strain tends to relax through surface rippling. However, thicker

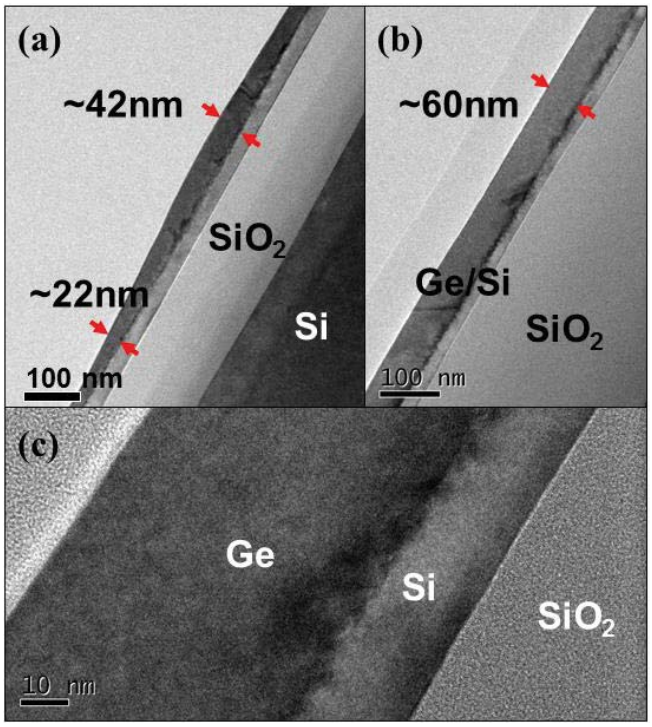

Fig. 3. Cross-sectinal TEM images of the (a) ~30-nm Ge film and (b) 60-nm Ge film. (c) Zoom-in TEM image of the 60-nm Ge sample.

Ge films can avoid this problem as shown in Fig. 3(b)–(c), because the strain relaxes mainly through the formation of misfit dislocations. This can be confirmed by the 60-nm Ge film. It shows a flat surface, and relatively large density of misfit dislocations are observed at the Ge/Si interface. For device fabrication, we use the 60-nm Ge film to perform the Ge FinFETs process.

B. Electrical Properties of the n-Channel Ge FinFET

The I_D–V_G transfer characteristics of the n-channel Ge FinFET with an L_{channel} of ~120 nm and W_{Fin} of ~40 nm are shown in Fig. 4(a). The drain current is normalized by 160 nm ($2 \times H_{\text{Fin}} + W_{\text{Fin}}$). Although the S/D areas (650 μm^2) are very large in our device, we can see that the GeOI structure is capable of effectively suppressing the junction leakage current. Therefore, very high $I_{\text{ON}}/I_{\text{OFF}}$ ratio for I_D is obtained; ~5 $\times 10^5$ at $V_D = 0.1$ V and ~10^4 at $V_D = 1$ V. The threshold voltage is 1.1 V because we used a high-work-function metal (Pt, Φ_m ~5.6 eV) as the gate electrode. The Ge channel was undoped, and the S/D doping was directly performed by the heavily doped S/D without extensions or halo implant. The tri-gate architecture does provide better gate-control ability, and the DIBL is only ~110 mV/V. The SS is 144 mV/dec. In the OFF-state region, the leakage increases with raising the negative gate and drain biases, indicating that the origin is the gate-induced drain leakage. The overlapping area is large in our device; however, for general gate-last processing, the replacement gate technique could efficiently reduce the overlapping area. Fig. 4(b) shows the I_D–V_D output characteristics. The driving current is 120 μA/μm at $V_G - V_{\text{TH}} = 0.9$ V and $V_D = 1$ V.

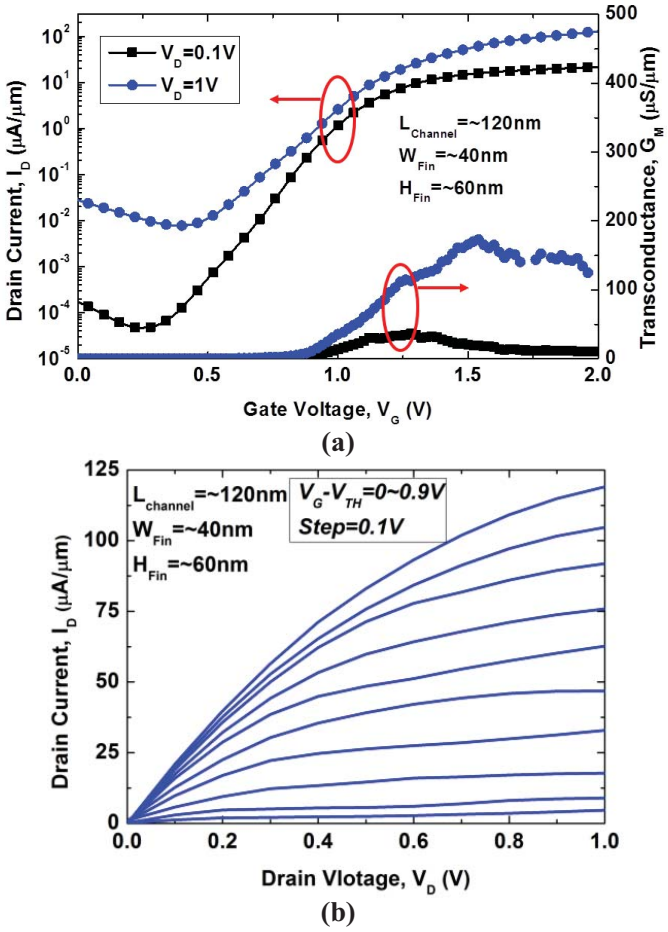

Fig. 4. (a) I_D-V_G transfer characteristics and (b) I_D-V_D output characteristics of the n-channel Ge FinFET with L_{channel} of ~120 nm and W_{Fin} of ~40 nm.

The V_{TH} shift, DIBL, and SS versus channel length for the Ge FinFETs with 40- to 100-nm fin width are shown in Fig. 5(a)–(c). For $W_{\text{Fin}} \geqq 60$ nm, the V_{TH} shift and DIBL increase obviously when L_{channel} <170 nm, indicating that the gate loses control toward the channel. In contrast, reducing fin width to 40 nm could provide better electrostatic control, and the V_{TH} shift and DIBL can keep at the level of ~0.1 V and ~110 mV/V for $L_{\text{channel}} = 120$ nm, respectively. The SS for the long-channel devices is approximately 150 mV/dec, independent of the fin width. Nevertheless, the OFF-state leakage current significantly increases for the short-channel devices, degrading the SS as $W_{\text{Fin}} \geqq 60$ nm. But, as $W_{\text{Fin}} =$ 40 nm, the subthreshold leakage current can be suppressed, hence the SS does not degrade obviously for the devices with L_{channel} <170 nm. Based on these results, further improvement in SCEs could be expected as the fin width is reduced to less than 40 nm.

For the planar MOSFETs, the driving current could be boosted by increasing the effective channel width. Similarly, the effective channel width of FinFETs could be enlarged by increasing the number of fins. Fig. 6 shows the top-view SEM image of the multifin structure after the active area definition. The fin width is ~ 50 nm, and the fin pitch is 400 nm. The electrical characteristics of the five-fin n- and p-channel Ge

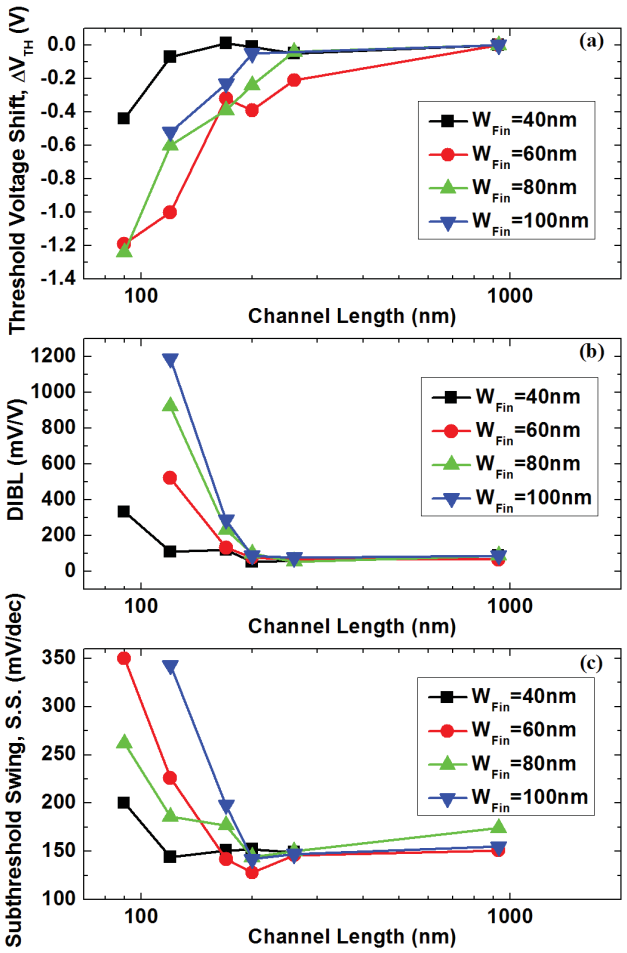

Fig. 5. (a) Threshold shift, (b) drain-induced barrier lowering, and (c) subthreshold swing versus channel length for the n-channel Ge FinFETs with 40 ~ 100 nm fin width.

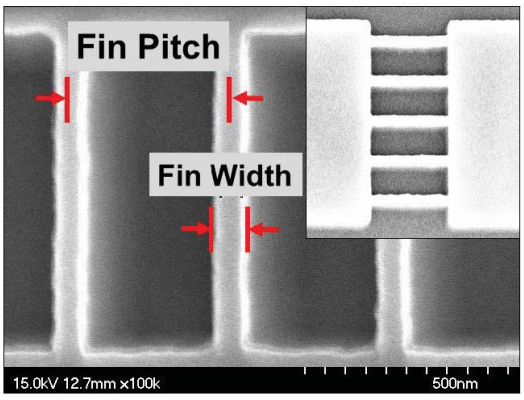

Fig. 6. SEM image of the multifin structure. The fin pitch and fin width are 400 and ~ 50 nm, respectively.

FinFETs with $L_{\text{channel}} =\sim 170$ nm are shown in Fig. 7(a) and (b), respectively. Obviously, the output current is boosted by increasing the number of fins, and the rectifying ratios of both the n- and p-channel FinFETs exceed 10^4 at $V_D = 0.1$ V. However, the p-FinFET depicts higher SS (~237 mV/dec), revealing higher subthreshold leakage current, and the junction should be further improved to suppress the OFF-state leakage.

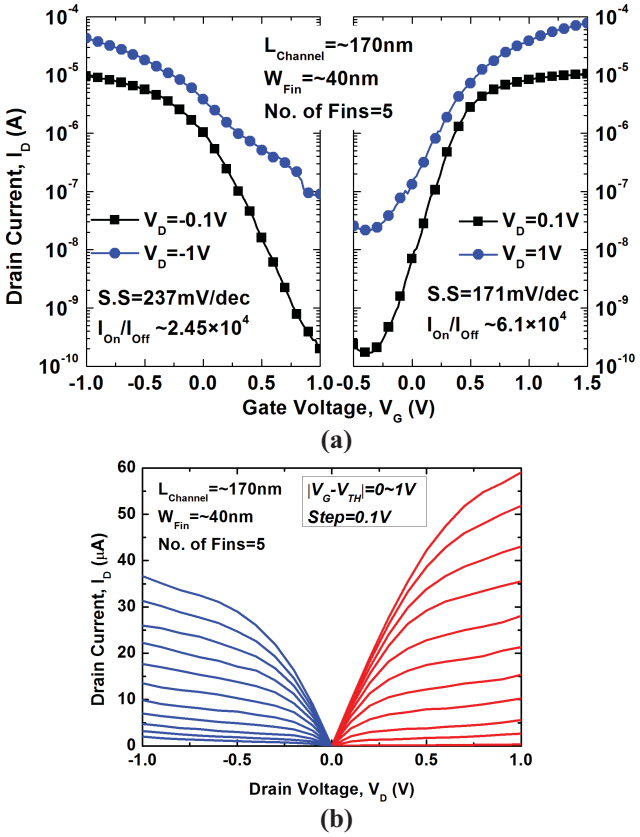

Fig. 7. (a) I_D–V_G transfer characteristics and (b) I_D–V_D output characteristics of the five-fin n- and p-channel Ge FinFETs with an L_{channel} of ~ 170 nm and W_{Fin} of ~ 50 nm.

Fig. 7(b) shows the I_D–V_G of n- and p-channel Ge FinFETs. The epitaxial Ge on the SOI substrate provides well-behaved output electrical characteristics of Ge FinFETs.

C. Characteristics With Forming Gas Annealing

Fig. 8 shows the I_D–V_G transfer characteristics of the n-channel Ge FinFET with an L_{channel} of ~90 nm and W_{Fin} of ~40 nm before and after FGA (H_2:N_2 = 5:100) at 300 °C for 30 min. The driving current is decreased after FGA, indicating that the total resistance increases and the output performance degrades, as shown in the inset of Fig. 8. Since the S/D region is directly exposed to RTA ambient without intermetal dielectric protection, phosphorus might get out-diffused during FGA, inducing the S/D series resistance degradation.

Passivating the dangling bonds at the oxide/Ge interface by hydrogen is insufficient, which has already been demonstrated in the previous reports by both theoretical [18] and experimental results [19]. However, the SS is decreased around 20%–25% after FGA in our experiment. We roughly calculated the interface states density (D_{it}) by the subthreshold swing equation of the double-gate devices [20], [21], and the D_{it} is around ~7×10^{12} cm^{-2}–eV^{-1} before FGA and ~4.8×10^{12} cm^{-2}–eV^{-1} after FGA. The interface state density is higher than that of the RTO-grown GeO_2 passivated planar MOSFET [22]. We consider that the {110} sidewall orienta-

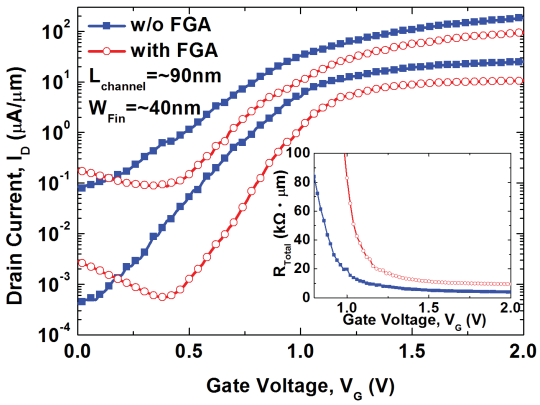

Fig. 8. I_D-V_G transfer characteristics of the n-channel Ge FinFET with an L_{channel} of ~90 nm and W_{Fin} of ~ 40 nm before and after FGA. Inset: Total resistance of the device before and after FGA.

tion of the channel surface is not the main origin of causing higher amount of D_{it}, because it has been proved that the D_{it} of GeO_2 passivated MOSCap is independent of the surface orientation of Ge [23]. The GeO_2 passivation layer was grown by *ex situ* RTO, and the GeO_2 layer may be damaged by the moisture before loading the samples into the ALD system. Besides, R. Zhang *et al.* [24] reported that thin GeO_2 will be damaged severely during ALD deposition process, causing the dramatic increase of D_{it}. We speculate that these damages can be repaired by FGA. Moreover, FGA could increase more Ge^{4+} oxidation states to reduce D_{it} [25]. Therefore, we regard that FGA is still a promising procedure for fabricating Ge MOSFET with the GeO_2 passivation process.

IV. Conclusion

We integrated the epitaxial Ge films on the SOI substrate and fabricated the gate-last n-channel Ge FinFET. By optimizing the epitaxial Ge thickness on the SOI substrate, flat and relatively low-dislocation-density Ge film could be obtained. By employing the high-quality Ge on the SOI substrate, the SOI-like structure could effectively suppress the junction leakage, hence a high rectifying ratio of drain current could be achieved. However, the high series resistance of the Ge NMOSFET, which was induced by the Fermi-level pinning and dopant out-diffusion, degraded the output characteristic, and this is still the main challenge for improving the driving current. The tri-gate structure also plays an important role in controlling the SCEs. Shrinking the Ge fin width could improve the electrostatic control, and the V_{TH} shift, DIBL, and SS could still maintain at the same level when the $L_{\text{channel}} = 120$ nm. Multifin Ge n- and p-channel FinFETs with well-behaved electrical outputs were also demonstrated. The effect of FGA was also examined in this paper. The SS is improved after FGA, indicating that the D_{it} was reduced from 7×10^{12} to 4.8×10^{12} $\text{cm}^{-2}\text{-eV}^{-1}$ after FGA. Based on our demonstration, we believe Ge is still one of the candidates for the next-generation CMOS technology.

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References

[1] J. Mitard, B. De Jaeger, F. E. Leys, G. Hellings, K. Martens, G. Eneman, D. P. Brunco, R. Loo, J. C. Lin, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken, C. H. Yu, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, and M. M. Heyns, "Record ION/IOFF performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2008, pp. 873–876.

[2] C. H. Lee, T. Nishimura, N. Saido, K. Nagashio, K. Kita, and A. Toriumi, "Record-high electron mobility in Ge n-MOSFETs exceeding Si universality," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2009, pp. 457–460.

[3] R. Zhang, N. Taoka, P. C. Huang, M. Takenaka, and S. Takagi, "1-nm-thick EOT high mobility Ge n-and p-MOSFETs with ultrathin GeOx/Ge MOS interfaces fabricated by plasma post oxidation," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2011, pp. 642–645.

[4] D. Kuzum, T. Krishnamohan, A. Nainani, S. Yun, P. A. Pianetta, H. S. P. Wong, and K. C. Saraswat, "High-mobility Ge N-MOSFETs and mobility degradation mechanisms," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 59–66, Jan. 2011.

[5] L. Hutin, C. Le Royer, J. F. Damlencourt, J. M. Hartmann, H. Grampeix, V. Mazzocchi, C. Tabone, B. Previtali, A. Pouydebasque, M. Vinet, and O. Faynot, "GeOI pMOSFETs scaled down to 30-nm gate length with record OFF-state current," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 234–236, Mar. 2010.

[6] C. Le Royer, B. Vincent, L. Clavelier, J.-F. Damlencourt, C. Tabone, P. Batude, D. Blachier, R. Truche, Y. Campidelli, Q. T. Nguyen, S. Cristoloveanu, S. Soliveres, G. Le Carval, F. Boulanger, T. Billon, D. Bensahel, and S. Deleonibus, "High-κ and metal gate pMOSFETs on GeOI obtained by Ge enrichment: Analysis of ON and OFF performances," *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 635–637, Jun. 2008.

[7] B. Liu, X. Gong, G. Han, P. S. Y. Lim, Y. Tong, Q. Zhou, Y. Yang, N. Daval, C. Veytizou, D. Delprat, B.-Y. Nguyen, and Y.-C. Yeo, "High-performance germanium Ω-gate MuGFET with schottky-barrier nickel germanide source/drain and low-temperature disilane-passivated Gate Stack," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1336–1338, Oct. 2012.

[8] J. Feng, G. Thareja, M. Kobayashi, S. Chen, A. Poon, Y. Bai, P. B. Griffin, S. S. Wong, Y. Nishi, and J. D. Plummer, "High-performance gate-all-around GeOI p-MOSFETs fabricated by rapid melt growth using plasma nitridation and ALD Al_2O_3 gate dielectric and self-aligned NiGe contacts," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 805–807, Jul. 2008.

[9] C. Deguet, L. Sanchez, T. Akatsu, F. Allibert, J. Dechamp, F. Madeira, F. Mazen, A. Tauzin, V. Loup, C. Richtarch, D. Mercier, T. Signamarcheix, F. Letertre, B. Depuydt, and N. Kernevez, "Fabrication and characterization of 200 mm germanium-on-insulator (GeOI) substrates made from bulk germanium," *Electron. Lett.*, vol. 42, no. 7, pp. 415–417, Mar. 2006.

[10] J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan, and C. M. Lieber, "Ge/Si nanowire heterostructures as high-performance field-effect transistors," *Nature*, vol. 441, pp. 489–493, May 2006.

[11] L. Zhang, R. Tu, and H. Dai, "Parallel core-shell metal-dielectric-semiconductor germanium nanowires for high-current surround-gate field-effect transistors," *Nano Lett.*, vol. 6, no. 12, pp. 2785–2789, Dec. 2006.

[12] S.-H. Hsu, C.-L. Chu, W.-H. Tu, Y.-C. Fu, P.-J. Sung, H.-C. Chang, Y.-T. Chen, L.-Y. Cho, W. Hsu, G.-L. Luo, C. W. Liu, C. Hu, and F.-L. Yang, "Nearly defect-free Ge gate-all-around FETs on Si substrates," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2011, pp. 825–828.

[13] J. Feng, R. Woo, S. Chen, Y. Liu, P. B. Griffin, and J. D. Plummer, "P-channel germanium FinFET based on rapid melt growth," *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 637–639, Jul. 2007.

[14] C.-W. Chen, C.-T. Chung, G.-L. Luo, and C.-H. Chien, "Body-tied germanium FinFETs directly on a silicon substrate," *IEEE Electron Device Lett.*, vol. 33, no. 12, pp. 1678–1680, Dec. 2012.

[15] K. Martens, C. C. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, "On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 547–556, Feb. 2008.

[16] A. Satta, T. Janssens, T. Clarysse, E. Simoen, M. Meuris, A. Benedetti, I. Hoflijk, B. De Jaeger, C. Demeurisse, and W. Vandervorst, "P implantation doping of Ge: Diffusion, activation, and recrystallization," *J. Vacuum Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 24, no. 1, pp. 494–498, Jan. 2006.
[17] A. Dimoulas, P. Tsipas, A. Sotiropoulos, and E. K. Evangelou, "Fermi-level pinning and charge neutrality level in germanium," *Appl. Phys. Lett.*, vol. 89, no. 25, p. 252110, Dec. 2006
[18] J. R. Weber, A. Janotti, P. Rinke, and C. G. van de Walle, "Dangling-bond defects and hydrogen passivation in germanium," *Appl. Phys. Lett.*, vol. 91, no. 14, p. 142101, Oct. 2007.
[19] V. V. Afanas'ev, Y. G. Fedorenko, and A. Stesmans, "Interface traps and dangling bonds defects in (100)Ge/HfO_2," *Appl. Phys. Lett.*, vol. 87, no. 3, p. 032107, Jul. 2005.
[20] D. J. Wouters, J. P. Colinge, and H. E. Maes, "Subthreshold slope in thin-film SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 37, no. 9, pp. 2022–2033, Sep. 1990.
[21] P. Francis, A. Terao, D. Flandre, and F. Van de Wiele, "Modeling of ultrathin double-gate nMOS/SOI transistors," *IEEE Trans. Electron Devices*, vol. 41, no. 5, pp. 715–720, May 1994.
[22] M. Jamil, J. Oh, M. Ramon, S. Kaur, P. Majhi, E. Tutuc, and S. K. Banerjee, "High mobility TaN/Al_2O_3/Ge (111) nMOSFETs with RTO grown passivation layer," *IEEE Electron Device Lett.*, vol. 31, no. 11, pp. 1208–1210, Nov. 2010.
[23] T. Sasada, Y. Nakakita, M. Takenaka, and S. Takagi, "Surface orientation dependence of interface properties of GeO_2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation," *J. Appl. Phys.*, vol. 106, no. 7, pp. 073716-1–073716-7, Oct. 2009.
[24] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, "Suppression of ALD-induced degradation of Ge MOS interface properties by low power plasma nitridation of GeO_2," *J. Electrochem. Soc.*, vol. 158, no. 8, pp. G178–G184, Jun. 2011.
[25] Y. Oshima, Y. Sun, D. Kuzum, T. Sugawara, K. C. Saraswat, P. Pianetta, and P. C. McIntyre, "Chemical bonding, interfaces, and defects in hafnium oxide/germanium oxynitride gate stacks on Ge(100)," *J. Electrochem. Soc.*, vol. 155, no. 12, pp. G304–G309, Oct. 2008.

Cheng-Ting Chung, photograph and biography are not available at the time of publication.

Che-Wei Chen, photograph and biography are not available at the time of publication.

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