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Sloped-Gate Voltage Method for Improving Measurement of Poly-Si Nanowire FET in Aqueous Environment

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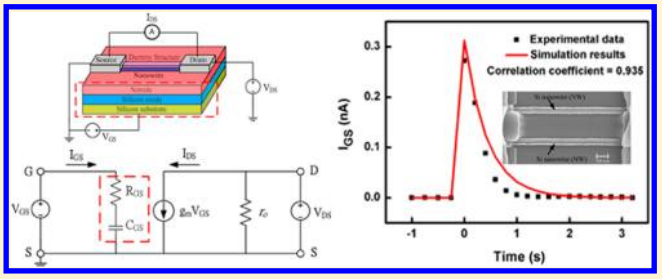
Supporting Information

ABSTRACT: Nanowire field-effect transistors are suited to study the activity of biomolecules in bionanotechnology. The changes of biomolecules process are efficiently affected the charge at the nanowire surface; thus, the electrical characterization of NW-FET is changed. Although NW-FET is a well-known device in bioapplications, however, the intrinsic electrical characterization of NW-FET effect on real electrical measurement is not well studied. We present herein a novel measurement method to avoid errors in electrical characteristic of nanowire field-effect transistors. A physical model is developed to explore the effect of the leakage current, which is influenced by the charging effect of an equivalent capacitor in a NW-FET. We also present a sloped-gate voltage method to reduce the effect of equivalent capacitor in air, liquid, and phosphate buffered solution. The application of the sloped-gate voltage method significantly increases the stability of electrical characterization measurements. This method can also be easily applied to biosensing experiments.



INTRODUCTION

Biological sensors based on semiconductor nanowire field-effect transistors (NW-FETs)[1−9] hold great potential for detecting tiny amounts of charged biomolecules and are promising for applications in the area of bionanotechnology. While NWs are applied as NW-FET biosensors, NW is connected to two electrodes to form a current channel, with a gate electrode on the top or bottom of the NW to conduct gate voltage as the typical FET device. Because of ultrasensitive, label-free, and real-time response, the NW-FET biosensors can be used to detect DNA molecules,[10−17] pH,[18,19] gas molecules,[20] proteins,[21] and single virus particles.[22]

According to the principle of FETs, the gate voltage modulates the electron flow in the channel between the source and the drain. The nanowire acts as an electron bridge between the drain and the source. The identification of biotargets is based on a small change in induced electric signals through the environmental variation around the surface of the NW-FET device, where the gate voltage is applied in the subthreshold regime.[23] Because of the difficulty of measuring small electrical signals (of the order under nanovolts or nanoamperes) and extracting data from the environmental disturbance mixed signals, appropriate electrical measurements and signal analysis methods are critical in biosensing experiments.

The accuracy of electrical measurements with FETs is affected by leakage current generated by the charging effect of a capacitor that appears across the gate oxide, in which the gate oxide serves as an insulator between gate and channel. This leakage current may significantly influence NW-FET because they operate in the femtoampere (fA) to nanoampere (nA) range. This paper reports a new method for NW-FET to avoid gate oxide current leakage problem. The proposed method uses a sloped variation in the gate voltage to reduce the potential difference between the gate and the source of an NW-FET. This leads to a more stable electrical characteristic measurement, and data obtained at different times after varying the gate voltage show the potential of using NW-FET in future applications. We verify by experiment that the proposed method achieves accurate results with stable performance.

EXPERIMENTAL DEVICE AND METHODS

The n-type polycrystalline silicon (poly-Si) NW-FETs are fabricated by a fully complementary metal-oxide-semiconductor-compatible (CMOS-compatible) process at the National Nano Device Laboratory in Hsinchu, Taiwan. The Si substrate consisted of a 100 nm silicon oxide (SiO_2) layer coated with a 50 nm silicon nitride (Si_3N_4) layer. A 1600 nm long, 500 nm wide SiO_2 dummy structure was fabricated on the substrate. A 1000 nm thick α-Si layer was deposited on the substrate and subjected to annealing at 600 °C to transform α-Si into poly-Si.

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The poly-Si NWs with source and drain (S/D) contacts were then created using photolithography and plasma etching. The S/D contacts were estivated by a 2000 nm thick SiO_2 layer to prevent current leakage.[18] Figure 1a shows our poly-Si NW

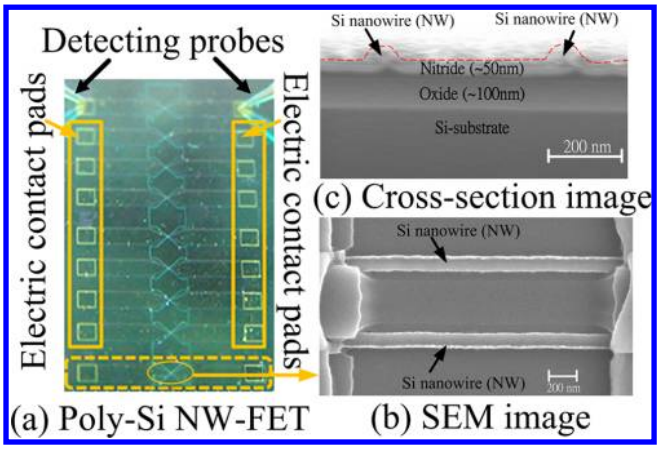

Figure 1. (a) Poly-Si NW-FETs with detecting probes. Inside the regions defined by an orange solid line and dashed line are the electric contact pads and one NW-FET device, respectively. The nanowire region is circled expanded as shown in (b). Top-view SEM image of a poly-Si NW-FET with a 200 nm scale bar. Cross-section structure of a poly-Si NW-FET device shown in (c). The nitride layer is ~50 nm, and the oxide layer is ~100 nm.

FETs and the electric contact pads in the orange line serve as sources and drains. Inside the orange dashed line is one of the NW-FET devices. In our measurement system, the signals from NW-FET device were collected by the two detecting probes. These two probes can be also easily moved to make different NW-FET measurements. Figure 1b shows the SEM top-view image of a poly-Si NW structure which is consisted of two parallel poly-Si NW of ~1600 nm length. The poly-Si NW-FET has two nanowires in each device; one of the NW is the dummy structure. The cross-section structure with NW-FET device is showed in Figure 1c.

In the NW-FET device, the current I_S from the source terminal is based on the applied drain-to-source voltage V_{DS} and modified by the applied gate voltage V_{GS}. All the measurements of the poly-Si NW-FETs were under back-gating conditions in this study. Figure 2 shows I_S versus V_{GS} characteristics of a poly-Si NW-FET, for V_{DS} = 0.1 V and V_{GS} varying from −1 to 3 V with a 0.2 V step. The electrical

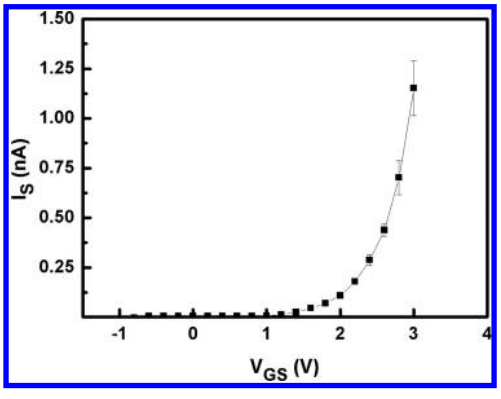

Figure 2. Measurement of current I_S with the gate-source voltage V_{GS} switched from −1 to 3 V.

properties of the poly-Si NW-FET exhibit threshold voltage of V_{th} ~ 2.16 V, subthreshold slope of S ~ 0.84 V/decade, and field effect mobility of μ ~ 225 cm^2/V s. Figure 3 shows I_S−V_{DS}

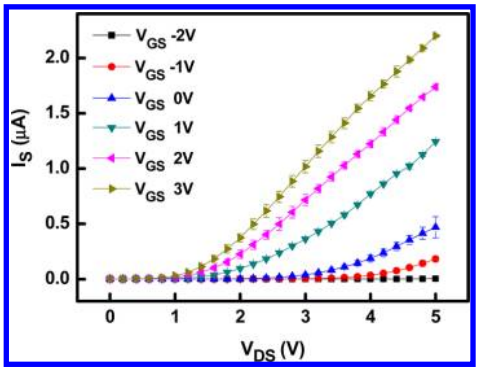

Figure 3. I_S vs V_{DS} measurement for various values of V_{GS}.

curves for V_{GS} varying from −2 to 3 V. The device exhibits typical metal-oxide-semiconductor field effect transistor (MOSFET) behavior, and the electronic properties of the poly-Si NW-FETs are well described by the conventional MOSFET theory. The experiments in this study reveal that current increases with increasing back-gate voltage V_{GS} superposed on forward V_{DS} in the NW-FET device. This characteristic also indicates the n-type-semiconductor nature of the device.

The measurement processes of the poly-Si NW-FETs were in an electromagnetic isolated probe station to reduce electromagnetic interference. All experimental results were obtained with measurement system included a high-precision source measure unit (PXI-4132, National Instrument) and a low-noise current preamplifier (SR570, Stanford Research Systems). These measurements of electric properties of the poly-Si NW-FETs were performed in air (room temperature, 45% humidity) under well-controlled conditions.

RESULTS AND DISCUSSION

The real-time responses of the source current (I_S) of the poly-Si NW-FET was investigated in the atmosphere. The back-gate voltage V_{GS} was stepped up from 0 to 2.5 V in 0.5 V increments, with each step lasting ~5 s. During the step lasting time interval, I_S was measured by our measurement system. The results described that I_S increased in conjunction with V_{GS}, as shown in Figure 4. When the V_{GS} was 0.5 and 1 V, the original current (I_{DS}) was lower than the peak current and the

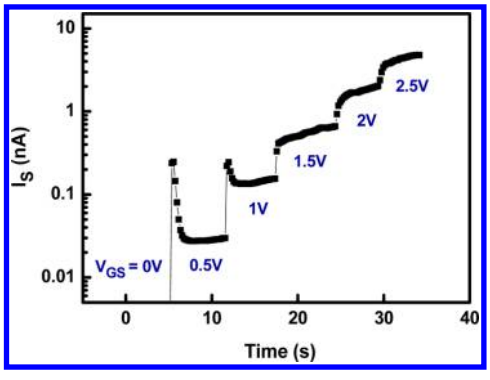

Figure 4. Temporal response of I_S as V_{GS} is stepped up from 0 to 2.5 V in 0.5 V increments.

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peak would be measured. As the V_{GS} was higher than 1.5 V, the original current (I_{DS}) would cover the peak current and the I_{DS} current would make main contribution to data measurement. However, the spike of I_S were observed for the V_{GS} steps from 0 to 0.5 V and from 0.5 to 1 V.

At the same time, the peaks of gate-to-source current (I_{GS}) in response to switching V_{GS} were also monitored in Figure 5. The

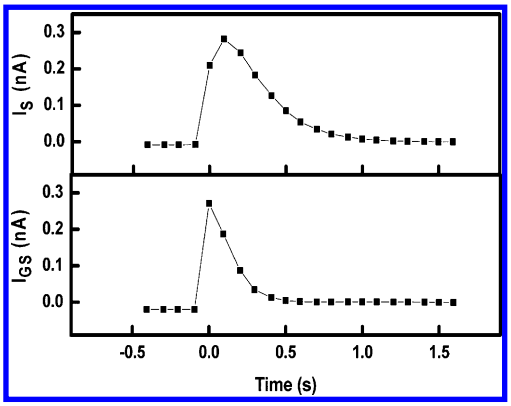

Figure 5. A comparison between I_S and I_{GS} after V_{GS} is switched from 0 to 0.5 V.

peak of I_{GS} could be interpreted as minimal leakage current due to V_{GS} through the dielectric interface to the drain and source channel. Furthermore, the minimal leakage ~0.3 nA would cause I_S bursting phenomenon at low gate voltage but would be stopped while gate voltage V_{GS} up to 1.5 V. Although the leakage current from the back-gate voltage was covered for larger I_S, this event can affect the accuracy of poly-Si NW-FET measurements for biosensing applications because ultrahigh sensitivity is dependent on small electronic signal measurement.

The origin of this I_{DS} spike has been attributed to be the charging effect of a capacitor because the structure between source and gate in the poly-Si NW-FET is similar to a capacitor. For interpreting the bursting phenomenon clearly, a physical model, an equivalent transformation model of electric circuit of a n-type NW-FET, is given in Figure 6, where G is back gate, D is drain, S is source, V_{GS} is the back-gate voltage, R_{GS} is the equivalent resistance, C_{GS} is the equivalent capacitance, g_m is the transconductance of the device, r_o is the output impedance, and V_{DS} is the drain-to-source voltage. In the physical model, the drain-to-source current (I_{DS}) can be described by the MOSFET theory as follows[21−24]

$$I_{DS} = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{th})V_{DS} \approx g_m V_{GS} \quad (1)$$

where n is the charge-carrier effective mobility, W is the gate width, L is the gate length, C_{ox} is the gate oxide capacitance of the NW-FET unit area, and V_{th} is the threshold voltage. The V_{GS} was applied to the Si substrate, which consisted of a silicon dioxide (SiO_2) layer and a silicon nitride (Si_3N_4) layer. Although no leakage current I_{GS} through the dielectric layers was expected, experimental results show that leakage current I_{GS} was nonzero during V_{GS} switching. Hence, these dielectric layers between source and gate can be described a simple series RC circuit. To analyze this equivalent circuit quantitatively, Kirchhoff's loop rule is applied, and the response of I_{GS} is expressed as

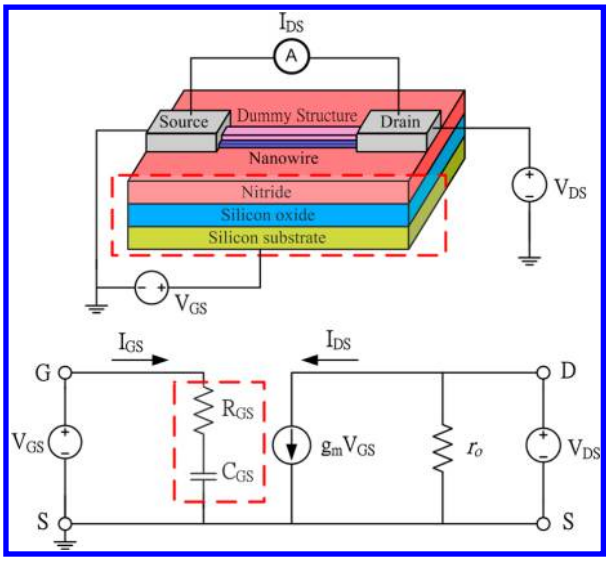

Figure 6. Equivalent circuit model of the NW-FET. R_{GS} and C_{GS} are the equivalent resistance and capacitance in the proposed physical model for the back-gate NW-FET structure, which is boxed in the red dashed line in the schematic above the circuit diagram. G is back gate, D is drain, S is source, V_{GS} is the back-gate voltage, g_m is the transconductance of the device, r_o is the output impedance, and V_{DS} is the drain-to-source voltage.

$$I_{GS} = \frac{V_{GS}}{R_{GS}} - \frac{q}{R_{GS}C_{GS}} \quad (2)$$

where I_{GS} is replaced by dq/dt. Then $q(t)$ can be evaluated as

$$q(t) = V_{GS}C_{GS}\{1 - \exp[-t/(R_{GS}C_{GS})]\} \quad (3)$$

Then the current through the back gate substrate is obtained by

$$I_{GS}(t) = \frac{V_{GS}}{R_{GS}} \exp[-t/(R_{GS}C_{GS})] \quad (4)$$

The source current $I_S(t)$ consists of two components. One is the leakage current $I_{GS}(t)$ produced by the charging effect of a capacitor, and the other one is the drain-source current (I_{DS}) produced by the drain-to-source voltage (V_{DS}). The source current can be expressed as

$$I_S(t) = I_{GS} + I_{DS} = \frac{V_{GS}}{R_{GS}} \exp[-t/(R_{GS}C_{GS})] + g_m V_{GS} \quad (5)$$

This physical model indicates that current signal I_S will be contaminated with leakage current I_{GS} soon after V_{GS} is switched on or changed. The measured current signal I_S would be dominated by real channel current between drain and source long after switching V_{GS}. Typically, the efficiency of the leakage current would fade out while $t \gg R_{GS}C_{GS}$. Figure 7 shows that the experimental results are well reproduced by the simulation using the physical model outlined above; the correlation coefficient for the fit is ~0.9354. The experimental results fitted with eq 4 were extracted $R_{GS} \approx 1.6$ GΩ and $C_{GS} \approx 0.27$ pF for V_{GS} switching from 0 to 0.5 V and with $V_{DS} = 0.1$ V. This physical model can therefore be used to explain the I_S spike phenomenon for measurements done while switching V_{GS} at low gate voltage.

According to previous discussions, the simplest method to avoid the interference of leakage current (I_{GS}) is applying appropriate time lag before collecting I_S data in the biosensing

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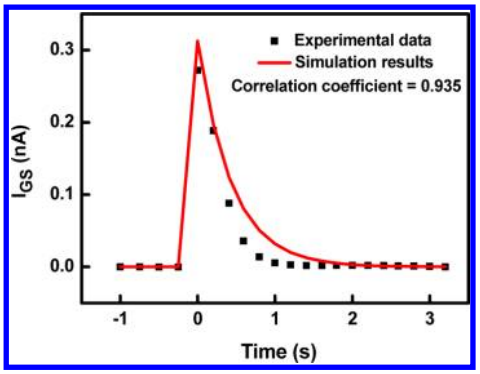

Figure 7. Experimentally measured I_{GS} for V_{GS} switched from 0 to 0.5 V state fit (red line) with eq 4.

experiment. However, equivalent resistance and capacitance of the NW-FET will differ after semiconductor processing; determining the required time lag to reach stable state of I_S becomes difficult. To avoid the charging effect of the capacitance in the NW-FET, the sloped-gate voltage method was used to the I_S measurement in Figure 8. On the basis of eq

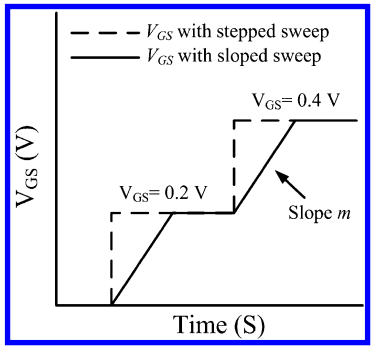

Figure 8. Slope modification used in V_{GS} switching from 0.2 to 0.4 V.

4, I_{GS} is proportioned to V_{GS}. In general, the V_{GS} sweep was applied a step function in V_{GS} switching (dotted line in Figure 8). Here the step V_{GS} in common use was modified as a sloped V_{GS} changing (solid line in Figure 8) to reduce the gate voltage different under Δt. Therefore, V_{GS} was slowly stepped up to measure I_S independently of V_{GS}. The applied potential difference between the poly-Si NW-FET source and gate was sequentially increased V_{GS} to the experimentally required value.

NW-FET devices are usually used to detect biosignal variances in a liquid environment. Therefore, the experiments of I_S measurement results compared without sloped-gate voltage method to with the method in PB (phosphate buffer, 10 mM) solution in Figure 9. After V_{GS} was switched from 0.2 to 0.4 V, the results shown in Figure 9a were acquired without adjusting the V_{GS} slope m (step function), and Figure 9b shows results for I_S with the slope adjusted to m = 0.04. The corresponding variances σ of different operating conditions in I_S are 1.12×10^{-10} and 1.783×10^{-11}, respectively. The corresponding variances σ is defined by the standard deviation of the averaged I_S to interpret the variance of measurement of I_S. The σ is represented by (6) as

$$\sigma = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(X_{\text{time}} - \mu_{\text{time}})} \tag{6}$$

where

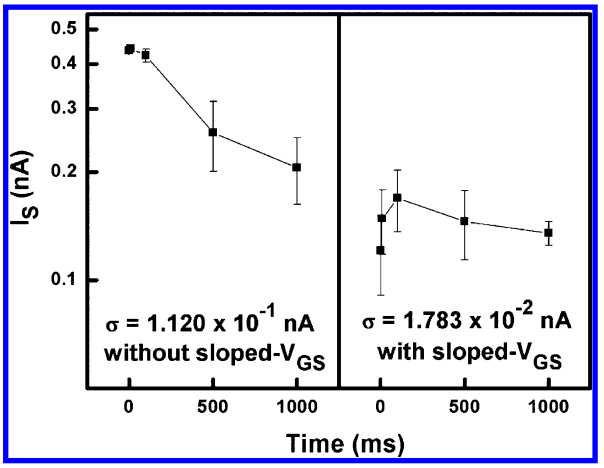

Figure 9. (a) I_S measured at various times after switching V_{GS} from 0.2 to 0.4 V without sloped-gate method in PB solution. (b) Same measurement as for (a) but with sloped-gate voltage method.

$$\mu = \frac{1}{N}\sum_{i=1}^{N} X_{\text{time}} \tag{7}$$

Time is five different sampling points of time (1, 10, 100, 500, and 1000 ms). These results indicate that switching V_{GS} with an adjusted slope m permits simultaneous measurements of I_S that are unaffected by the leakage current I_{GS}. The results of the variances for I_S are summarized in Table 1.

Table 1. Variance in Measured I_{DS} Values (ampere) after Switching V_{GS} with and without Adjusting V_{GS} Slope in Three Experiment Conditions

variance of I_{DS} (A) with different time intervals		
experiment condition	without sloped V_{GS}	with sloped V_{GS}
air	1.189×10^{-10}	1.985×10^{-12}
DI water	1.788×10^{-10}	1.120×10^{-10}
PB	2.682×10^{-11}	1.783×10^{-11}

For the poly-Si NW-FET in air, the variance reduced almost 2 orders of magnitude upon using the sloped-gate voltage method. Under liquid (De Ion water, DI Water) conditions, the variance decreased slightly more than 1 order of magnitude. The variance decreased ~1 order of magnitude in PB solution. These data demonstrate that the sloped-gate voltage method can also be applied under liquid conditions, making it a promising technique for future in biosensing processing. In addition, the slope-gate voltage method on reproducibility has been shown in the Supporting Information.

■ CONCLUSION

NW-FET has become an import device in the area of biological sensing application. The detecting tiny amounts of charged biomolecules affect femtoampere (fA) to nanoampere (nA) current change of electrical characteristic. Experimental results show that the leakage current I_{GS} is caused by the charging effect of an equivalent capacitor in the NW-FET structure. To explain this phenomenon, a physical model with equivalent resistance and capacitance was developed to simulate the leakage current of the poly-Si NW-FET, and the fit based on this model has a high correlation with the experimental data. This study also shows that the leakage current (I_{GS}) affects the

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accuracy of NW-FET measurements. To solve this problem, a novel V_{GS} switching method, which is the sloped-gate method, was proposed. The results indicate that the sloped-gate method decreases the variance in I_{DS} measured after switching V_{GS}, for poly-Si NW-FETs detections in air, liquid, and phosphate buffered solution (PBS). This method of measuring I_S in NW-FETs can be used for accurate measurements of different targets or for other applications as part of a biosensor platform; on the other hand, the physical model is able to evaluate the equivalent capacitor in the NW-FET for other analysis parameters of the biosensing application.

■ ASSOCIATED CONTENT

Supporting Information

Table I. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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