Improving Breakdown Voltage of LDMOS Using a Novel Cost Effective Design

Ming-Hung Han, Hung-Bin Chen, Chia-Jung Chang, Chi-Chong Tsai, and Chun-Yen Chang, *Life Fellow, IEEE*

***Abstract*—A reduced surface field (RESURF) laterally diffused metal oxide semiconductor (LDMOS) device with the concept of charge compensation using p-implant layer (PIL) without additional process step is proposed in standard 0.18-μm technology. By simply using the p-type drift drain (PDD) implantation of p-type LDMOS into n-type LDMOS, breakdown voltage (V_{BD}) is substantially improved. For a thorough study of device phenomena, hydrodynamic transport simulations are first performed to analyze the electric field distributions at high voltage bias in order to explain increases in breakdown voltage and predict its optimal design parameter. Then fabrication of the devices is performed and shows that the breakdown voltages increase significantly. The measurement results show a 12% improvement in V_{BD} and a 5% improvement in figure of merit (FOM). Throughout the fabrication process, the enlarged breakdown voltage obtained by the PIL without additional process and device area show the potential of cost effective. Because such devices have good off-state breakdown voltage and specific on-resistance, they are very competitive with similar technologies and promising system-on-chip (SOC) applications.**

***Index Terms*—RESURF, LDMOS, implantation, breakdown voltage**

I. Introduction

COMPLEMENTARY metal-oxide-semiconductor (CMOS) technologies, which integrate logic circuits, radio frequency (RF) circuits and power switches on a single chip, currently require power devices with reduced specific on-resistance ($R_{on,sp}$), improved breakdown voltage (V_{BD}) and current driving capability. Suitable power devices using CMOS must be developed to achieve the goal of system-on-chip (SOC) technology [1]–[11], particularly in the low voltage range such as 30 V rating for RF wireless system, display driver, and DC–DC converter applications [12]–[17], [24]–[28]. Recently, laterally diffused-metal-oxide-semiconductor (LDMOS) with double reduced surface field (RESURF) technologies, which using the concept of charge compensation, perform with thin epitaxial layers or well implants to design high-voltage devices with a low $R_{on,sp}$ are proposed [18]–[23]. Many studies of double RESURF show that high breakdown voltages can be maintained while increasing drift region doping concentration up to double that in single RESURF devices in order to achieve a good trade-off between off-state V_{BD} and $R_{on,sp}$. Additionally, many studies have improved the characteristics of lateral devices with CMOS-compatible processes, including silicon on insulator (SOI) [26]–[28] and Bipolar CMOS (BiCMOS) [29], [30] technologies; however, their novel mask designs, large device areas, and complex processes increase fabrication costs [24]–[30].

In this work, we propose a simple p-implant layer (PIL) implant methodology to implement the idea of charge compensation in RESURF LDMOS devices to improve off-state breakdown voltage and attain low $R_{on,sp}$ without adding any new process step in standard 0.18-μm CMOS technology. The paper is organized as follows. In §2, we describe the device structure, simulation technique, and fabrication process flow. In §3, we study the simulation and experimental results to examine the breakdown voltage with different PIL design. Finally, conclusions and future work are drawn.

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II. Simulation Methodology and Fabrication Process

Fig. 1 show the LDMOS device structure and layout design in this work. In simulations of the explored devices have an oxide thickness 45 nm, a channel length (L) of 1.2 μm, and a channel width (W) of 10 μm. The overlap between gate and n-type drift drain (NDD) region is 0.5 μm, the space between gate edge and source/drain is 1 μm, source/drain junction length and depth are 410 nm and 300 nm, respectively, and the NDD region depth is 1.1 μm. The p-well doping concentration is 2×10^{17} cm^{-3}, the doping concentrations in the source, drain and poly-gate are all $1\text{x}10^{20}$ cm^{-3}, and the NDD doping concentration in the drift region is 2×10^{17} cm^{-3}. To achieve the concept of charge balance, the PIL is used, in which the depth is the same as the NDD region depth, 1.1 μm, and the width and length of PIL (W_{PIL}, and L_{PIL}) are design parameters, as shown in Fig. 1. For accurate numerical results under high voltage conditions, device simulations are performed by solving 3D hydrodynamic transport equations and drift-diffusion equations using commercial tool Synopsys Sentaurus Device [31]. The Shockley–Read–Hall recombination model is considered. Fig. 2 displays the process flow of the proposed n-type LDMOS. The transistor fabrication

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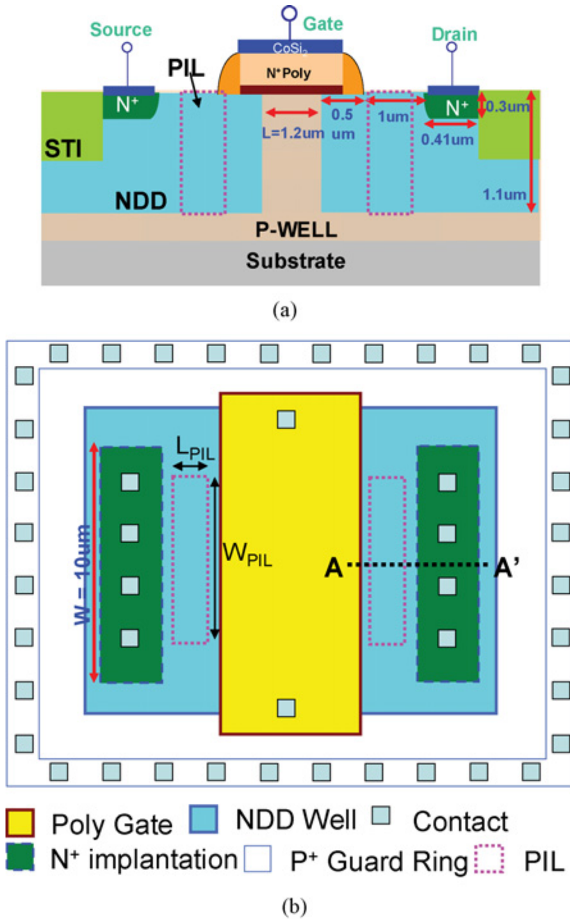

Fig. 1. The (a) device structure and parameters and (b) layout design of LDMOS used in this work. The position of p-implant layer (PIL) is also indicated.

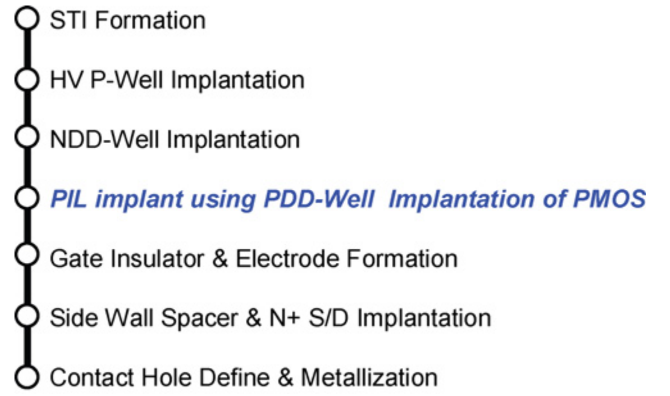

Fig. 2. The fabrication process flow of the 0.18 μm n-type LDMOS device in this work. To implement p-implant layer, we use PDD-Well implantation of p-type LDMOS after NDD-Well implantation.

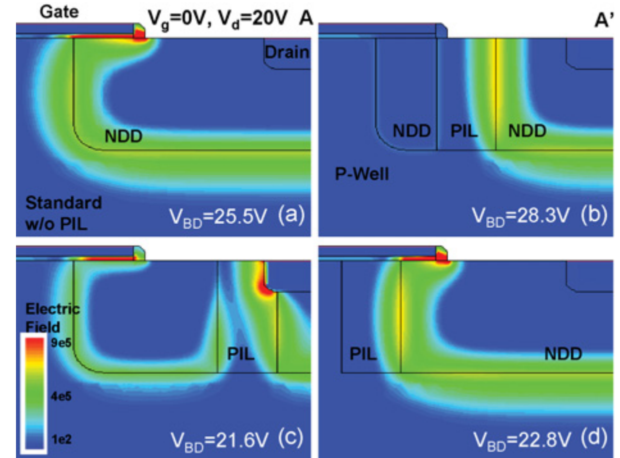

Fig. 3. The simulated electric field distributions of (a) standard device (without PIL), and with PIL located (b) at middle of NDD region, (c) connect to the drain, and (d) connect to the channel at bias condition V_g = 0 V and V_d = 20 V. The VBDs of the devices are shown in the bottom and positions of A and A' are indicated in Fig. 1(b).

process is based on a 0.18-μm high voltage (HV) CMOS technology developed by Maxchip Electronics Corporation. This technology is applicable in both HV LDMOS with and without PIL. The n-type LDMOS is fabricated from a (100) oriented p-type wafer with doping concentration of 1×10^{15} cm^{-3}, and the fabrication process begins by defining the active region and then performing shallow trench isolation (STI). The HV p-well ion implantations are then performed. The NDD ion implantation in the drift region is then carried out after the p-well drive-in. For implementation of PIL, the p-type drift drain (PDD) implantation is used when implant PDD region of p-type LDMOS (PMOS). Then gate electrode, nitride spacer side wall, and source/drain annealing are performed. A thick inter-level oxide deposition of TEOS is followed by contact lithography and oxide etching to form the contact window. The final step of the LDMOS transistors fabrication sequence is metallization and passivation.

III. Results and Discussions

Since the PDD implantation of PMOS is utilized to maintain simple process and low cost, the dose and depth of PIL are thus fixed in this work. To find the optimal design of PIL, we firstly use the simulation to search the highest V_{BD} by tuning the position, width, and length of PIL. The characteristics of simulated standard device are calibrated to that of the experimental data. Fig. 3 compares the electric field distributions of standard (3(a)), PIL locate at the middle of NDD region (3(b)), PIL connect to the drain (3(c)), and PIL connect to the channel (3(d)) before device breakdown (V_g = 0V and V_d = 20V) for discussing the PIL position effect to device V_{BD}. The L_{PIL} and W_{PIL} in Fig. 3 are set to 500 nm and 10 μm, respectively, and the positions of A and A' are indicated in Fig. 1(b). The off-state (V_g = 0 V) breakdown voltages which are defined as the voltage at I_d = 1μA in I_d-V_d curves of different devices are also presented in the bottom of each plot. In Fig. 3(a), it is clearly showed that the electric field concentrates at the channel surface and NDD/P-well junction. Additionally, after the use of PIL in the NDD region, the electric field in channel surface is reduced, therefore, the V_{BD} improves significantly, as shown in Fig. 3(b). However, once the PIL connect to the drain, an additional junction is produced, which provide a large electric field due to the large concentration gradient between drain and PIL, result in the degradation of V_{BD}, as presented in Fig. 3(c). Fig. 3(d) displays another extreme case, the PIL

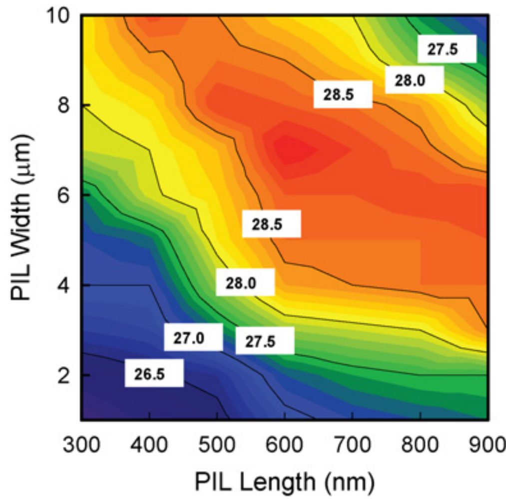

Fig. 4. The contour plot of simulated breakdown voltages of LDMOS with PIL for different PIL length L_{PIL} and PIL width W_{PIL}.

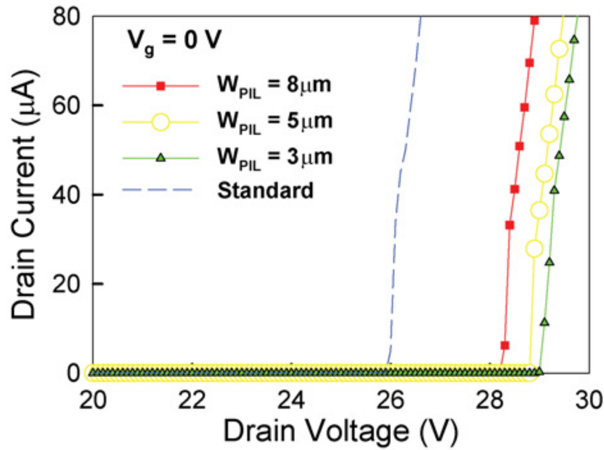

Fig. 5. Measured off-state (Vg = 0 V) I-V characteristic of the LDMOS with different PIL design.

connect to the p-well and directly changes the device channel length. Although the electric field distribution does not greatly alter, since the standard LDMOS device in this work is well designed, the change of channel length substantially affects the device performances, including the V_{BD}. On the other hand, it has to mention that although the use of PIL may reduce the current and degrade the $R_{on,sp}$ owing to the opposite doping type of PIL, since the depth of PIL is the same as NDD region depth, the current distribution in NDD region will not change significantly, thus the current crowding effect in device with PIL is similar to that in standard device when operating near breakdown. Fig. 4 shows the contour plot of V_{BD} as a function of L_{PIL} and W_{PIL} with position of PIL located at the center of NDD region (from NDD edge under the gate to drain edge). The simulation results show that if the area of PIL (L_{PIL}xW_{PIL}) becomes too small or too large, the V_{BD} will not improve according to the calculation of Poisson equation for charge balance condition. Moreover, the simulation results also indicate that there provide a large design window to perform V_{BD}>28 V (10% improvement). To confirm the simulation

TABLE I

SUMMARY OF DEVICES CHARACTERISTICS FOR DIFFERENT PIL DESIGN

L_{PIL} (μm)	W_{PIL} (μm)	R $_{on,sp}$ mΩxmm^2	V_{BD} (V)	V_{BD} improvement %	FOM (V_{BD} / $R_{on,sp}$)
0.42	8	33.3	28.1	8.9	0.84
0.42	5	20	28.6	10.8	1.43
0.42	3	14.2	28.9	12	2.04
0*	0*	13.3	25.8	0	1.94

No p-implant layer (PIL), standard device.

results, three kinds of PIL designed devices are fabricated according to the optimal simulated results. However, due to the position of PIL is important, and considers the thermal diffusion of Boron in PIL when forms the gate insulator/electrode and source/drain implantation annealing, the minimum design rule of L_{PIL}, 0.42 μm, is used. The design parameter in fabricated devices considers the W_{PIL} only, the performances of W_{PIL} = 3 μm, 5 μm, and 8 μm are measured and discussed. It has to notice that the LPIL and W_{PIL} in fabricated devices are layout dimensions, which may not equal to the physical PIL length and PIL width used in the simulation due to thermal diffusion of Boron in PIL. According to the fabrication experience and theoretical calculation of thermal budget, the physical dimensions of the PIL in fabricated devices are about L_{PIL} = 750 nm, and W_{PIL} = 8.3, 5.3, and 3.3 μm, respectively. Fig. 5 displays the measured I_d-V_d characteristics at Vg = 0 V for LDMOS devices with different PIL. The off-state breakdown voltages improve about 9%, 11%, and 12% for W_{PIL} = 8 μm, 5 μm, and 3 μm, compare with standard LDMOS. Using PDD-Well implantation of PMOS to perform PIL in n-type LDMOS is a good way to improve V_{BD} while maintaining simple process and low cost. Additionally, since the substrate current I_{sub} is an important predictor to monitor the device lifetime [32], [33], I_{sub} of standard and best device in this work are measured and compared to discuss the reliability of the devices. Although the implantation of PIL may cause damage to the NDD region and degrade the performance, the reduction of measured I_{sub} of device with PIL revealing the use of PIL improves the reliability of the device due to the reduced electrical field in NDD region, as demonstrated in Fig. 6. Table I summarizes the comprehensive comparison of electrical characteristics. The Fig. of merit (FOM) which is defined by V_{BD} /$R_{on,sp}$, is used to evaluate device efficiency. The value of $R_{on,sp}$ is extracted from I_d-V_d curve for on-state (V_g = 18 V) and V_d = 0.1 V. The best FOM of the devices in this study is 2.04, which is 5% better than that of standard device. Fig. 7 compares the $R_{on,sp}$ vs V_{BD} of several LDMOSs in recent years [13]–[17], in which the devices in literatures provide various rated of breakdown voltage. It is a trade-off between breakdown voltage and specific on-resistance. The devices in this work show competitive with respect to similar technologies and device with W_{PIL} = 3 μm improves V_{BD} significantly which keep the comparable $R_{on,sp}$.

IV. CONCLUSION AND FUTURE WORK

This study successfully implemented a RESURF LDMOS device with PIL in standard 0.18-μm technology. By simply

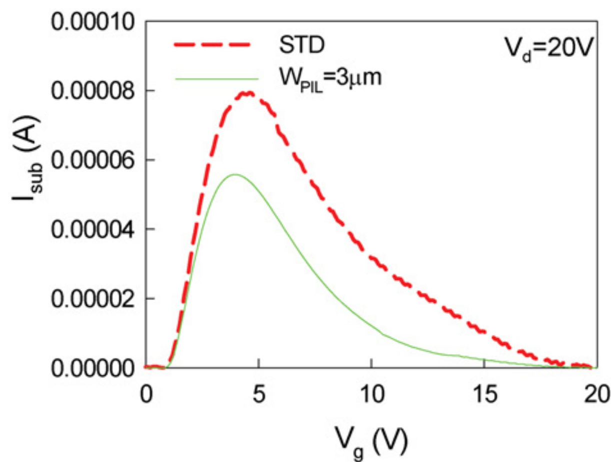

Fig. 6. Measured substrate currents I_{sub} of the standard and best LDMOSs.

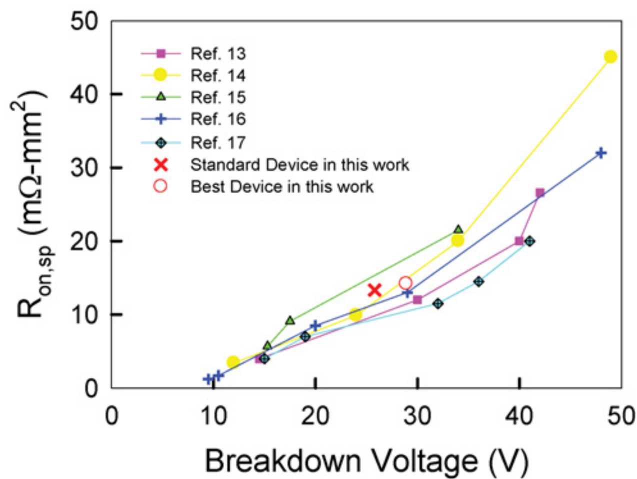

Fig. 7. Comparison of $R_{on,sp}$ vs V_{BD} between devices in this work and similar technologies.

using the PDD implantation of p-type LDMOS as PIL into NDD region of n-type LDMOS, a device fabricated with best PIL area achieves a V_{BD} improvement of 12% with a small increase of $R_{on,sp}$. Throughout the whole fabrication process, no additional process step and not increase in device area are required. Because of their good off-state V_{BD} and $R_{on,sp}$, the devices have potential use in SOC applications. We are currently working on using NDD implantation into PMOS with the same idea proposed in this work, which may improve the performances of PMOS simultaneously for CMOS application.

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