Sealing Bump With Bottom-Up Cu TSV Plating Fabrication in 3-D Integration Scheme

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***Abstract*— A sealing bump approach for the simplification of the conventional bottom-up copper through-silicon via (TSV) plating process flow is developed to reduce the process steps and increase the throughput without sacrificing the structure integrity and electrical performance. In this approach, TSV and bump formation can be achieved simultaneously through the bottom-up plating. Results from the analysis reveal excellent electrical characteristics and quality examination, which indicate that the proposed approach may be a good candidate for the TSV fabrication in 3-D integration.**

***Index Terms*— 3-D integration, bottom-up plating, through-silicon via (TSV).**

I. Introduction

THREE-dimensional integrated circuit (3-D IC) technology provides a solution to overcome the lithography and physical limitation according to International Technology Roadmap for Semiconductors [1]. To connect the contacts vertically, through-silicon via (TSV) is considered as the critical technology in 3-D IC application [2]. Intrinsically, copper (Cu) TSV formation can be achieved by top-down and bottom-up plating approaches. Conventional top-down TSV approach, using blind-via plating technique, offers a number of merits, including the flexibility of integration flow in via-first, via-middle, and via-last schemes. For example, the Interuniversity Microelectronics Center has developed a representative of Cu nail technique after front-end-of-line process using the top-down TSV approach [3]. Some issues have to be concerned using blind-via plating technique. For example, the characterization of the barrier/seed layer becomes extremely challenging with the higher aspect ratio of TSVs. Seams or voids are easily trapped inside if the via profile is not well defined. In addition, electrolyte with additives and a monitor system are required to achieve a void-free filling [4].

The advantages of the bottom-up TSV approach are to avoid the concerns mentioned above [5], [6]. Especially, the bottom-up process is suitable for the via-last approach, which can integrate separate tiers from different foundry/packaging services using the optimized technology. However, the bottom-up plating usually requires the temporary bonding or attaching technology with metal layer at the bottom side in order to accomplish the via filling process [5], [6]. The removal of handing carrier or attached metal may result in extra cost and reliability issue. In this letter, we demonstrate a new approach of sealing bump before Cu TSV filling based on bottom-up plating process. The electrical characteristics and material analysis of this scheme are also investigated and discussed in this letter.

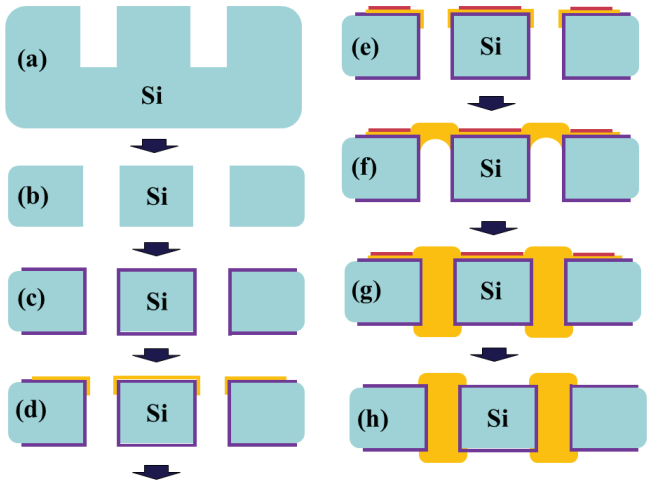

Fig. 1. Process flow of proposed sealing bump bottom-up plating approach.

II. Process and Integration Demonstration

Fig. 1 shows the process flow of sealing bump bottom-up Cu TSV plating approach.

1) TSV is formed by using a photoresist as the hard mask and an optimized Bosch process to obtain a vertical profile.
2) After TSV etching, the wafer is thinned down until exposing vias.
3) Plasma-enhanced tetraethyl-orthosilicate oxide as an insulation layer is deposited on the wafer surface and the via sidewall.
4) Barrier layer/adhesion layer and Cu seed layer are sputtered on the top of the wafer.

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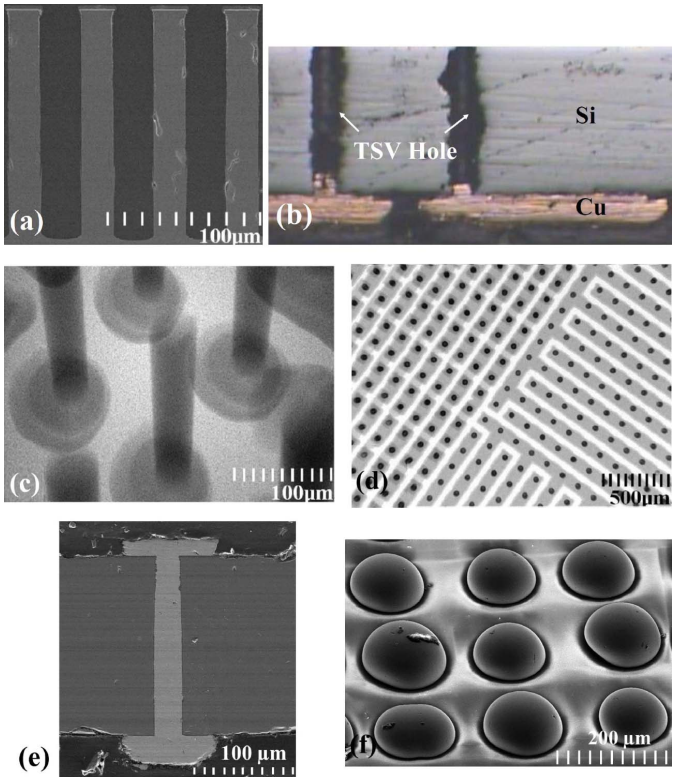

Fig. 2. (a) Etching profile of 25 μm via using DRIE Bosch process. (b) Fabricated sealing bumps before TSV filling. (c) X-ray image of voidfree filled TSVs. (d) Wafer from backside with TSVs, where top and bottom metal lines are overlapped. (e) SEM image of single TSV structure with Cu bumps on both sides. (f) Final structures of Cu bumps with TSVs inside.

5) Uniform sprayed photoresist (5-μm thick) is coated on the nonplanar substrate surface with TSV holes, and followed by a lithography process to define the bump area.
6) Cu sealing bumps are formed by electroplating.
7) After the bump side of wafer is coated with photoresist, the wafer is flipped upside down and performed with bottom-up Cu TSV plating.
8) After removing the photoresist and barrier/seed layers, the thinned 3-D integration wafer with Cu TSVs and bumps is completed.

III. Material Analysis and Electrical Characteristics

Scanning electron microscope (SEM), optical microscope, and X-ray analysis are adopted to ensure no defects in the wafer produced subsequently by the approach proposed. The cross-sectional SEM image of etched 25-μm TSV profile is shown in Fig. 2(a). The feature of 25 μm with the large via depth of 200 μm shows a successful TSV etching with an aspect ratio of 8. Followed by the via etching, bump sealing is successfully fabricated, and then via filling with electrochemical deposition plating is performed, as shown in Fig. 2(b) and (c), respectively. The nondestructive X-ray analysis is utilized for the defect inspection. Multiple Cu TSVs are thoroughly filled without any seam or void trapped inside.

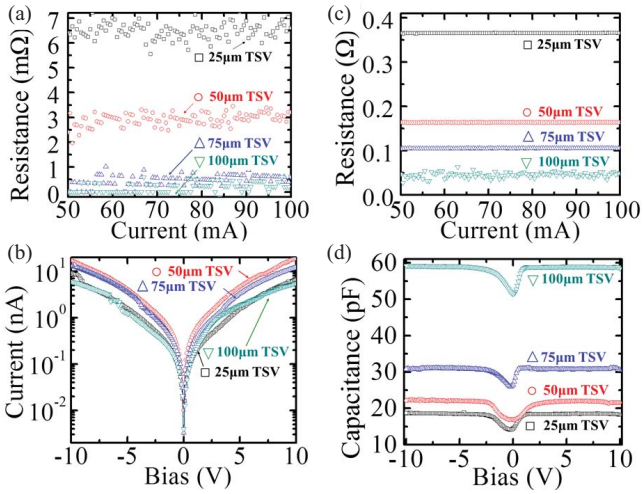

Fig. 3. (a) Resistance measurement of single Cu TSV with different sizes. (b) Resistance measurement of 30 TSVs in series based on daisy chain structure. (c) Leakage current measurement of 100 TSVs based on comb structure. (d) Coupling capacitance measurement of 100 TSVs.

Metal lines on the front side can be fabricated and conducted to TSVs sequentially during sealing bump process, whereas those on the back side substrate can be formed after TSV bottom-up plating. In Fig. 2(d), the black dots are Cu TSVs, the white area is the SiO_2 region, and the gray-colored area is consisted of the metal lines. These clear structures on the image indicate a successful fabrication. As shown in Fig. 2(e), the SEM image of single TSV with Cu bumps on both sides of the thinned wafer shows a complete Cu filling profile without voids, seams, or defects. Finally, the successful fabricated 3-D integration structure is shown in Fig. 2(f), where multiple Cu bumps are fabricated with Cu TSVs inside.

The four-point Kelvin structure is fabricated to investigate the characteristic of single TSV. Fig. 3(a) shows the resistance results of the single TSV with different diameters under current stressing. Measured resistances of single TSV with various sizes mostly match the theoretical values. Only the resistance of single 50-mm-diameter TSV is higher because of the quality of TSV and contact resistance of TSV and metal layer. In addition, the resistances of daisy chain structure with multiple Cu TSVs, metal lines, and corresponding contact resistances are measured, as shown in Fig. 3(b). With the same TSV pitch of 200 μm, the measured daisy chain resistances of 25, 50, 75, and 100 μm TSV show stable values during the current operation.

To realize the insulating capability of TSV sidewall, a comb structure with 100 TSVs and bumps on the front side is designed to measure the leakage current. By supplying the voltage between 10 and -10 V, the average leakage currents of 25, 50, 75, and 100 μm TSVs are all below 1 nA. This leakage value is identical with other studies, showing the excellent insulation performance on via sidewall is demonstrated [7], [8]. Finally, Fig. 3(d) shows the measurement of coupling capacitance by applying the voltage from 10 to -10 V. The capacitance behavior can be further explained as the coupling structure with two TSVs is similar to two MOS capacitors.

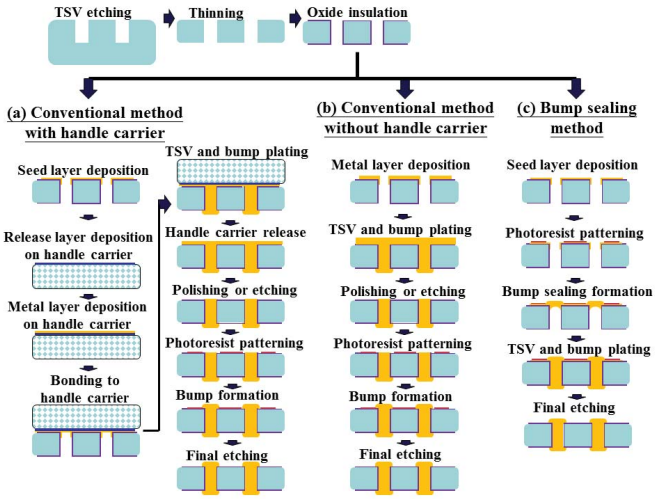

Fig. 4. Schematic diagrams. (a) Conventional method with handle carrier. (b) Conventional method without handle carrier. (c) Bump sealing method proposed in this letter.

When the voltage is applied, two capacitors are operated in the depletion and accumulation mode. The average measured coupling capacitances for 25, 50, 75, and 100 μm of TSVs are 0.74, 0.88, 1.23, and 2.36 pF, respectively. Based on the equation derived theoretically in the previous literature [9], the coupling capacitances of 25, 50, 75, and 100 μm TSVs are 0.56, 1.09, 1.64, and 2.19 pF, respectively. The small difference of measured and calculated capacitances mainly comes from the dielectric constant of oxide and variance of oxide thickness in TSV (for example, the actual thickness of PE-TEOS oxide at the top, middle sidewall, and bottom in 25-μm TSV are 0.95 m, 0.68 m, and 0.86 μm, respectively). Therefore, experimental results are compatible to the ideal values, indicating this structure is well-fabricated.

IV. Comparison With Other Bottom-Up TSV Plating Approaches

In the conventional bottom-up plating scheme, the temporary bonding technique is usually used to hold the wafer to be thinned [5]. In addition, the metal seed layer is required on the handle carrier in addition to the backside of wafer. Therefore, two metal layers can be bonded together before bottom-up plating. However, although the scheme of one thin-top wafer bonded to the bottom wafer can be achieved, the temporary bonding and following handle carrier release process make this approach complicate and not cost-effective, as shown in Fig. 4(a).

When the target of wafer thickness is not too thin, the thinned wafer can be processed in fabrication equipment without the extra handle carrier. Then the method of direct metal seed layer deposition on one side of the wafer is usually applied before bottom-up plating [10]. As shown in Fig. 4(b), however, this approach still requires all the processes to fabricate bumps or RDL after the metal layer is removed.

Comparing with the above two bottom-up approaches, our proposed approach in Fig. 4(c) does not require the extra handle wafer and corresponding releasing process. In addition, the approach can achieve TSV and bump formation simultaneously. With the validation of electrical performance and quality examination, this approach can be possibly applied in 3-D integration scheme, especially for packaging or via-last fabrication.

V. Conclusion

In this letter, we proposed a new approach for the simplification of the bottom-up Cu TSV plating. By swapping the procedure of TSV and bump formation, the process steps can be reduced effectively. TSVs with different sizes using this approach were fabricated and investigated. Kelvin structure, daisy chain, and comb structure were designed to investigate for the electrical characteristics of single TSV resistance, via chain resistance, leakage, and coupling capacitance. The advantages of this approach included not only those of bottom-up plating approach, but also the simplification of fabrication flow. The proposed framework was compatible to the ready process of the via-last approach in 3-D integration scheme.

References

[1] *International Technology Roadmap for Semiconductors*, Semiconductor Industry Association, San Jose, CA, USA, 2001.

[2] C. Laviron, B. Dunne, V. Lapras, P. Galbiati, D. Henry, F. Toia; S. Moreau, R. Anciant, C. Brunet-Manquat, and N. Sillon, "Via first approach optimisation for through silicon via applications," in *Proc. 59th Electron. Compon. Technol. Conf.*, May 2009, pp. 14–19.

[3] A. Jourdain, T. Buisson, A. Phommahaxay, A. Redolfi, S. Thangaraju, Y. Travaly, E. Beyne, and B. Swinnen, "Integration of TSVs, wafer thinning and backside passivation on full 300 mm CMOS wafers for 3D applications," in *Proc. IEEE 61st Electron. Compon. Technol. Conf.*, Jun. 2011, pp. 1122–1125.

[4] S. P. Shen, W. P. Dow, M. Kubo, T. Kamitamari, E. Cheng, J. Y. Lin, and F. C. Hsu, "Novel Cu plating formula for filling through silicon vias," in *Proc. IEEE 4th Microsyst., Packag., Assembly Circuits Technol. Conf.*, Oct. 2009, pp. 186–189.

[5] H. H. Chang, Y. C. Shih, C. K. Hsu, Z. C. Hsiao, C. W. Chiang, Y. H. Chen, and K. N. Chiang, "TSV process using bottom-up Cu electroplating and its reliability test," in *Proc. 2nd Electron. Systemintegr. Technol. Conf.*, Sep. 2008, pp. 645–650.

[6] Y. Aibin, J. H. Lau, W. H. Soon, A. Kumar, W. Y. Hnin, W. S. Lee, M. C. Jong, V. N. Sekhar, V. Kripesh, D. Pinjala, S. Chen, C. F. Chan, C. C. Chao, C. H. Chiu, C. M. Hunag, and C. Chen, "Fabrication of high aspect ratio TSV and assembly with fine-pitch low-cost solder microbump for Si interposer technology with high-density interconnects," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 1, no. 9, pp. 1336–1344, Sep. 2011.

[7] A. Mercha, J. Van Olmen, C. Huyghebaert, A. Jourdain, M. Stucchi, M. Rakowski, I. Debusschere, P. Soussan, W. Dehaene, K. De Meyer, Y. Travaly, E. Beyne, S. Biesemans, and B. Swinnen, "3D stacked ICs using Cu TSVs and Die to wafer hybrid collective bonding," in *Proc. IEEE Int. Electron Dev. Meeting*, Dec. 2009, pp. 1–4.

[8] T. Nakamura, H. Kitada, Y. Mizushima, N. Maeda, K. Fujimoto, and T. Ohba, "Comparative study of side-wall roughness effectson leakage currents in through-silicon via interconnects," in *Proc. IEEE Int. 3D Syst. Integr. Conf.*, Jan. 2012. pp. 1–4.

[9] G. Katti, M. Stucchi, K. D. Meyer, and W. Dehaene, "Electrical modeling and characterization of through silicon via for three-dimensional ICs," *IEEE Trans. Electron Dev.*, vol. 57, no. 1, pp. 256–262, Jan. 2010.

[10] S. Ho, S. Yoon, Q. Zhou, K. Pasad, V. Kripesh, and J. H. Lau, "High RF performance TSV for silicon carrier for high frequency application," in *Proc. IEEE Electron. Compon. Technol. Conf.*, May 2008, pp. 1956–1952.