

A Latchup-Immune and Robust SCR Device for ESD Protection in 0.25- μm 5-V CMOS Process

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Abstract—Based on good electrostatic discharge (ESD) robustness, silicon-controlled rectifier (SCR) device is used for on-chip ESD protection. The major concern of SCR is the latch-up issue, because of its low holding voltage. Previous papers tried to design latchup-immune SCR devices; however, those devices would cause lower ESD robustness. In this letter, a new latchup-immune and robust SCR device for ESD protection is proposed and verified in a 0.25- μm 5-V CMOS process. Through inserting one additional parasitic bipolar junction transistor into SCR device structure, this new proposed SCR can increase the holding voltage without causing degradation on its ESD robustness.

Index Terms—Electrostatic discharges (ESD), latchup, silicon-controlled rectifier (SCR).

I. INTRODUCTION

SILICON-controlled rectifier (SCR) device is known as an efficient device for electrostatic discharge (ESD) protection as it can have the highest ESD robustness in the smallest layout area [1]. However, the main concern of SCR device used in CMOS ICs is the latchup issue. Some noises may mistrigger the SCR device during normal circuit operations to cause the IC function failure.

Three conventional methods are presented to solve the latchup problem in previous papers. The first method is to increase the triggered current of SCR [2], [3]. In addition, some additional epitaxial or isolation layers are used to improve latchup immunity of the SCR for ESD protection [4], [5]. The second method is to dynamically modulate the holding voltage of SCR. The idea of dynamic holding voltage is to adjust the holding voltage of SCR by changing the gate bias of the embedded nMOS and pMOS to avoid latchup issue [6]. The third method is to increase the SCR holding voltage [7], [8]. If the holding voltage of SCR is higher than the normal supply voltage, it will be free from latchup issue. This method may decrease the ESD robustness because of the higher heat generation during ESD current discharging. Therefore, it is still a challenge to design an ESD-robust and latchup-immune SCR device within small layout area. In this letter, a new design is proposed to increase the holding voltage

Manuscript received January 30, 2013; revised March 2, 2013; accepted March 8, 2013. Date of publication April 1, 2013; date of current version April 22, 2013. This work was supported in part by the National Science Council, Taiwan, under Contract NSC 101-2220-E-009-020, Contract NSC 101-2221-E-009-141, and Contract NSC 101-3113-P-110-004. The review of this letter was arranged by Editor W. Ng.

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Digital Object Identifier 10.1109/LED.2013.2252456

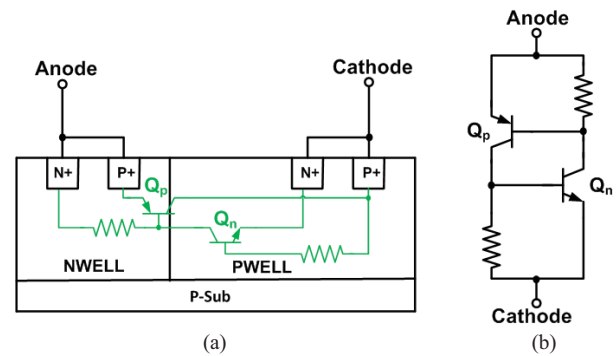


Fig. 1. (a) Cross-sectional view. (b) Equivalent circuit of conventional SCR.

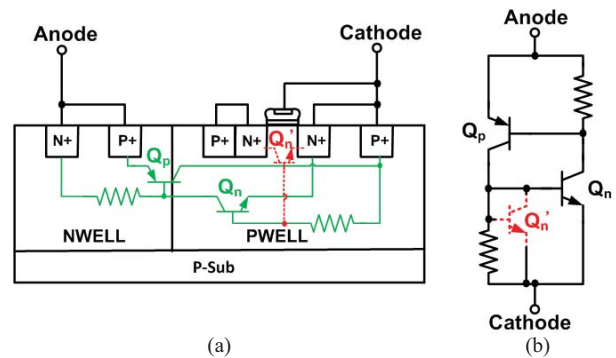


Fig. 2. (a) Cross-sectional view. (b) Equivalent circuit of new proposed SCR with high latchup immunity.

of the SCR device without decreasing its ESD robustness in a compact layout area.

II. DEVICE STRUCTURES

Two SCR structures are compared in this letter, which are labeled as the conventional SCR and the new proposed SCR, respectively. The cross-sectional view of the conventional SCR is shown in Fig. 1(a). The equivalent circuit of the conventional SCR is shown in Fig. 1(b) with the parasitic BJTs and resistors. During ESD stress, the NPN BJT (Q_n) may turn on first, and then it will help the PNP BJT (Q_p) to be turned on. The positive feedback of those two BJTs in SCR [9] is the reason why SCR can have such low holding voltage.

To improve latchup immunity, the new structure of SCR is shown in Fig. 2. To increase the holding voltage of SCR, one more parasitic BJT (Q_n') is inserted into the device structure, which is shown in Fig. 2(a). The equivalent circuit of the new proposed SCR is shown in Fig. 2(b). During the turn-on

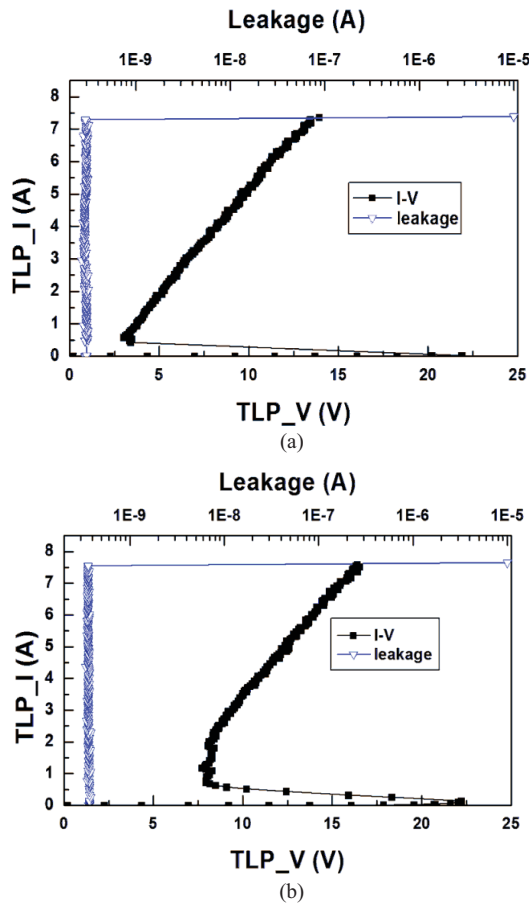


Fig. 3. TLP measurement results. (a) Conventional SCR. (b) New proposed SCR.

operation of the SCR, the NPN BJT (Q_n) and the additional parasitic BJT (Q_n') turn on at the same time. The additional BJT (Q_n') clamps the voltage between base and emitter of the NPN (Q_n), which makes the positive feedback of BJTs weaken. That is, the additional BJT (Q_n') will break the positive feedback of the NPN and PNP BJTs. Hence, the holding voltage of this new proposed SCR will be higher than that of the conventional SCR. Therefore, the new proposed SCR can be free from latchup problem. A dummy gate is added to reduce the base width of the additional BJT (Q_n'), which is the spacing between the two N^+ diffusions of collector and emitter. The dummy gate is connected to the cathode of SCR to turn off the channel beneath of dummy gate. The current gain of the additional BJT (Q_n') can be further increased by using a shorter channel length of dummy gate in the inserted NMOS. The new proposed SCR is fully process-compatible to the commercial CMOS processes without additional mask or process step in the chip fabrication.

This design is fabricated in a $0.25\text{-}\mu\text{m}$ 5-V process. The total widths of all test SCR devices are drawn as $200\ \mu\text{m}$ for performance comparison. All of the test devices occupy the same layout area.

III. EXPERIMENTAL RESULTS

A. TLP Test

A transmission-line-pulsing (TLP) system is used to measure the breakdown voltage, holding voltage, and the

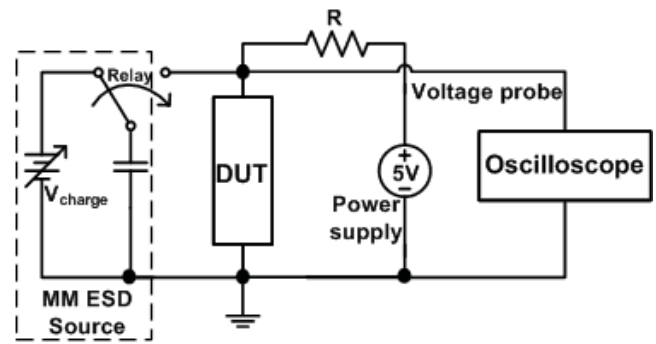


Fig. 4. Measurement setup of TLU test [10].

maximum current-handling ability (the second breakdown current, I_{t2}) of the fabricated devices. The failure criterion is defined as the leakage current over $1\ \mu\text{A}$ under the 5-V bias condition.

The TLP measurement results of the fabricated SCR devices are shown in Fig. 3. In Fig. 3(a), the breakdown voltage of the conventional SCR structure is $\sim 22\ \text{V}$ and the holding voltage is $\sim 3\ \text{V}$. Therefore, it may suffer the latchup issue by noise triggering in the normal operation condition with V_{DD} of 5 V. Comparing with the measurement result of the new proposed SCR in Fig. 3(b), the holding voltage of the new proposed SCR is increased to $\sim 7.7\ \text{V}$, whereas the breakdown voltage unchanged. The maximum current-handling ability (I_{t2}) of the new proposed SCR is not degraded, which is still as high as $\sim 7.5\ \text{A}$. Additional ESD-detection circuit [1] can be used to trigger the proposed SCR on, during ESD events.

B. ESD Robustness

To make sure that the ESD robustness of the new proposed SCR is not degraded, the human-body-mode (HBM) and machine-mode (MM) ESD tests are performed to the fabricated devices by the ESD tester. The failure criterion is defined with 30% of breakdown voltage shift after ESD stress. The conventional SCR can pass 8-kV HBM and 800-V MM ESD tests, which are the voltage limitation of a given ESD tester. The new proposed SCR can also pass the 8-kV HBM and 800-V MM ESD tests. This result confirms that the new proposed SCR does not degrade the ESD robustness.

C. TLU Test

Transient overshoots on power-supply voltage can take place because of the noise coupling under system or environment disturbance. Those overshoots may let SCR be mistriggered. The transient-induced-latchup (TLU) test is to simulate the noise condition under the normal operation. The TLU setup is shown in Fig. 4 [10], where the MM ESD source is used to generate the transient noise into the power supply of device under test. Therefore, the parasitic BJTs in SCR may be mistriggered by such transient noise. If it is affected by the latchup issue, the voltage waveform monitored in the oscilloscope will be clamped down to its holding voltage after transient noise triggering.

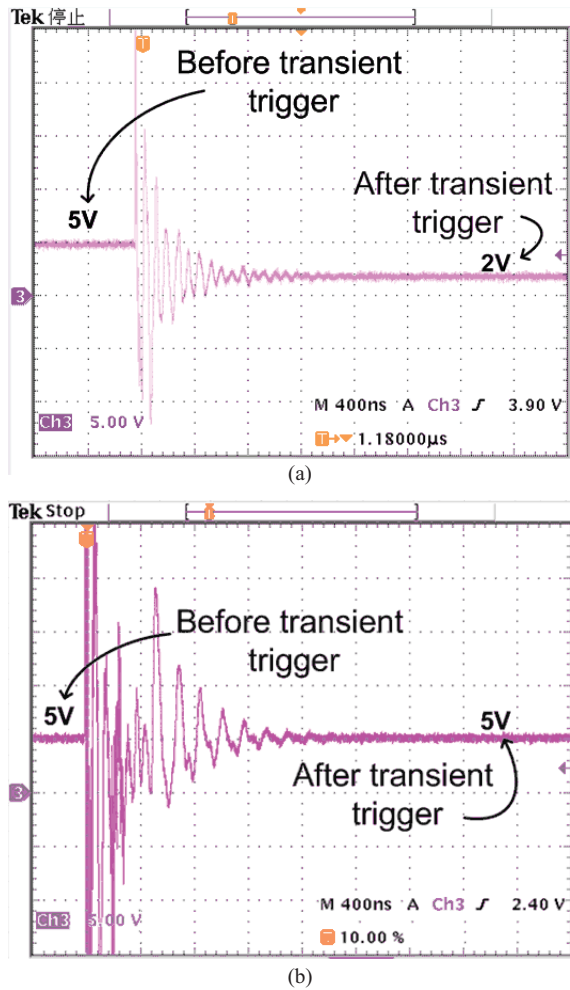


Fig. 5. Voltage waveforms before/after transient noise triggering. (a) Conventional SCR. (b) New proposed SCR, during TLU test.

The test results of the fabricated SCR devices are shown in Fig. 5. In Fig. 5(a), after transient noise triggering with the initial V_{charge} of only 50 V, the voltage is clamped down to ~ 2 V. On the contrary, the voltage across the new proposed SCR is still kept at 5 V, as shown in Fig. 5(b), even if the V_{charge} is up to 800 V during the TLU test. This result has proved that the new proposed SCR is a high latchup-immune device for 5-V circuit applications.

IV. CONCLUSION

A new SCR device was proposed and verified in a 0.25- μm 5-V CMOS process, which performed both of high ESD robustness and high latchup immunity in the same layout area, as compared with the convention SCR device. The new proposed SCR was fully process-compatible to the general CMOS processes without additional mask or process step in the chip fabrication. This new proposed SCR will be a good solution of ESD protection for 5-V circuit applications in the commercial IC products.

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