[3] C. J. Keavney, V. E. Haven, and S. M. Vernon, "Emitter structures in MOCVD InP solar cells," in *Conf. Record 21st IEEE Photovoltaic Specialists Conf.*, 1990, pp. 141–144.
[4] P. A. Basore, "PC-1D version 3: improved speed and convergence," in *Conf. Record 22nd IEEE Photovoltaic Specialists Conf.*, Las Vegas, NV, Oct. 1991, pp. 299–302.
[5] I. Weinberg, "Radiation damage in InP solar cells," *Solar Cells*, vol. 31, pp. 331–348, 1991.
[6] R. K. Jain and D. J. Flood, "Influence of the dislocation density on the performance of heteroepitaxial indium phosphide solar cells," *IEEE Trans. Electron Devices*, vol. 40, pp. 1928–1934, 1993.
[7] C. J. Keavney and M. B. Spitzer, "Indium phosphide solar cells by ion implantation," *Appl. Phys. Lett.*, vol. 52, pp. 1439–1441, 1988.
[8] C. J. Keavney, private communication.
[9] R. K. Jain, I. Weinberg, and D. J. Flood, "Comparison of n^+p and p^+n structures in indium phosphide solar cells," in *Proc. 3rd Int. Conf. on Indium Phosphide and Related Materials*, Cardiff, UK, Apr. 1991, pp. 168–172.
[10] R. K. Jain, G. A. Landis, D. M. Wilt, and D. J. Flood, "Lattice-mismatched $In_{0.40}Al_{0.60}As$ window layers for indium phosphide solar cells," in *Conf. Record 23rd IEEE Photovoltaic Specialists Conf.*, Louisville, KY, May 1993, pp. 757–762.

Interface Trap Effect on Gate Induced Drain Leakage Current in Submicron N-MOSFET's

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***Abstract*—An interface trap assisted tunneling mechanism which includes hole tunneling from interface traps to the valence band and electron tunneling from interface traps to the conduction band is presented to model the drain leakage current in a $0.5\,\mu m$ LATID N-MOSFET. In experiment, the interface traps were generated by hot carrier stress. The increased drain leakage current due to the band-trap-band tunneling can be adequately described by an analytical expression of $\Delta I_d = A\exp(-B_{\rm it}/F)$ with a value of $B_{\rm it}$ of 13 MV/cm, which is much lower than that (36 MV/cm) of direct band-to-band tunneling.**

I. Introduction

Gate-induced drain leakage (GIDL) current which is attributed to direct band-to-band tunneling has been recognized as a major drain leakage mechanism in off-state MOSFET's [1], [2]. Recently, the effect of hot carrier stress generated interface traps on the GIDL current has received considerable interest since it may impose a limiting factor on the scaling of a MOSFET. Various characterization and modeling techniques have been proposed to study the interace trap effects [3]–[5]. Hori characterized the additional drain leakage current at a low drain-to-gate bias by assuming a band-to-defect tunneling mechanism [6]. In his model, electrons are thermally excited from the valence band to interface traps, followed by tunneling into the conduction band. However, as the drain-to-gate bias increases, significant band-bending causes the quasi-Fermi level much below interface traps. Thermal excitation is no longer a dominant mechanism responsible for electron occupation in interface traps. Here, we develop an interface trap assisted two-step tunneling model to evaluate the trap effect on the drain leakage current in N-MOSFET's.

A 0.5 μm LATID MOSFET was fabricated. The increased drain leakage current after hot carrier stress was measured to compare the model.

Manuscript received March 14, 1994; revised July 6, 1994. The review of this brief was arranged by Associate Editor K. Shenai. This work was supported in part by the National Science Council, ROC, under Contract NSC81-0404-E-009-106 and in part by the Electronics Research Service Organization, ITRI, ROC, under Contract E83014.

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IEEE Log Number 9405948.

II. Interface Trap Assisted Tunneling Model

The schematic energy band diagram in the gate-to-drain overlap region, including hot carrier stress generated interface traps, is shown in Fig. 1. Due to a large lateral field in the channel (x direction), the interface states may have a chance to become negatively charged by emitting a hole into the valence band via quantum mechanical tunneling (step 1). In the same way, the interface states exchange the negative charge to the conduction band via electron tunneling (step 2). Thus a leakage current path resulting from a two-step tunneling process is established even in the absence of thermal excitation. In order to derive an analytical expression for the trap assisted tunneling current, we assume that electric fields in both x-direction and y-direction are constant in tunneling. In a steady state, the electron occupation factor of interface traps f_t is equated below for the number of trapped electrons remains constant [7];

$$(1 - f_t(E))/\tau_h(E) = f_t(E)/\tau_e(E) \tag{1}$$

where $\tau_h(E)$ and $\tau_e(E)$ are time constants for hole and electron tunneling through trap states with energy E. Based on the WKB approximation for tunneling through a triangular barrier, τ_h and τ_e are expressed in the following:

$$\tau_h(E) = \tau_{0v}\exp\left[\frac{4}{\hbar}(2m_p)^{1/2}\frac{(E-E_v)^{3/2}}{3qF_1}\right] \tag{2a}$$

$$\tau_e(E) = \tau_{0c}\exp\left[\frac{4}{\hbar}(2m_n)^{1/2}\frac{(E_c-E)^{3/2}}{3qF}\right] \tag{2b}$$

where m_n and m_p are effective masses for electrons and holes. F_1 is the lateral field and F is the vector sum of the lateral and vertical fields. τ_{0v} and τ_{0c} are effective carrier transit times in the valence band and in the conduction band. For simplicity, we use $m_n = m_p = 0.2m_0$ and $\tau_{0v} = \tau_{0c}$. It should be pointed out that hole tunneling is strictly restricted to the x-direction under a large negative gate bias from the viewpoint of energy conservation. In other words, only the lateral field can enhance the hole tunneling rate. Thus F_1 is involved in the expression of τ_h while a total field F is used in τ_e. For $F_1 < F$, the lateral field plays a dominant role in the current tunneling model.

Once the electron occupation factor f_t is obtained, the additional leakage current via the band-trap-band tunneling is derived:

$$\begin{aligned}\Delta I_d &\approx \Delta N_{\rm it}(E)f_t(E)/\tau_e(E)\,dE \\ &= \int \Delta N_{\rm it}(E)/[\tau_h(E)+\tau_e(E)]\,dE\end{aligned} \tag{3}$$

where $\Delta N_{\rm it}$ is the interface trap density generated during hot carrier stress. From (2), τ_h and τ_e vary exponentially with $E^{3/2}$. The integrand in (3) is a sharply peaking function of E, which has

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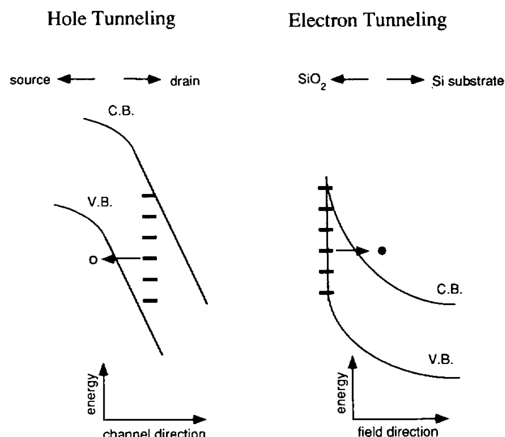

Fig. 1. Illustration of an interface trap-assisted two-step tunneling mechanism, including hole tunneling from interface traps to the valence band and electron tunneling from interface traps to the conduction band.

a maximum at $\tau_h(E) = \tau_e(E)$. Therefore, the integral can be simplified as follows:

$$\Delta I_d \approx \Delta N_{it}(E_t)/2\tau(E_t) \quad (4)$$

and

$$E_t = \frac{E_v + (F_1/F)^{2/3}E_c}{1 + (F_{1/F})^{2/3}} \quad (5)$$

where E_t is the trap level which is most effective in the trap-assisted tunneling process. Since τ has a function form of $\exp(B_{it}(E_t)/F)$, the interface trap induced drain leakage current can be adequately described by an analytical expression

$$\Delta I_d = A\exp(-B_{it}/F). \quad (6)$$

III. Experiment

A polysilicon gate LATID device [8] was characterized to study the hot carrier induced drain leakage phenomenon. The gate length is 0.5 μm. The gate oxide thickness, spacer width, and channel width are 150 Å, 0.15 μm, and 50 μm, respectively. The threshold voltage adjustment was performed by 60 keV BF_2 ions with a dose of 4×10^{12} cm^{-2}. The LATID n$^-$ dose and implant energy are 3.0×10^{13} cm^{-2} and 60 keV phosphorus with a tilt angle of 45°. The overlap between the gate and the n$^-$ region is about 0.075 μm. The 80 keV arsenic was implanted in the source/drain at a dose of 3.0×10^{15} cm^{-2}.

The device was stressed at a drain bias of 6.5 V and a gate bias of 2.5 V. Under this stress condition, a roughly maximum interface trap generation rate was obtained.

IV. Results and Discussion

The electric field distributions along the interface in both x and y directions are calculated from a two-dimensional device simulation in Fig. 2 at a drain bias of 8 V and a gate bias of −4 V. The spatial distribution of the interface traps calculated from a numerical simulation [9] is also shown in the figure. Note that the lateral field is much higher than the vertical field in the region of the interface traps in the current device structure. In this condition, F_1 is close to F and E_t in (5) is about $(E_v + E_c)/2$, which indicates that mid-bandgap traps are most effective in the tunneling process in the measured device. As a result, a theoretical lower limit of ($B_{it} = (4/\hbar)(2 \times 0.2m_0)^{1/2}[(E_g/2)^{3/2}/3q]$) is obtained and its value is 13 MV/cm. This value is consistent with the current measurement and is much lower than the reported experimental result (36 MV/cm [10]) of the GIDL current due to direct band-to-band tunneling. The measured and calculated additional drain leakage currents after hot carrier stress are compared in Fig. 3 with a stress time of 500 s. The drain biases are 7 V and 8 V in the measurement. In the calculation, (6) is used with a B_{it} value of 13 MV/cm. The electric field F at each bias point is obtained from a 2D device simulation. Good agreement between the measured and the calculated results is achieved with A as a fitting parameter.

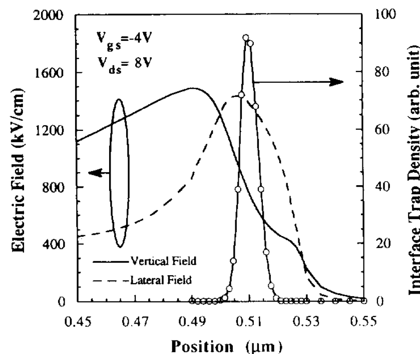

Fig. 2. Lateral and vertical field distributions along the interface at a drain bias of 8 V and a gate bias of −4 V. The interface trap distribution is also plotted.

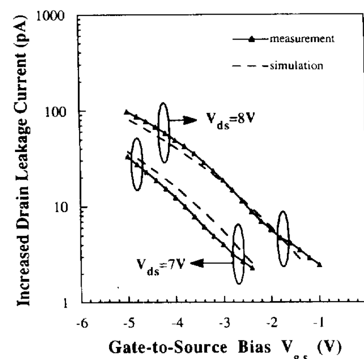

Fig. 3. Measured and calculated additional drain leakage current after hot carrier stress. The drain biases are 7 V and 8 V in measurement. Stress time is 500 s.

In conclusion, we have developed an interface trap assisted tunneling model to describe the increased drain leakage current in a 0.5 μm LATID MOSFET after hot carrier stress. Our model is confirmed by a good agreement between the measured data and the predicted dependence of the trap-assisted tunneling current on the gate and drain voltages.

References

[1] J. Chen, T. Y. Chan, P. K. Ko, and C. Hu, "Subbreakdown drain leakage current in MOSFET," *IEEE Electron Device Lett.*, vol. EDL-8, pp. 515–517, 1987.

[2] T. Y. Chan, J. Chen, P. K. Ko, and C. Hu, "The impact of gate-induced drain leakage current on MOSFET scaling," in *IEDM Tech. Dig.*, p. 721, 1987.

[3] H. Sasaki, M. Saitoh, and K. Hashimoto, "Hot-carrier induced drain leakage current in n-channel MOSFET," in *IEDM Tech. Dig.*, pp. 726–729, 1987.
[4] C. Duvvury, D. J. Redwine, and H. J. Stiegler, "Leakage current degradation in N-MOSFET's due to hot-electron stress," *IEEE Electron Device Lett.*, vol. 9, pp. 579–581, 1988.
[5] G. Q. Lo, A. B. Joshi, and D.-L. Kwong, "Hot-carrier-stress effects on gate-induced drain leakage current in n-channel MOSFET's," *IEEE Electron Device Lett.*, vol. 12, pp. 5–7, 1991.
[6] T. Hori, "Drain-structure design for reduced band-to-band and band-to-defect tunneling leakage," in *Symp. VLSI Technol.*, pp. 69–70, 1990.
[7] J. G. Fossum, A. Ortiz-Conde, H. Shichijo, and S. K. Banerjee, "Anomalous leakage current in LPCVD polysilicon MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 1878–1884, 1985.
[8] T. Hori, J. Hirase, Y. Odake, and T. Yasui, "Deep-submicrometer large-angle-tilt implanted drain (LATID) technology," *IEEE Trans. Electron Devices*, vol. 39, pp. 2312–2324, 1992.
[9] T. Wang, C. Huang, P. Chou, S. Chung, and T. Chang, "Effects of hot carrier induced interface state generation in submicron LDD MOSFET's," to be published in *IEEE Trans. Electron Devices*.
[10] D. S. Wen, S. Goodwin-Johansson, and C. Osburn, "Tunneling leakage in Ge-preamorphized shallow junctions," *IEEE Trans. Electron Devices*, vol. 35, pp. 1107–1115, 1988.

Nonuniform Reverse-Breakdown Characteristics of n^+-Diodes Fabricated by LOCOS and Trench Isolation

Takashi Ohzone and Hideyuki Iwata

***Abstract*— Light emission-intensity profiles, images and nonuniform photon counts from reverse biased n^+-diode fabricated by LOCOS and trench isolation are measured. Both spatial fluctuations of the emission profiles and nonuniform photon counts are relatively larger in trench-isolated diodes than those in LOCOS-isolated ones, and decrease as the reverse current increases.**

I. Introduction

For fabricating high-quality and high-yield LSI's, reverse breakdown of a diode must be sufficiently uniform at applied voltages much higher than the operation voltage. The reverse breakdown typically occurs at the junction periphery adjoining the isolation edge where the electric-field becomes higher than that of the plain junction region. The total length of the junction periphery becomes longer as the packing density of LSI's increases higher because the device size is scaled down and the number of devices increases rapidly. Consequently, a detailed analysis of the breakdown characteristics at the periphery is useful to develop the fabrication process as well as to improve the yield of LSI's. Although electrical measurements cannot distinguish weak or degraded points of the diode, they have been commonly used for a high-sensitivity analysis of the diode characteristics. Recently, a light emission microscope has been used for failure analysis of CMOS devices, for weak spot analysis of the diodes [1] and for reliability analysis [2].

In this paper, spatial fluctuations of the light emission-intensity profiles with and without an optical filter along the diode periphery and nonuniform photon counts from four sides of peripheries in reverse-breakdown n^+-diodes with LOCOS and trench isolation fabricated in six-inch wafers are discussed [3].

Manuscript received February 11, 1994; revised July 7, 1994. The review of this brief was arranged by Associate Editor K. Shenai.

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IEEE Log Number 9405947.

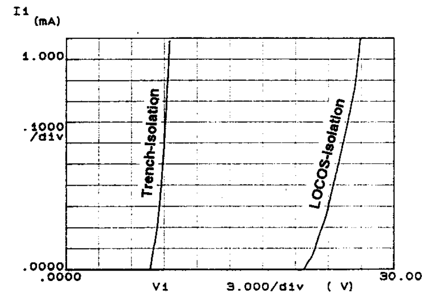

Fig. 1. Current-voltage characteristics of reverse-biased n^+-diodes.

II. Experiments

Light emission characteristics of the reverse-breakdown n^+-diode are measured by using the light emission microscope [3]. For measuring light emission characteristics from reverse-biased junction peripheries, an n^+-diode of $90 \times 90\,\mu m^2$ with four contacts at each corner is used as a test device for supplying uniform reverse bias-voltage to four sides of the peripheries. The substrate is $1 \times 10^{15}\ cm^{-3}$ p-type silicon and the junction depth of n^+-diodes formed by As-implantation is $0.20\,\mu m$. LOCOS isolation has $0.6\,\mu m$ thick field oxide under which a channel stop doping of about $4 \times 10^{16}\ cm^{-3}$ is formed to a depth of $0.45\,\mu m$. For trench-isolated diodes, shallow vertical trenches of $0.5\,\mu m$ depth are etched in the substrate, and boron ions are implanted into the trench sidewalls as a channel stop by using the tilt-angle four-times rotating implantation method [4]. Reverse-breakdown voltages of LOCOS and trench isolated n^+-diodes are about 22 V and 8 V, respectively, as shown in Fig. 1.

A superimposed micrograph of a reflected image and a light emission image from a reverse-breakdown n^+-diode with LOCOS-isolation is shown in Fig. 2(a). Reverse voltage (V_R) is applied to four corner pads of the square n^+-diode. Emission areas are localized along four peripheries of the n^+-diode. Emission images from four sides of the diode peripheries are shown in Fig. 2(b)–(d) for reverse current (I_R) of 4, 10, and 40 mA, respectively. Emission intensities from each side are quite different at low current levels, but the intensities become uniform as the current increases. A rectangle surrounded by a dotted line as seen in Fig. 2(b)–(d) shows an integrated area of total photon counts from one side of the periphery labeled "c."

A. Light Emission Intensity Profiles

Fig. 3 shows (a) normalized photoemission-intensity profiles without an optical filter along a periphery "c" of LOCOS-isolated n^+-diode for various reverse currents ranging from 2 to 10 mA, and (b) their emission images for two current levels of 2 and 10 mA. The emission-intensity profiles are measured along a linear slice of each image on which the maximum photon count is observed, and the slice is parallel to the periphery. The maximum photon count is nearly proportional to I_R as reported before [5]. The zero of

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