

A CMOS Power-Efficient Low-Noise Current-Mode Front-End Amplifier for Neural Signal Recording

Chung-Yu Wu, *Fellow, IEEE*, Wei-Ming Chen, *Student Member, IEEE*, and Liang-Ting Kuo

Abstract—In this paper, a new current-mode front-end amplifier (CMFEA) for neural signal recording systems is proposed. In the proposed CMFEA, a current-mode preamplifier with an active feedback loop operated at very low frequency is designed as the first gain stage to bypass any dc offset current generated by the electrode-tissue interface and to achieve a low high-pass cutoff frequency below 0.5 Hz. No reset signal or ultra-large pseudo resistor is required. The current-mode preamplifier has low dc operation current to enhance low-noise performance and decrease power consumption. A programmable current gain stage is adopted to provide adjustable gain for adaptive signal scaling. A following current-mode filter is designed to adjust the low-pass cutoff frequency for different neural signals. The proposed CMFEA is designed and fabricated in 0.18- μm CMOS technology and the area of the core circuit is 0.076 mm². The measured high-pass cutoff frequency is as low as 0.3 Hz and the low-pass cutoff frequency is adjustable from 1 kHz to 10 kHz. The measured maximum current gain is 55.9 dB. The measured input-referred current noise density is 153 fA/ $\sqrt{\text{Hz}}$, and the power consumption is 13 μW at 1-V power supply. The fabricated CMFEA has been successfully applied to the animal test for recording the seizure ECoG of Long-Evan rats.

Index Terms—Current-mode, front-end, low-noise low power design, neural recording, offset cancellation.

I. INTRODUCTION

IT is known that the acquisition device for neural signal recording is one of the most important components in a biomedical electronic system. In the acquisition device, the Front-End Amplifier (FEA) is one of the key elements, which senses and amplifies the neural signals such as Electroencephalography (ECoG), Electrocardiogram (ECG), action potential, local field potential (LFP) etc., through electrode-tissue interfaces. Since the amplitude of neural signals is very small and the electrodes are easily interfered by external noise sources

like 60-Hz noise from power lines or other disturbance sources, a low-noise FEA is required. With the increasing number of input electrodes required for clinical and implant applications, a FEA must meet the requirements of low power consumption and small chip area. The required low-pass cutoff frequency for neural signals varies from several hundred Hz to kilo Hz whereas the required high-pass cutoff frequency is below 0.1 Hz. Thus the low-pass cutoff frequency of FEAs should be adjustable. Moreover, the amplitude of the dc input offset voltage caused by the electrode-tissue interface varies with both material and size of electrodes. It must be eliminated to prevent the saturation of FEAs while amplifying neural signals below 0.1 Hz.

To reject the dc offset, the AC coupled techniques are proposed in some voltage-mode FEAs. In [1]–[3], MOS-bipolar or MOS pseudo resistors are adopted to realize ultra-large resistances which are highly dependent on the voltage across them. This causes large signal distortions and large variations of high-pass filter characteristics. Moreover, a reset signal is required [3] to reset the pseudo resistor and keep the bias condition stable. This makes the circuit design more complicated and the periodic reset signal causes the switched-capacitor effect which degrades the high-pass cutoff frequency. On the other hand, large external capacitors are used to achieve a high-pass cutoff frequency below 1 Hz [4], [5]. However, the use of discrete component increases the size of acquisition devices and limits the use of devices in implantable applications.

Generally, the internal nodes in current-mode circuits have low impedance characteristics and low voltage swings. Thus power supply voltage can be reduced to decrease the power consumption. The voltage noise is inversely proportional to dc operating current whereas the current noise is proportional to dc operating current. Thus current-mode circuits can achieve low noise under low power consumption.

Several current-mode circuits [6], [7] have been proposed for amplifier applications. In [6], a CMOS front-end amplifier for photo-current acquisition is presented with a feedback loop consisted of a sample-and-hold stage, an error amplifier, and a sinking device to bypass the flowing-out dc current. In [7], a trans impedance amplifier (TIA) consisted of an integrator followed by a differentiator is proposed to amplify the current signals of nanodevices. The dc offset current flows into the low-frequency feedback path and is rejected without affecting the in-band signal. However, the high-pass cutoff frequency (100 Hz–1 kHz) is too high for neural signals. The power dissipation is 45 mW which is not suitable for low-power FEAs.

In this paper, a new low-power current-mode front-end amplifier (CMFEA) for neural signal recording is proposed. In

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C.-Y. Wu is with the Department of Electronics Engineering, Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, and is also with the Biomedical Electronics Translational Research Center, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: peterwu@mail.nctu.edu.tw).

W.-M. Chen and L.-T. Kuo are with the Department of Electronics Engineering, Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan.

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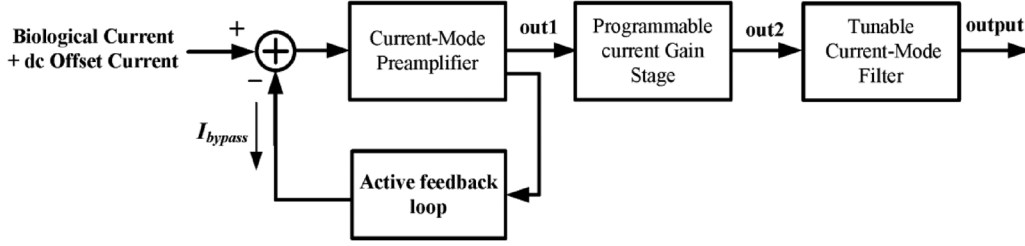


Fig. 1. Block diagram of the proposed current-mode front-end amplifier (CMFEA).

the proposed CMFEA, the biological signal current flowing in the input electrode-tissue interface as generated by the biopotential signal, is sensed and amplified. The proposed CMFEA can retain the advantages of low power consumption and low power supply in current-mode circuits. It also has a good noise rejection capability. As compared to the voltage-mode amplifiers, neither ultra-high value pseudo resistors with reset signals nor external large capacitors are required. Moreover, the current preamplifier with the cancellation feedback loop is designed to bypass the dc offset current generated by the electrode-tissue interface so that the dc offset current does not affect the amplifier operation.

The proposed CMFEA is designed and fabricated in $0.18\text{-}\mu\text{m}$ CMOS technology. The measurement results show that the high-pass cutoff frequency of 0.3 Hz can be achieved whereas the low-pass cutoff frequency can be adjusted from 1 kHz to 10 kHz . The measured input-referred current noise density is $153\text{ fA}/\sqrt{\text{Hz}}$. The power dissipation is $13\text{ }\mu\text{W}$ at 1-V power supply. The chip area is 0.576 mm^2 with 0.076 mm^2 of the core CMFEA circuit. The animal test on the ECoG signal recording of epileptic Long-Evan rats is demonstrated. These experimental results have verified that the proposed CMFEA is a potential solution for neural signal recording systems.

II. CIRCUIT DESIGN

The architecture of the proposed CMFEA is shown in Fig. 1 which consists of a current-mode preamplifier with an active feedback loop, a programmable current gain stage, and a tunable current-mode filter. The first stage is the current-mode preamplifier designed to amplify the in-band current signals. The incorporated active feedback loop is operated at a very low frequency to bypass the dc offset current generated from the electrode-tissue interface. The second stage is the programmable current amplifier which provides further amplification and adjustable signal gain for different neural signals. The third stage is a tunable current-mode filter. Its low-pass cutoff frequency is adjustable from 1 kHz to 10 kHz . A TIA is designed to convert the output current signal to voltage for measurement.

A. Current-Mode Preamplifier

Since the noise of the first stage is the dominate noise source, a current-mode preamplifier with low dc current is used as the first stage to suppress the noise contributed by this stage [8]. The structure of the current-mode preamplifier with low dc current is shown in Fig. 2(a) [8]. The operational amplifier OP_1 is designed with a two-stage topology as shown in Fig. 2(b) where the aspect ratio of $M_1(M_3)$ is identical to that of $M_2(M_4)$. In

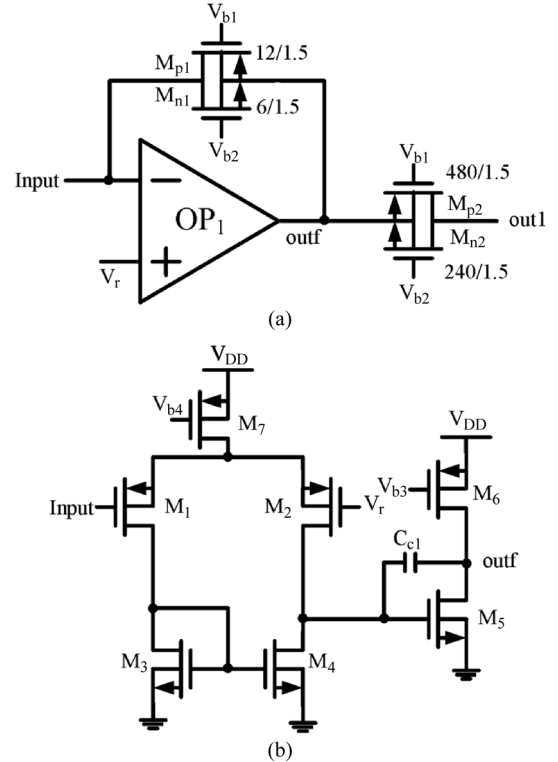


Fig. 2. (a) Structure of current-mode preamplifier. (b) Circuit schematic of OP_1 .

Fig. 2(a), the dc voltages of the input node and the node outf are set to $V_r = 1/2 V_{DD}$ (0.5 V) via the negative feedback loop of OP_1 . The voltage of out1 is also set to V_r via the negative feedback loop in the next stage. As a result, the dc drain-source voltages of M_{n1} , M_{n2} , M_{p1} , and M_{p2} are kept at 0 V . With $V_{b1} = 0.3\text{ V}$ and $V_{b2} = 0.7\text{ V}$, all devices are operated at a very low dc current in the linear subthreshold region as resistors. Since the channel lengths of $M_{p1}(M_{n1})$ and $M_{p2}(M_{n2})$ are the same, the resistance ratio of $M_{p2}(M_{n2})$ to $M_{p1}(M_{n1})$ is equal to the channel width ratio of $M_{p2}(M_{n2})$ to $M_{p1}(M_{n1})$ which is designed to be 40. With a small-signal input current i_1 flowing on M_{p1}/M_{n1} , the small-signal voltage across M_{p1}/M_{n1} is the same as that of M_{p2}/M_{n2} . Thus the current i_2 on M_{p2}/M_{n2} is equal to $40 i_1$ and a current gain of 40 can be obtained. The current-mode preamplifier in Fig. 2(a) has low input impedance and distortion.

In the OP_1 circuit of Fig. 2(b), $M_1 - M_2$ form an amplifier with the current-mirror load $M_3 - M_4$. Using PMOS as input devices can reduce the flicker noise. The OP_1 is designed

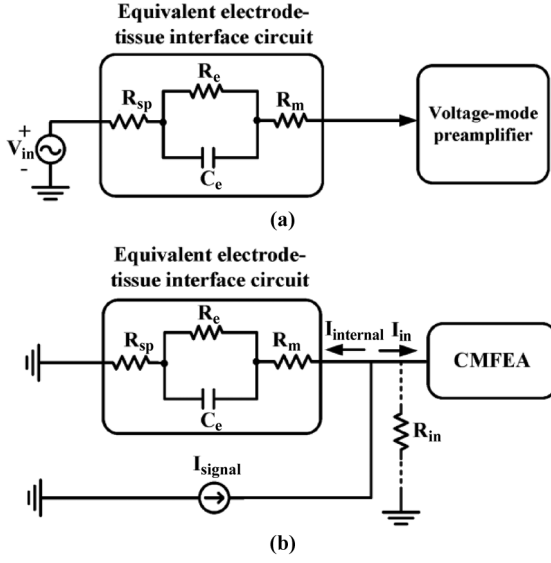


Fig. 3. (a) The equivalent electrode-tissue interface circuit with the voltage-mode preamplifier. (b) Norton equivalent circuit of the electrode-tissue interface circuit with the CMFEA.

to achieve low offset voltage with suitable gain. Therefore, the sizes of $M_1 - M_4$ which are the main contributions of offset are enlarged to decrease the offset caused by device mismatch.

The equivalent electrode-tissue interface circuit with the voltage-mode preamplifier is shown as Fig. 3(a). Its Norton equivalent circuit with the CMFEA is shown as Fig. 3(b). In Fig. 3, R_{sp} is the spreading resistance between electrolyte and tissue, R_e and C_e are the resistance and capacitance of the electrode-tissue interface, respectively, R_m is the resistance of the electrode, V_{in} is the neural potential signal, R_{in} is the input impedance of the CMFEA, I_{in} is the current signal injecting into the current-mode preamplifier, and $I_{internal}$ is the internal signal current flowing through the interface circuit in Fig. 3(b). Unlike voltage-mode preamplifiers whose input impedance should be designed as high as possible, the input impedance of current-mode preamplifier should be designed as low as possible to sense the input current signal. Thus the current signal generated by the neural signal on the input electrode-tissue interface can flow into the current-mode preamplifier with less degradation as can be seen from Fig. 3(b).

Note that the recorded current signal is generated by the neural potential signal on the input electrode-tissue interface and dependent on interface impedance. It can be used directly to extract physiological features like epileptic seizure occurrence. The recorded current signal can also be converted into the corresponding neural potential signal by using an analog TIA with the transimpedance equivalent to the electrode interface impedance.

Since the measured equivalent impedance of electrode is about 1 M Ω at dc and 100 k Ω at 10 kHz, the input resistance of the current-mode preamplifier is designed to be 4.6 k Ω which is determined by R_{Mn1} , R_{Mp1} , and the gain of OP_1 as

$$R_{in} = \frac{R_{Mn1} \parallel R_{Mp1}}{A_{OP1}} \quad (1)$$

where R_{Mn1} and R_{Mp1} are the turn-on resistance of M_{n1} and M_{p1} , and A_{OP1} is the gain of OP_1 which is designed to be 60 dB.

In the normal AC coupled voltage-mode preamplifier, the voltage signal in the kHz frequency range generates displacement current flowing in the electrode and input capacitor circuit. The displacement current is in the range of nA when the kHz voltage signal in the range of mV. In the proposed current-mode preamplifier, the input signal current is also in the range of nA when the kHz voltage signal in the range of mV.

The input referred current noise I_n of the current-mode preamplifier can be expressed as [8]

$$\overline{I_n^2} = \left[\frac{kT}{3} (g_{m-Mn1} + g_{m-Mp1}) + (2\pi f)^2 C_{in}^2 \overline{V_{op}^2} \right] \Delta f \quad (2)$$

where k is the Boltzmann constant, T is the absolute temperature, g_m is the transconductance of MOS device, f is the signal frequency, C_{in} is the input capacitance of OP_1 , V_{op} is the input referred voltage noise of OP_1 , and Δf is the bandwidth of the preamplifier.

The first term in (2) is mainly contributed by M_{p1}/M_{n1} and proportional to the transconductance. Thus, low dc currents in the devices M_{p1}/M_{n1} result in a low noise performance. Since M_{p2}/M_{n2} are operated at low dc currents and their noise contribution to the equivalent input noise is divided by the gain of 40, the noise influence of M_{p2}/M_{n2} is negligible.

In the second term in (2), V_{op} is contributed by the flicker noise $V_{n,op-flicker}$ and the thermal noise $V_{n,op-thermal}$ of the devices in OP_1 , which can be expressed as

$$\overline{V_{n,op}^2} = \overline{V_{n,op-thermal}^2} + \overline{V_{n,op-flicker}^2} \quad (3)$$

$$\overline{V_{n,op-thermal}^2} = \frac{16kT}{3} \frac{1}{g_{m1}^2} \quad (4)$$

$$\times \left[g_{m1} + g_{m3} + \frac{g_{m5} + g_{m6}}{2g_{m5}^2 (r_{o2} \parallel r_{o4})} \right] \quad (4)$$

$$\approx \frac{16kT}{3} \frac{1}{g_{m1}^2} [g_{m1} + g_{m3}] \quad (5)$$

$$\overline{V_{n,op-flicker}^2} = \frac{2K_p}{W_1 L_1 C_{ox} f} + \frac{2K_n}{W_3 L_3 C_{ox} f} \left(\frac{g_{m3}}{g_{m1}} \right)^2 + \frac{1}{g_{m2}^2 g_{m5}^2 (r_{o2} \parallel r_{o4})} \quad (6)$$

$$\times \left[\frac{g_{m5}^2 K_n}{W_5 L_5 C_{ox} f} + \frac{g_{m6}^2 K_p}{W_6 L_6 C_{ox} f} \right] \quad (6)$$

$$\approx \frac{2K_p}{W_1 L_1 C_{ox} f} + \frac{2K_n}{W_3 L_3 C_{ox} f} \left(\frac{g_{m3}}{g_{m1}} \right)^2 \quad (7)$$

$$= \frac{2}{C_{ox} f} \left[\frac{K_p}{W_1 L_1} + \frac{\mu_n K_n L_1}{\mu_p W_1 L_3^2} \right] \quad (8)$$

where r_o , W , L , C_{ox} , and μ are the output resistance, width, length, gate capacitance density, and the mobility of the MOS device, respectively, and K is the process-dependent constant of flicker noise. From (5), the thermal noise can be reduced by increasing g_{m1} . Thus, the bias current in the first stage of OP_1 is increased to increase g_{m1} and reduce the thermal noise contributed to the preamplifier. Since the flicker noise is inversely

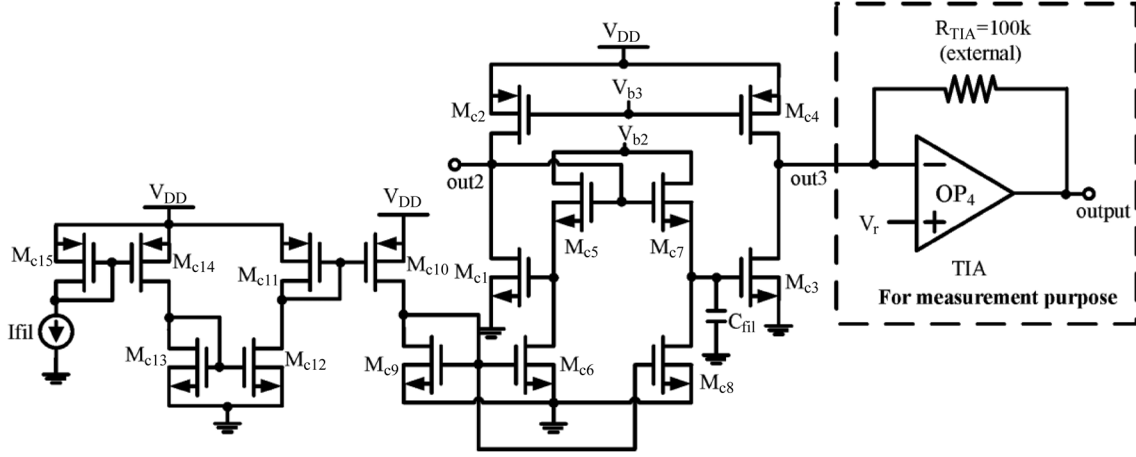


Fig. 6. Schematic of the first-order log-domain current-mode filter.

C. Programmable Current Gain Stage

Since the output dc voltage of out1 in the proposed current preamplifier of Fig. 2(a) has to be clamped to V_r by the next stage, a programmable current gain stage incorporated with a negative feedback loop is proposed as the second stage. The structure of the programmable current gain stage is shown in Fig. 5. Since the noise of the second stage is not the dominate source, the multi-stage current mirror is designed as the programmable current gain stage. In Fig. 5, OP₃ has a two-stage structure as shown in Fig. 2(b). It is used not only to clamp the voltage of out1, but also to reduce the input impedance of the stage. This also reduces the variations of input impedance with different input signal currents so that the signal distortion can be minimized and the linearity can be improved. The input impedance of the programmable current gain stage can be derived as

$$R_{in2} = \frac{1}{A_{OP3}g_{m3n}} \quad (11)$$

$$= \frac{nU_T}{A_{OP3}(I_{bias} + I_{in})} \quad (12)$$

where A_{OP3} is the gain of OP₃ and g_{m3n} is the transconductance of M_{3n} . M_{3n} is operated in the subthreshold region, thus the input impedance can be expressed as (12) where I_{bias} is the dc bias current in M_{3n} , and I_{in} is the input current signal flowing in to the programmable current gain stage. It can be seen from (12) that the input impedance is reduced by a factor of A_{OP3} . Thus the current injection efficiency can be increased.

The current amplification ratio is determined by the MOS size ratio. When S_1 turns on, the parallel-connection number of M_{3n} and M_{3p} is increased and the current gain is reduced. On the other hand, when S_1 turns off, the transistors of M_{3p1} and M_{3n1} are turned off and the current gain is increased. With digital control signals on the switches S_1 and S_2 , the number of parallel-connection transistors is selected to adjust the current gain. The current gain can be adjusted from 12 dB to 24 dB in four steps.

D. Tunable Current-Mode Filter

A first-order log-domain current-mode filter is used as shown in Fig. 6 [9] where the transistors M_{c1} , M_{c3} , M_{c5} , and M_{c7}

are operated in the weak inversion region. The low-pass cutoff frequency f_{LP} is described as

$$f_{LP} = \frac{I_{fil}}{2\pi nU_T C_{fil}} \quad (13)$$

where I_{fil} is the current of M_{c7} and M_{c8} , and C_{fil} is the capacitor used in the current-mode filter. From (13), the low-pass cutoff frequency of the current-mode filter can be designed at a very low frequency by applying a low I_{fil} without the use of large capacitance. By adjusting I_{fil} , the low-pass cutoff frequency of the CMFEA can be tuned from 1 kHz to 10 kHz.

In Fig. 6, the TIA with a 100 k external resistor is used to convert the output current signal to voltage signal for measurement purpose, since there is no measurement equipment available to measure the current signal directly. In the integration of the proposed CMFEA with ADC, the TIA with the external resistor is not required.

III. EXPERIMENT RESULTS

The proposed CMFEA has been designed and fabricated by TSMC 0.18- μm CMOS technology. The chip photograph of the fabricated circuit is shown in Fig. 7. The total chip area is 0.576 mm² including the ESD pad. The chip areas of the core circuit are 0.076 mm² and 0.135 mm² without and with the TIA, respectively.

In the measurement setup for functionality test, the input voltage signal is fed into the discrete circuit which is the same as the equivalent electrode-tissue interface circuit as shown in Fig. 3(a). Thus, the voltage signal can be converted into current signal through the discrete circuit and fed into the CMFEA.

The measured frequency response is shown in Fig. 8 where low-pass and high-pass cutoff frequencies are both tunable. The low-pass cutoff frequency is located in the range of 1 kHz to 10 kHz with $I_{fil} = 0.1$ nA to 1 nA as shown in Fig. 8(a) and Fig. 8(b), respectively. The high-pass cutoff frequency can be as low as 0.3 Hz when the input dc current is 5 nA. The maximum gain is 55.9 dB. The maximum input dc offset current which can be bypassed by the active feedback loop is 15 nA with the high-pass cutoff frequency remains below 1 Hz.

The measurement result of the THD is shown in Fig. 9 where the input signal has the maximum operation frequency (10 kHz)

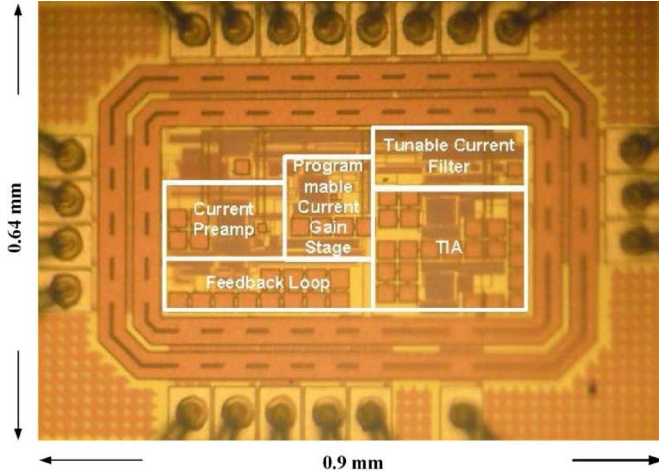


Fig. 7. Chip photograph of the fabricated CMFEA.

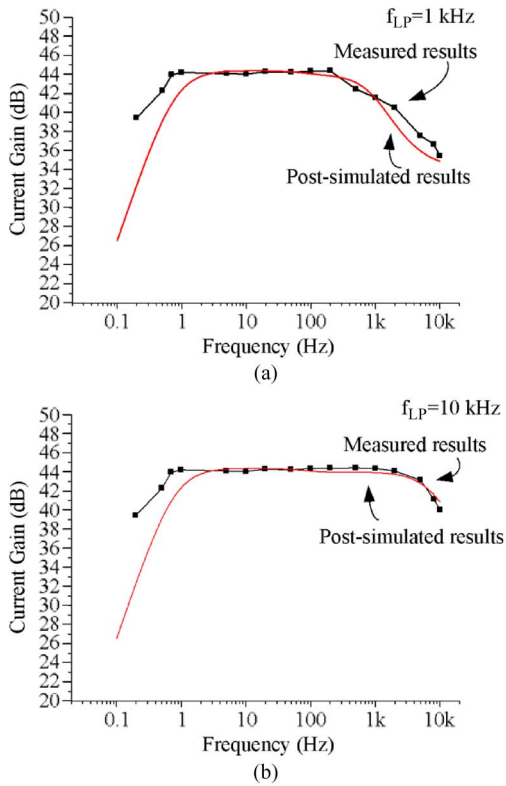


Fig. 8. The measured frequency response with (a) 1 kHz low-pass cutoff frequency and (b) 10 kHz low-pass cutoff frequency.

and 20 nAp-p peak-to-peak amplitude. It can be seen that under the maximum input signal 20 nAp-p which is much higher than the normal neural signal, the THD is 1.03%. Thus the proposed CMFEA has a low THD. The measured output current noise from 1 Hz to 10 kHz is shown in Fig. 10. The measured input-referred current noise is $15.3 \text{ pA}_{\text{rms}}$. By using the maximum input current of $7.07 \text{ nA}_{\text{rms}}$, the SNR or maximum dynamic range of the CMFEA can be calculated as $20 \log(7.07 \text{ nA}/15.3 \text{ pA}) = 53.29 \text{ dB}$.

The fabricated CMFEA chip is applied to the measurement of ECoG signals of Long-Evan rats. Fig. 11 shows the measurement setup of the animal test where the recording electrode is

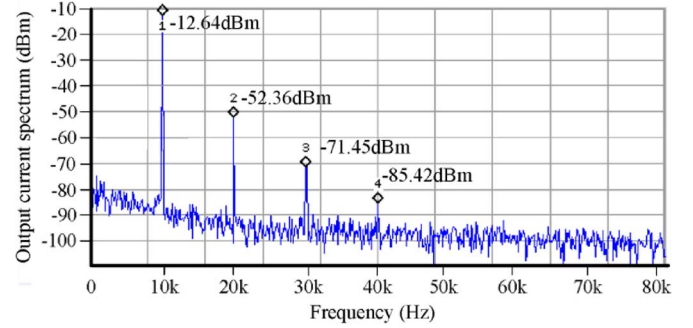


Fig. 9. The measured frequency spectrum of output current when $I_{in} = 20 \text{ nA}_{p-p}$ at 10 kHz.

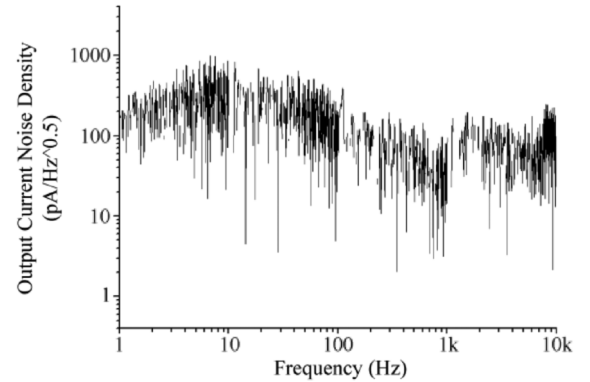


Fig. 10. The measured output current noise from 1 Hz to 10 kHz.

connected to the CMFEA with wire. The ECoG signal is sensed and amplified by the CMFEA and the amplified signal is measured by the oscilloscope.

Figs. 12(a) and (b) show the ECoG measurement results of the animal test in both time and frequency domains with the gain of CMFEA set to 55.9 dB. Fig. 12(a) shows the measured normal ECoG signal. As can be seen from Fig. 12(a) that the amplitude variations of the transient waveform are small and no specific component is shown on the spectrum. Fig. 12(b) shows the measured ECoG signal when the rat has epileptic seizures. In Fig. 12(b), the corresponding input current is around 0.3 nA. As can be seen from the measured spectrum, the main frequency components are around 7.5 Hz and 15 Hz which are identical with the measurement results of voltage-mode amplifiers.

The experimental results are summarized in Table I with the comparisons to other reported voltage-mode FEAs. With the same bandwidth of $7 \sim 10 \text{ kHz}$, the power consumption of the proposed current-mode front-end amplifier is less than other voltage-mode FEAs. The formula of the noise efficiency factor (NEF) is

$$NEF = V_{ni,rms} \sqrt{\frac{2I_{tot}}{4\pi U_T kTBW}} \quad (14)$$

where $V_{ni,rms}$ is the input-referred rms noise voltage, I_{tot} is the total supply current, and BW is the amplifier bandwidth. To calculate the NEF of the proposed CMFEA, the input noise current density referred to the input node of the electrode is converted to the input noise voltage density by multiplying the measured impedance of the electrode with $R_{sp} = 10 \text{ k}\Omega$, $R_e =$

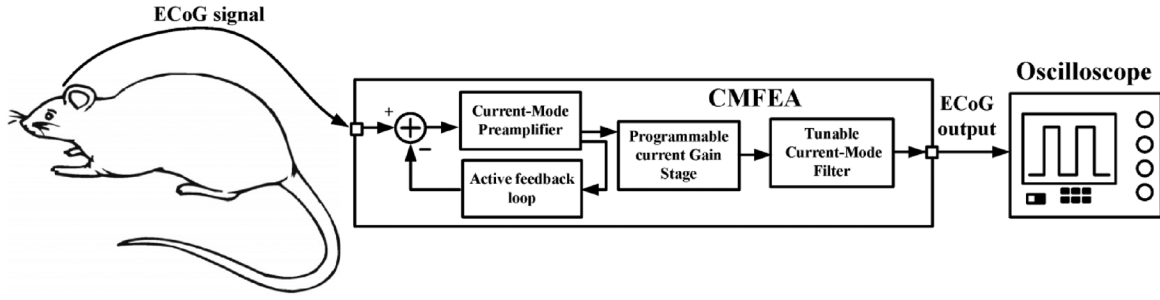


Fig. 11. The measurement setup of the animal test.

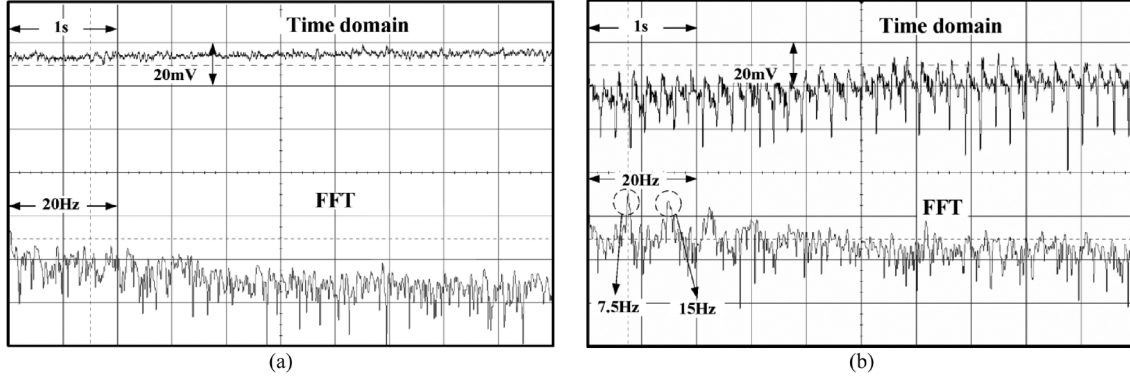


Fig. 12. The measured ECoG signals of the rat when in the (a) normal state and (b) epileptic seizure state.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF FEAS

	This Work	[1]	[5]	[10]	[11]	[12]
Technology	0.18 μm CMOS	1.5 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.35 μm CMOS
Area^a(mm²)	0.076 ^b /0.135 ^c	0.22	0.38	0.3	0.22	0.76
Topology	Current-mode	Voltage-mode	Voltage-mode	Voltage-mode	Voltage-mode	Voltage-mode
Supply Voltage (V)	1	± 2.5	1.5	1	1.5	3.3
Power (μW)	13	80	7.5	3.5	26.9	11.5 ^f /231 ^g
Gain (dB)	44.5/50/55.9 ^d	39.5 ^e	40.8 ^e	60 ^e	51.9/57.4/59.9/ 65.6 ^e	40~75 ^e
Bandwidth (Hz)	0.3~1k-10k	0.025~7.2k	0.5, 10~100-400	0.2~100	1.1~12k	2.6~6.2k
Input-referred Noise (integration bandwidth)	15.3 pArms/ 4.4 μVrms^i (10kHz)	2.2 μVrms (50kHz)	1.27 μVrms (100Hz)	1.3 μVrms (100Hz)	3.12 μVrms (50kHz)	2.3 ^f ~2.9 ^g Vrms (6kHz)
Large-value Resistor	None	Pseudo resistor	Pseudo resistor	Yes	Pseudo resistor	Pseudo resistor
External Capacitor	None	None	Yes	Yes	None	None
NEF	5.45 ⁱ 0.10 ^j	4	6.1	8.6	2.68 ^h	5.1

a. Area per channel. b. w/o TIA. c. w/TIA. d. Current gain. e. Voltage gain. f. Bandwidth of 200 Hz. g. Bandwidth of 200~6.2 kHz. h. Only the first stage. i. Referred to the input node of the electrode. j. Referred to the input node of the CMFEA.

900 k Ω , $C_e = 500$ pF and $R_m = 90$ k Ω as shown in Fig. 3(b). The calculated NEF of the CMFEA is 5.45. For the NEF re-

ferred to the input node of the CMFEA which is adopted in voltage-mode FEAs, the input impedance value of 4.6 k Ω and

NEF is 0.10. Unlike voltage-mode FEAs, the CMFEA has low input impedance which leads to low input noise voltage. Thus the calculated NEF of the CMFEA can be as low as 0.10.

IV. CONCLUSION

In this paper, a new CMOS current-mode front-end amplifier (CMFEA) for neural signal recording is proposed. In the proposed CMFEA, both bandwidth and current gain are all tunable for different neural signals. Through an active feedback loop incorporated with the first-stage current-mode preamplifier, the high-pass cutoff frequency can achieve 0.3 Hz and the dc offset current caused by electrode-tissue interface can be bypassed. No reset signal or ultra-high value pseudo resistor is needed in the CMFEA. The measured input referred current noise density is $153 \text{ fA}/\sqrt{\text{Hz}}$ with the bandwidth up to 10 kHz. The power dissipation is $13 \mu\text{W}$ at 1-V power supply. The proposed CMFEA is also applied to the animal test successfully to measure the epileptic ECoG of rats. The experimental results have demonstrated that the CMFEA is a promising solution for designing low-noise and low-power neural recording amplifiers.

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Chung-Yu Wu (S'76–M'76–SM'96–F'98) was born in 1950. He received the M.S. and Ph.D. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1976 and 1980, respectively.

Since 1980, he has been a Consultant to high-tech industry and research organizations and has built strong research collaborations with high-tech industries. From 1980 to 1983, he was an Associate Professor with National Chiao Tung University.

From 1984 to 1986, he was a Visiting Associate Professor with the Department of Electrical Engineering, Portland State University, Portland, OR, USA. Since 1987, he has been a Professor with National Chiao Tung University. From 1991 to 1995, he served as the Director of the Division of Engineering and Applied Science, National Science Council, Taiwan. From 1996 to 1998, he was bestowed as the Centennial Honorary Chair Professor of National Chiao Tung University. From 2007 to 2011, he served as the President of National Chiao Tung University. He is currently a Chair Professor of National Chiao Tung University and the Director General of the National Program on Nano Technology, Taiwan. He has authored or coauthored more than 300 technical papers in international journals and conferences. He holds 30 patents, including 17 U.S. patents. His research interests are biomedical electronic devices and systems, intelligent bio-inspired vision sensor systems, nanoelectronic circuits and systems for RF/microwave communication.

Dr. Wu is a member of Eta Kappa Nu and Phi Tau Phi. He was a recipient of the 1998 IEEE Fellow Award and a 2000 Third Millennium Medal. He was also the recipient of numerous research awards presented by the Ministry of Education, National Science Council (NSC), and professional foundations in Taiwan (1999–2003).



Wei-Ming Chen (S'12) was born in Hsinchu, Taiwan, in 1979. He received the B.S. degree in electrophysics and the M.S. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2003 and 2005, respectively.

Currently, he is working toward the Ph.D. degree at the Institute of Electronics, National Chiao Tung University. His major research interests are biomedical electronics and analog integrated circuits design.



Liang-Ting Kuo was born in Tainan, Taiwan, in 1987. He received the B.S. and M.S. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2009 and 2011, respectively.

Recently, he worked at MediaTek, Hsinchu, Taiwan, on analog integrated circuit design.