Implantable Stimulator for Epileptic Seizure Suppression With Loading Impedance Adaptability

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***Abstract*—The implantable stimulator for epileptic seizure suppression with loading impedance adaptability was proposed in this work. The stimulator consisted of the high voltage generator, output driver, adaptor, and switches, can constantly provide the required 40-μA stimulus currents, as the loading impedance varied within 10 kΩ–300 kΩ. The performances of this design have been successfully verified in silicon chip fabricated by a 0.35-μm 3.3-V/24-V CMOS process. The power consumption of this work was only 1.1 mW–1.4 mW. The animal test results with the fabricated chip of proposed design have successfully verified in the Long-Evans rats with epileptic seizures.**

***Index Terms*—Adaptability, epilepsy, epileptic seizure suppression, implantable device, stimulator.**

I. Introduction

THERE are $\sim 1\%$ of the people in the world affected by the epilepsy [1], [2]. This disease is caused by transient abnormal discharge in brain, and it is one of the common neurological diseases [3]–[5]. If this seizure cannot be well controlled, the patients will be affected in sensations, emotions, memories, and other related activities. Typically, the epileptic seizure can be treated by pharmacologic or surgical treatments. The most common way to suppress epileptic seizure is the pharmacologic treatment [6]–[8]. There are more than 20 types of medications for specific types of epileptic seizures. However, there are still many patients who can not be cured by the medications [9]. For these medically refractory patients, an alternative is the surgical treatment [10]–[12]. In this treatment, some tissues with abnormal discharge will be removed from the brain. It is a risky treatment because patients may loss some physical functions permanently after taking the surgery. In addition, some patients still can not be completely cured by the surgery [13], [14].

In recent years, the new techniques of electrical stimulation, such as the vagus nerve stimulation and deep brain stimulation [15]–[17], have been demonstrated to suppress the abnormal discharge signal before epileptic seizure happen. Comparing with the traditional treatments, the electrical stimulation is more harmless, flexible, recoverable, and less-destructive [18], [19]. Therefore, many epilepsy control systems by using electrical stimulation have been studied. Fig. 1 shows the functional block diagram of a closed-loop epileptic seizure monitoring and controlling system in an implantable device [20]–[22]. This implantable device consists of the detector, signal processor, and stimulator to form a closed-loop seizure controller.

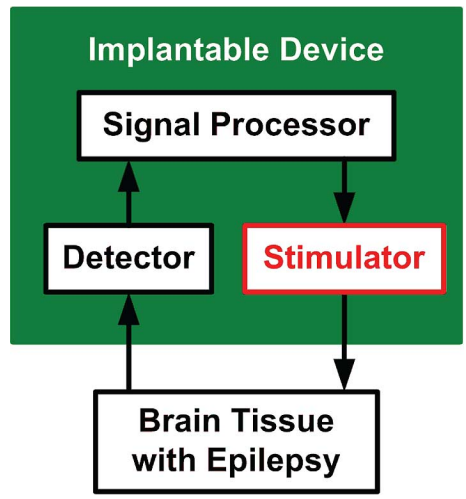

Fig. 1. Block diagram of implantable device for epileptic seizure suppression.

In the animal test of Long-Evans rats with epileptic seizures shown in [20], the required stimulus current to suppress the seizure is found to be 40 μA. Besides, due to different tissues, locations, distances, and implanted time, the effective loading impedance of stimulator will vary from 100 kΩ to 250 kΩ. Therefore, the stimulator with loading impedance adaptability is needed.

To deliver the stimulus current with the varied loading impedance, some approaches have been studied. For example, the stimulator can monitor the loading impedance first, and then setting the operating voltage [23], [24]. Of course, the monitoring circuit adds more area and complexity to the stimulator.

In this work, the integrated circuit design of implantable stimulator for epileptic seizure suppression with loading impedance adaptability and low power consideration is proposed [25]. This proposed stimulator can deliver bi-phasic stimulus currents by two leads electrode per stimulus site [26] with single supply voltage ($V_{\rm DD} = 3.3$ V). The required high voltage of stimulator can be adjusted to reduce the power consumption. The detailed design procedures of the stimulator will be presented in Section II. A 0.35-μm 3.3-V/24-V CMOS process is used

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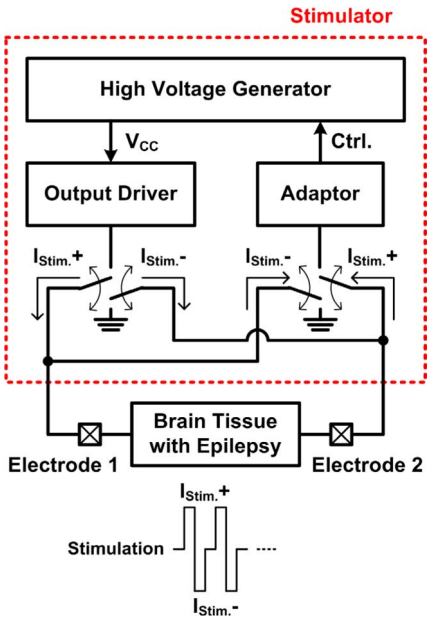


Fig. 2. Block diagram of stimulator with loading impedance adaptability.

in this work for the chip implementation. The measurement results in silicon chip will be presented in Section III. The comparison among the reported on-chip stimulators in recent literature [27]–[29] and this design will be summarized in Section IV. The animal test results in the closed-loop epileptic seizure monitoring and controlling system will be presented in Section V.

II. Proposed Stimulator Design

Fig. 2 shows the proposed stimulator, which consists of a high voltage generator, an output driver, an adaptor, and switches. The proposed stimulator adopts two leads electrode set per stimulus site (electrode 1 and electrode 2) to generate bi-phasic stimulus currents. Once the detector of implantable device in Fig. 1 detects the epileptic seizure, the stimulator becomes active. Under stimulation, the positive stimulus current $(I_{\mathrm{Stim.}}+)$ will flow through the output driver, electrode 1, brain tissue, electrode 2, and adaptor, while the negative stimulus current $(I_{\mathrm{Stim.}}-)$ will flow through the output driver, electrode 2, brain tissue, electrode 1, and adaptor. The high voltage generator is used to supply the variable voltage (V_{CC}) to output driver, and it is controlled by the feedback signal from adaptor (Ctrl.). Since the targeted stimulus current is 40 μA and the loading impedance varies from 100 kΩ to 250 kΩ, the voltage difference between two electrodes is between 4 V and 10 V. In other word, the required supply voltage for output driver (V_{CC}) must be as high as 10 V, which is much higher than the supply voltage $(V_{\mathrm{DD}} = 3.3\ \mathrm{V})$. Therefore, the high voltage generator is used to provide the variable high voltage. To reduce the power consumption in stimulator, the high voltage generator can output the different voltage level according to the different loading impedance.

The design and operation of the output driver, adaptor, high voltage generator, and switches will be discussed in following paragraphs.

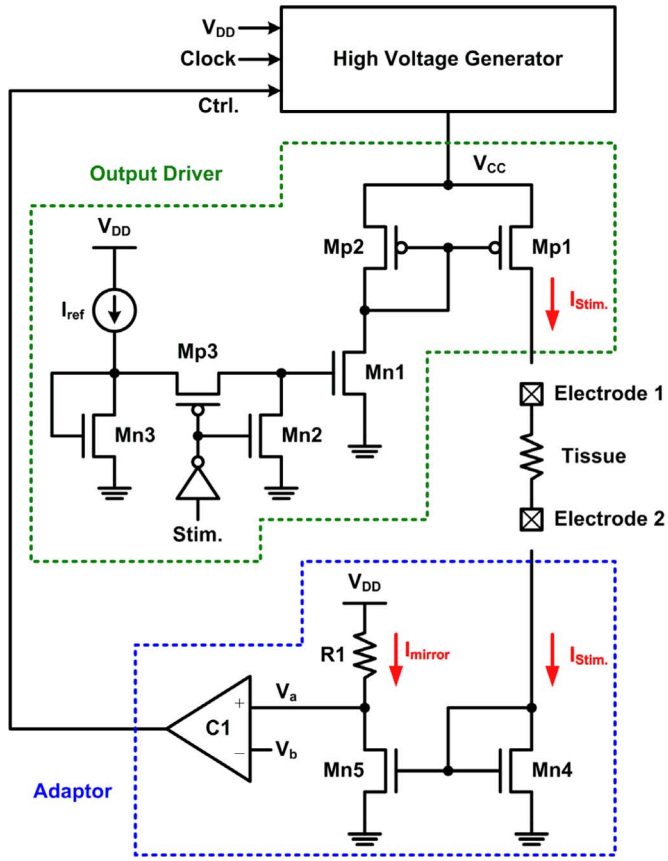


Fig. 3. Schematic circuits of output driver and adaptor.

A. Output Driver

The schematic circuits of the output driver and adaptor are shown in Fig. 3. In the output driver, the stimulus current source consists of a current mirror (Mp1 and Mp2) and bias circuit (Mn1, Mn2, Mn3, Mp3, and I_{ref}). The 3.3-V supply voltage (V_{DD}), variable voltage (V_{CC}), and stimulation signal (Stim.) are used in this circuit. The I_{ref} is used to provide the bias voltage for the gate terminal of Mn1. During the stimulation "on" interval, the stimulation signal is high $(\mathrm{Stim.} = 3.3\ \mathrm{V})$, Mn2 is turned off, Mp3 is turned on, and Mn1 is biased through Mp3. The Mn1 is biased to operate in saturation region under stimulation. The Mp1 and Mp2 are also designed to operate in saturation region under stimulation. The V_{CC} voltage will increase or decrease to keep delivering 40-μA stimulus current $(I_{\mathrm{Stim.}})$ under stimulation. Besides, if the V_{CC} is initially stored at higher voltage and applied to the lower loading impedance, the I_{ref} can limit the $I_{\mathrm{Stim.}}$ at $\sim 40\ \mu$A. The I_{ref} can also prevent the tissue from large glitch current. During the stimulator "off" interval, the stimulation signal is low $(\mathrm{Stim.} = 0\ \mathrm{V})$. Mn2 is turned on and Mn1 is turned off, so there is no stimulus current delivered.

B. Adaptor

The adaptor of stimulator consists of a current mirror (Mn4 and Mn5), resistor (R1), and comparator (C1), as shown in Fig. 3. During the stimulation "on" interval, the positive (negative) stimulus current passes through tissue and electrode 2 (electrode 1), and then flows into the adaptor. In the

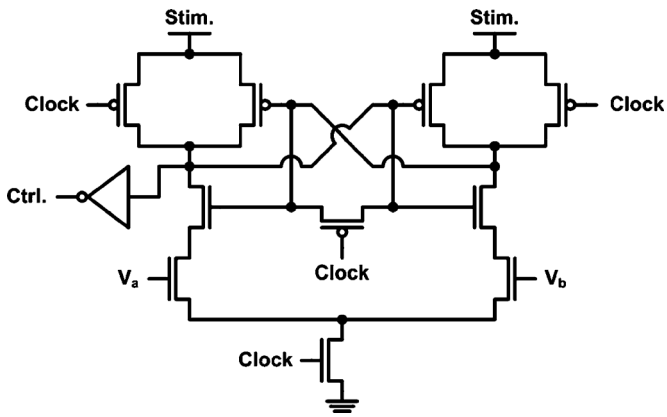


Fig. 4. Low-power comparator used in adaptor.

meantime, the positive or negative stimulus current $(I_{\mathrm{Stim.}})$ flows into the Mn4 of current mirror. The gate terminal of Mn5 is biased to induce the proportional current (I_{mirror}). In this work, the Mn4 and Mn5 are designed to keep the $I_{\mathrm{Stim.}}$ equal to I_{mirror}. The adaptor utilizes I_{mirror} flowing through resistor $(R1 = 41.25\ \mathrm{k}\Omega)$ to generate a voltage signal $(V_a = V_{\mathrm{DD}} - I_{\mathrm{mirror}} \times R1)$. Another voltage signal (V_b) which is used to compare with V_a is $0.5 \times V_{\mathrm{DD}}$. Since the V_b voltage is kept at $0.5 \times V_{\mathrm{DD}}$, it can be divided from V_{DD}. Whenever the stimulator is turned on to stimulate the brain tissue, the comparator in the adaptor compares these two voltage signals (V_a and V_b) and distinguishes the amplitude of stimulus current. The variable supply voltage (V_{CC}) for output driver can be controlled by the output of comparator (Ctrl.). If the I_{mirror} is lower than 40 μA, which leads to V_a higher than V_b, the output of comparator will become high $(\mathrm{Ctrl.} = 3.3\ \mathrm{V})$. The high voltage generator will keep pumping to provide higher voltage until the I_{mirror} reaches 40 μA. Once the I_{mirror} is higher than 40 μA, which leads to V_a lower than V_b, the output of comparator will become low $(\mathrm{Ctrl.} = 0\ \mathrm{V})$. The high voltage generator will stop pumping to provide lower voltage until the I_{mirror} returns 40 μA. The feedback design of adaptor keeps the stimulus current at $\sim 40\ \mu$A.

The comparator used in the adaptor is shown in Fig. 4 [30]. Under stimulation $(\mathrm{Stim.} = 3.3\ \mathrm{V})$, the comparator turns on. When the clock signal is low, the comparator is pre-charged, and there is no dc current path from power to ground. When the clock is high, the comparator compares the V_a and V_b, and the feedback loop latches the comparator into steady state. In steady state of comparator, there is also no dc current path from power to ground. The comparator without dc current is very power-saving.

During the stimulator "off" interval, the stimulation signal (Stim.) is equal to 0 V, so the last-stage inverter of comparator outputs high signal $(\mathrm{Ctrl.} = 3.3\ \mathrm{V})$. Even so, the Stim. stops the high voltage generator from pumping to high voltage in this interval.

C. High Voltage Generator

The high voltage generator of stimulator uses the charge-pump-based circuit, as shown in Fig. 5(a). The high voltage generator consists of the 4-stage charge pump circuit,

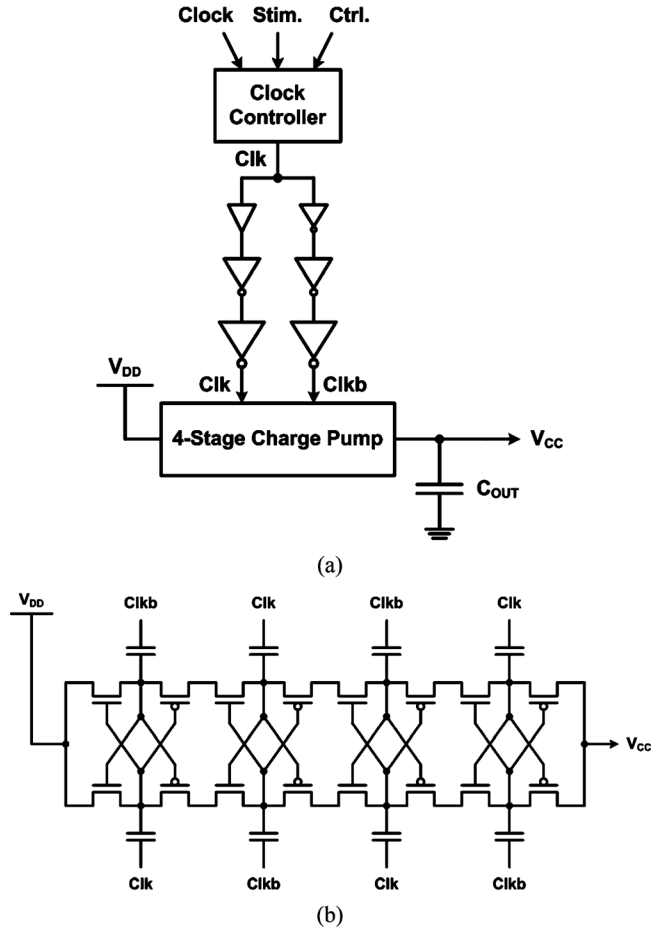


Fig. 5. Design of (a) high voltage generator and (b) 4-stage charge pump circuit.

clock controller, clock buffers, and output capacitor (C_{OUT}). The clock controller is utilized to generate the frequency-modulated clock signal (Clk) which depends on the reference clock signal (Clock), stimulation signal (Stim.), and the feedback signal from comparator (Ctrl.).

During the stimulator "on" interval, the stimulation signal is high, and the clock controller starts to send the frequency-modulated clock signal to the 4-stage charge pump circuit. If the Ctrl. signal is low, the reference clock signal is modulated to the lower-frequency output (Clk). Likewise, if the Ctrl. signal is high, the reference clock signal is modulated to the higher-frequency Clk. During the stimulator "off" interval, the stimulation signal is low $(\mathrm{Ctrl.} = 0\ \mathrm{V})$, and the Clk signal also keeps at 0 V, so the 4-stage charge pump circuit stops pumping.

The used 4-stage charge pump circuit is shown in Fig. 5(b). This charge pump circuit has been studied to output the high voltage $(>V_{\mathrm{DD}})$, but it will not suffer the gate-oxide reliability issue [31]. There is a compromise between capacitor size and clock frequency, so the used reference clock frequency is 25 MHz, and each capacitor in 4-stage charge pump is 15 pF. The output voltage (V_{CC}) of the 4-stage charge pump circuit with 3.3-V V_{DD} supply can be ideally pumped up to ~ 16 V.

At the beginning of operation, there is no charge stored at the output capacitor (C_{OUT}) of high voltage generator, and the output voltage (V_{CC}) is initially 0 V. Under stimulation, the

charge pump circuit starts to pump to high voltage. If the Ctrl. signal is high, the charge pump circuit keeps pumping to higher voltage. Therefore, the output voltage of high voltage generator increases, and stimulus voltage is delivered from the charge pump. The charge pump circuit keeps pumping until the stimulus current is slightly higher than 40 μA to cause that V_a is lower than V_b in the adaptor, that is to say, the Ctrl. signal becomes low. The inactivated charge pump circuit causes that output voltage of high voltage generator and stimulus current decrease. Therefore, by changing the state of charge pump circuit instantaneously, the output voltage of high voltage generator keeps at the required high voltage.

During the stimulator "off" interval, the Clk signal keeps at low to inactive the charge pump circuit. Although the charge pump circuit stops pumping, some charges still store in the output capacitor $(C_{\rm OUT})$ to keep the $V_{\rm CC}$ at higher voltage within a short time. The $C_{\rm OUT}$ used in this work is 15 pF, and the time constant to discharge the $C_{\rm OUT}$ during the stimulator "off" interval is ~ 0.6 ms.

D. Switches

The switches are used to conduct positive and negative stimulus currents ($I_{\rm Stim.}+$ and $I_{\rm Stim.}-$). Besides stimulation intervals, the switches are shorted to ground to prevent from charge accumulation in brain tissue.

E. Simulation Results

The proposed stimulator has been simulated in HSPICE with the 0.35-μm 3.3-V/24-V CMOS process. Fig. 6 shows the voltage/current waveforms of $V_{\rm CC}$, tissue, and V_a as one stimulation with loading impedance (R_L) is 300 kΩ. During 0–2 μs, the stimulation signal is low, and the stimulus current keeps at 0 A. In the same duration, the $V_{\rm CC}$ is initially set at 3 V, which simulates the voltage stored in the output capacitor $(C_{\rm OUT})$ from previous stimulation. During 2–10 μs, the stimulation signal is high, and the stimulus current is sent. The required time for stimulus current to reach 40 μA is 1.26 μs. After that, the stimulus current keeps at ~ 40 μA once the stimulation signal keeps at high. In this time period, the voltage of V_a moves around $V_b(1.65$ V), and the voltage of $V_{\rm CC}$ also moves around ~ 14 V, as shown in Fig. 6(a). Although it seems an oscillation, the waveform is controlled by the adaptor. As V_a is higher than V_b, the high voltage generator pumps the $V_{\rm CC}$ to higher voltage. While V_a is lower than V_b, the high voltage generator stops pumping, so the $V_{\rm CC}$ decreases. The stability and reliability of this circuit have been considered in design phase [32]. In this stimulation of current pulses with $\pm$40-μA amplitude, 0.5-ms pulse width, 2.5-ms period, and 0.5-s duration, the total power consumption of the stimulator is 0.9 mW in which 0.6 mW is consumed in the high voltage generator, 0.11 mW is consumed in the output driver, 0.1 mW is consumed in the adaptor, and 0.09 mW is consumed in the switches.

The stimulation with different loading impedance is also simulated. The stimulus current always keeps at ~ 40 μA as the loading impedance varies from 10 kΩ to 300 kΩ. The simulated $V_{\rm CC}$ as the loading impedance varies from 10 kΩ to 300 kΩ are 7–14 V. The efficiency of high voltage generator calculated according to [33] is $\sim 50\%$. The total power consumption of the stimulator is 0.4–0.9 mW, as shown in Fig. 7. Fig. 7 also compares the power consumption of the traditional design with constant $V_{\rm CC}$ and that of the proposed design with adaptor to adjust $V_{\rm CC}$ voltage. Although additional power is consumed in the adaptor, the proposed design can reduce the total power consumption in low impedance region.

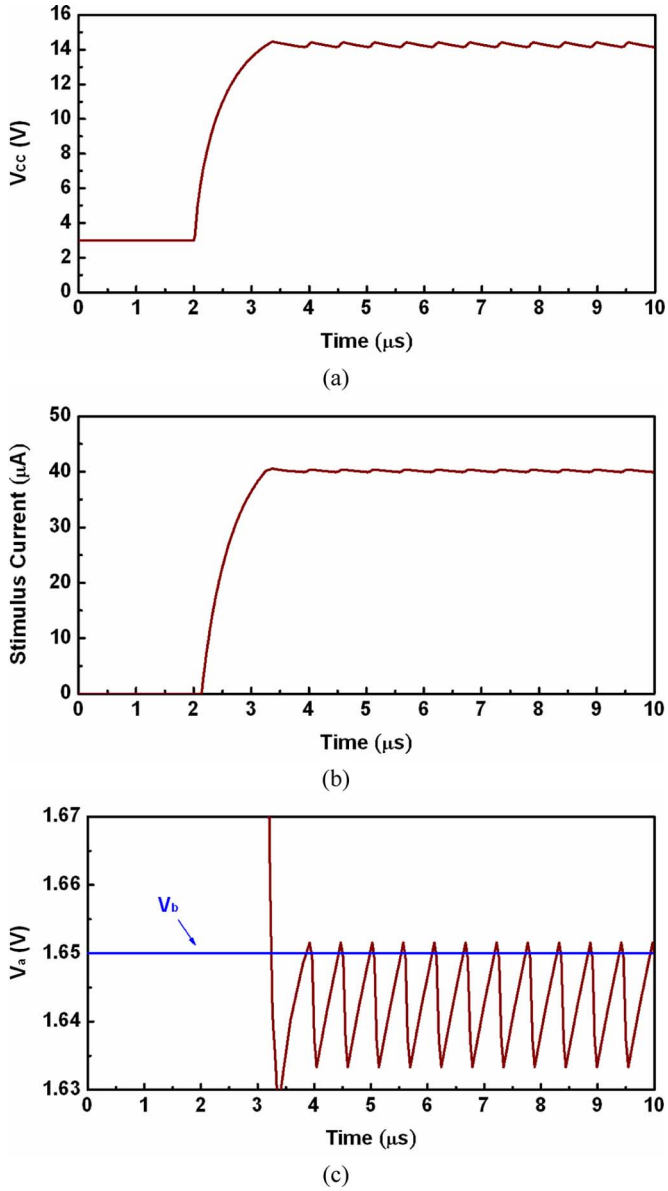


Fig. 6. Simulated voltage/current waveforms of (a) $V_{\rm CC}$, (b) $I_{\rm Stim.}$, and (c) V_a, as loading impedance is 300 kΩ.

III. Verification in Silicon Chip

The proposed bi-phasic stimulator to suppress epileptic seizure with loading impedance adaptability and low-power consideration has been fabricated in the 0.35-μm 3.3-V/24-V CMOS process. Fig. 8 shows the chip photograph of the fabricated stimulator. The occupied area of the proposed stimulator

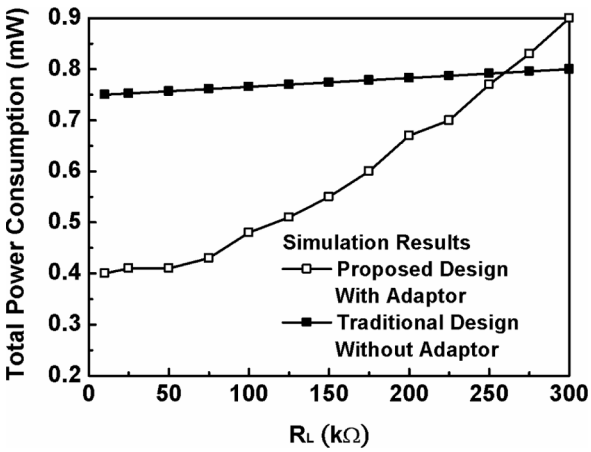


Fig. 7. Simulated total power consumption of stimulator as loading impedance varies from 10 kΩ to 300 kΩ.

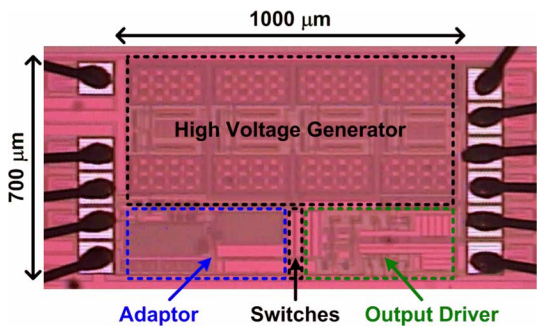


Fig. 8. Chip photograph of fabricated chip.

is about $1000 \times 700\ \mu\mathrm{m}^2$. The chip has been assembled in package for measurement.

Under measurement, Agilent E3631A is used to provide the fixed 3.3-V V_{DD}. Hp 33120A is used to supply the 25-MHz reference clock signal and to send the stimulation signal. Tektronix 3054B is used to observe the stimulus voltage/current in the loading.

While stimulation signal is given, the proposed design starts to deliver the stimulus current. Fig. 9 shows the stimulus current with 300-kΩ loading impedance. In this stimulation, the measured waveforms of V_{CC}, $I_{\mathrm{Stim.}}$, and V_a during -2–$8\ \mu$s are shown in Fig. 10. In this duration, the voltage of V_a moves around V_b (1.65V), and the voltage of V_{CC} moves around ~ 15 V to keep the stimulus current at $\sim 40\ \mu$A with the ripple of $\sim 1\ \mu$A. Besides, once the loading impedance is modeled as a series resistor and capacitor, the measured stimulus current with loading impedance of 300-kΩ resistor and 1-μF capacitor in series is also shown in Fig. 9.

Fig. 11 summarizes the measurement results of stimulus currents when the loading impedance varies from 10 kΩ to 300 kΩ. Although the stimulus currents vary 12% over the load range, the difference should be low enough to prevent from charge imbalance issue. Because the negative stimulus current follows the positive stimulus current immediately during the stimulation, and the loading impedance of stimulator will not change instantaneously, the same positive and negative stimulus currents can be provided. Fig. 12 summarizes the operating voltage

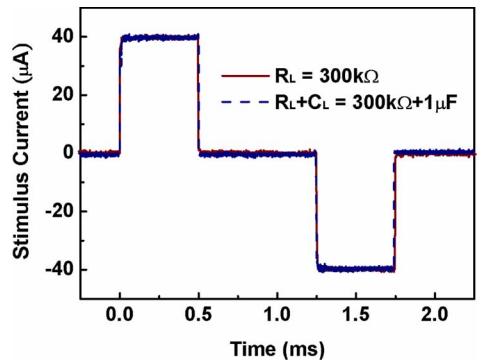


Fig. 9. Measured stimulus currents as loading impedance are 300 kΩ and 300 kΩ + 1 μF.

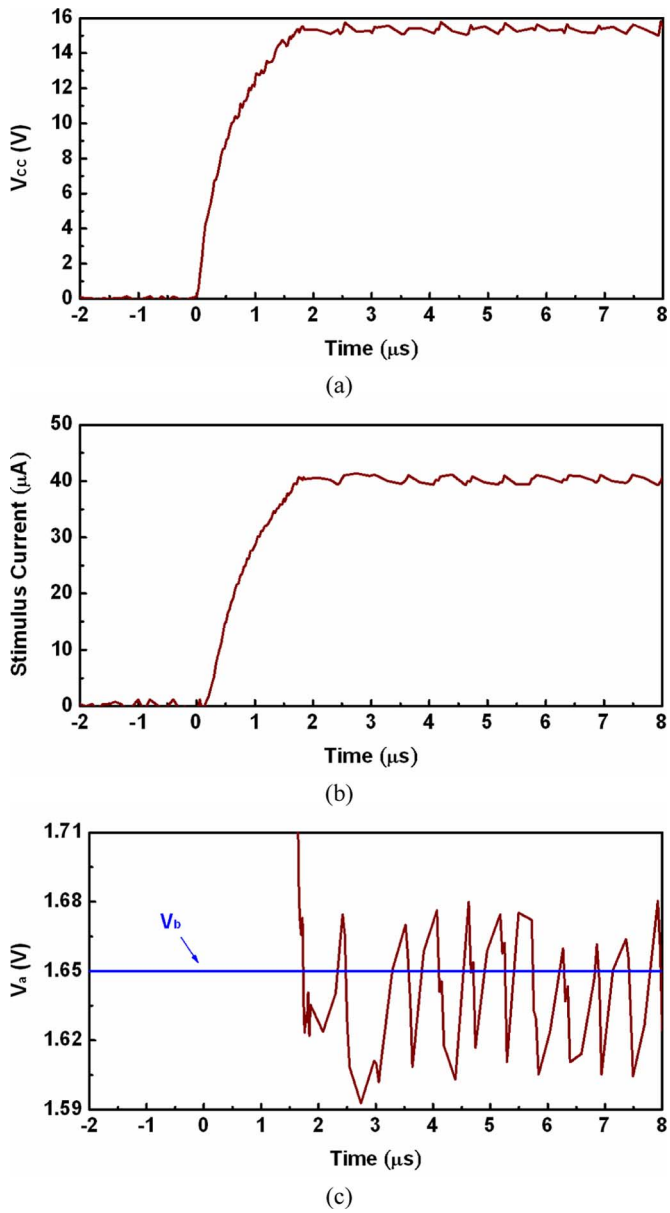


Fig. 10. Measured voltage/current waveforms of (a) V_{CC}, (b) $I_{\mathrm{Stim.}}$, and (c) V_a, during -2–$8\ \mu$s as loading impedance is 300 kΩ.

(V_{CC}) and total power consumption of stimulator verses loading impedance. Although the measured V_{CC} was little higher than

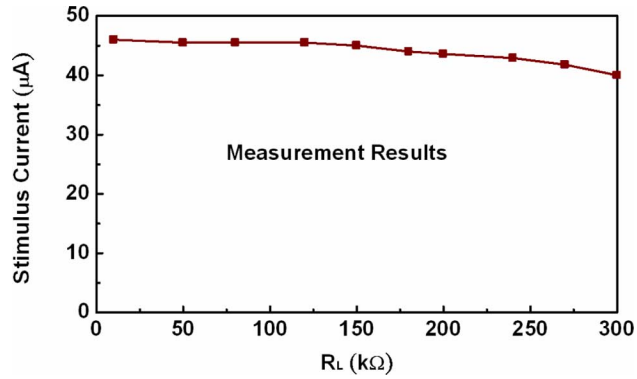


Fig. 11. Measured stimulus current as loading impedance varies from 10 kΩ to 300 kΩ.

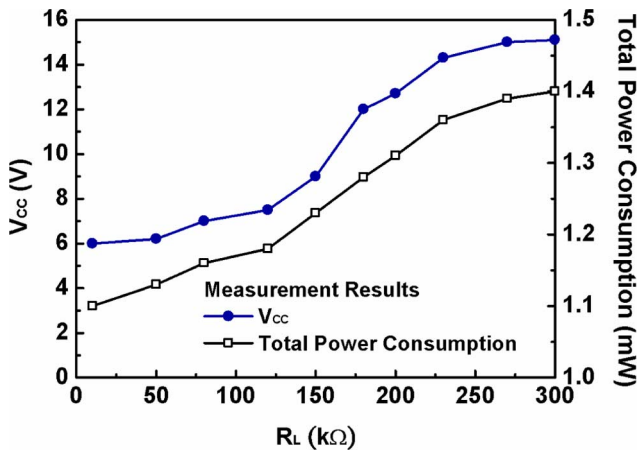


Fig. 12. Measured variable supply voltage (V_{CC}) and total power consumption of stimulator as loading impedance varies from 10 kΩ to 300 kΩ.

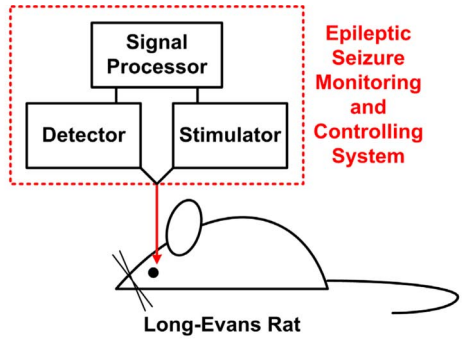
TABLE I
SUMMARY OF PROPOSED STIMULATOR

Technology	**0.35-μm 3.3-V/24-V CMOS Process**
Layout Area	**1000 x 700 μm²**
Electrode Configuration	**Two Leads Per Site**
Stimulus Current ($I_{Stim.}$)	**~40 μA**
Loading Impedance (R_L + C_L)	**10 ~ 300 kΩ and 1 μF**
Supply Voltage (V_{DD})	**3.3 V**
Power Consumption	**1.1 ~ 1.4 mW**

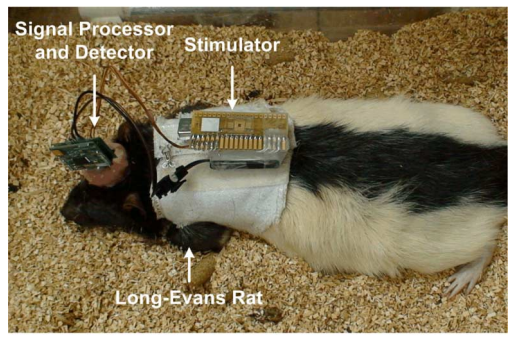
the simulated one, the 40-μA stimulus currents can be constantly provided. The average power consumption of the stimulator is 1.1–1.4 mW. The higher power is consumed in the comparator (C1), which is mostly consumed as clock transition, so the comparator design can be further optimized to reduce the power. For example, the clock frequency used in the comparator can be decreased to lower the power consumption. All of measurement results are summarized in Table I.

IV. COMPARISON

The comparison among the reported on-chip stimulators in recent literature [27]–[29] and this design is summarized in Table II. To sustain high stimulus voltage caused by the product of loading impedance and stimulus current, high-voltage processes are usually used. In this work, the stimulator has been designed to deliver the required stimulus current by using low supply voltage (3.3 V). Since the other circuit blocks of the implantable device use the same supply voltage, the stimulator can be easily integrated into the implantable device as a system in package (SiP).



(a)



(b)

Fig. 13. Measurement setup for animal test.

V. ANIMAL TEST

The fabricated chip of proposed stimulator has been further integrated into the closed-loop epileptic seizure monitoring and controlling system [20] for animal test. The stimulator originally used in [20] is replaced by the fabricated chip, while the other blocks remain. The measurement setup for animal test is shown in Fig. 13(a), and the photograph of the implantable device with Long-Evans rat for tests is shown in Fig. 13(b). All these experimental procedures have been reviewed and approved by Institutional Animal Care and Use Committee of National Cheng-Kung University, Taiwan.

In this experiment, the detection electrodes were bilaterally implanted over the area of the frontal barrel cortex (anterior 2.0 mm, lateral 2.0 mm with regard to the bregma). The stimulus current is conducted by a 4-microwire bundle, each made of Teflon-insulted stainless steel wire, to stimulate the right-side zona incerta of Long-Evans rat (posterior 4.0 mm, lateral 2.5 mm, and depth 6.7–7.2 mm). The diameter of the microwire (#7079, A-M Systems) is 50 μm. The ground electrode was implanted 2 mm caudal to lambda. Whenever the system detects an epileptic seizure, the proposed stimulator is activated. The stimulus current of pulse train with $\pm$40-μA amplitude, 0.5-ms pulse width, 2.5-ms period, and 0.5-s duration is used to suppress the

TABLE II
COMPARISON AMONG CURRENT STIMULATORS IN RECENT LITERATURE

	[27]	[28]	[29]	This Work
Technology	1.5-μm CMOS	0.8-μm CMOS	0.35-μm CMOS	0.35-μm CMOS
Loading Impedance	1.15 kΩ and 0.98 μF	100 kΩ	24 ~ 200 kΩ and 1 μF	10 ~ 300 kΩ and 1 μF
Stimulus Current	136 μA	0~136 μA	30 μA	40 μA
Current Type	Constant	Exponential	Constant	Constant
Duty Cycle	N/A	N/A	40 %	40 %
Stimulation Channel	15	4	1	1
Supply Voltage	±1.75 V	3.3 V	12~22 V	3.3 V
Power Consumption	2.22 mW	51.37 mW [1]	0.24 ~ 0.56 mW [2]	1.1 ~ 1.4 mW

[1] Without stimulation current.
[2] Excluding charge pump.

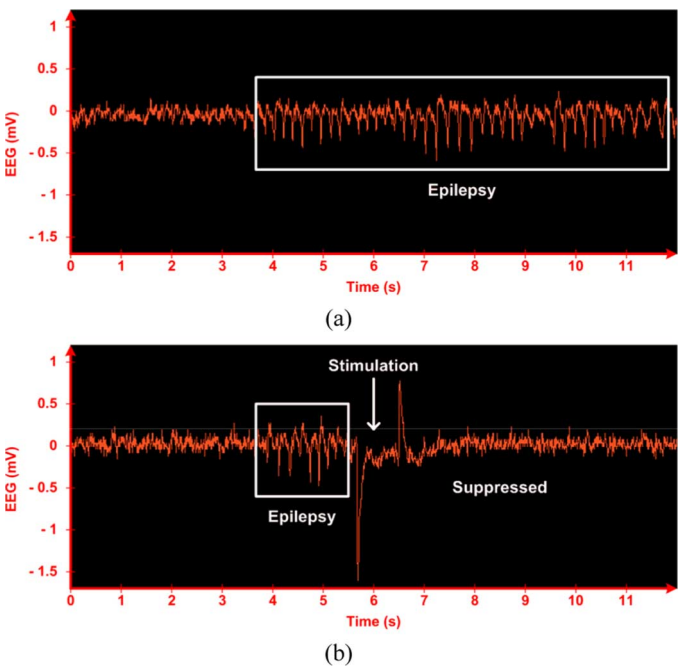


Fig. 14. Experimental results on EEG signals of Long-Evans rat (a) without stimulation, and (b) with stimulation.

epileptic seizure of Long-Evans rat. The injected charge density is $\sim 1000\ \mu\mathrm{C/cm^2}$. The other microwire with wider diameter can also be used to decrease the charge density, since the proposed stimulator has considered the loading impedance adaptability.

One Long-Evans rat with spontaneous absence epileptic discharges is demonstrated in Fig. 14. The electroencephalography (EEG) signals of long-Evans rat without and with applying the stimulation are shown in Fig. 14(a) and (b), respectively. Each experiment is conducted for 10 minutes. In Fig. 14(a), the epileptic discharges are observed during 3.5–12 s. When the seizure controller is applied in Fig. 14(b), the seizure is detected during 3.5–5.5 s. Upon the detection of the seizure, the intensive and rapidly brain activities are suppressed by the stimulation at ~ 6 s. At this measurement, the loading impedance of stimulator is $\sim 150\ \mathrm{k\Omega}$.

According to the experiment results, the functionalities of the proposed stimulator in the closed-loop epileptic seizure monitoring and controlling system have been successfully verified.

VI. CONCLUSION

Design of bi-phasic stimulator for epileptic seizure suppression with loading impedance adaptability is proposed in the 0.35-μm 3.3-V/24-V CMOS process. The stimulator consists of the high voltage generator, output driver, adaptor, and switches. With adaptive loading consideration, the adaptor is used to detect the loading impedance, and the high voltage generator is able to adjust the suitable level of operating voltage. While the loading impedance varies from 10 kΩ to 300 kΩ, the proposed stimulator can constantly deliver 40-μA stimulus current. The power consumption of this work is only 1.1 mW–1.4 mW. The stimulator is successfully integrated into the closed-loop epileptic seizure monitoring and controlling system for animal tests to verify its performances.

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