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Simultaneous Activation and Crystallization by Low-Temperature Microwave Annealing for Improved Quality of Amorphous Silicon Thin-Film Transistors

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In this study, activation and crystallization in short channel amorphous Si TFTs were demonstrated using a novel microwave annealing (MWA) technique. Both low-temperature MWA and rapid thermal annealing (RTA) were compared to study the dopant activation level. We successfully activated the source/drain region, improved the electronic mobility and suppressed the short-channel effects using low temperature MWA. This can reduce the annealing temperature and processing time below that of solid phase crystallization (SPC). This technique is promising for realizing a high utility rate of AM-LCDs with low cost.
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The commercial success of active-matrix liquid-crystal displays (AM-LCDs) has attracted much research into the performance improvement of thin-film transistors (TFTs), which function as the pixel switches in AM-LCDs. Various materials have been investigated as candidates for high mobility channels, such as organic semiconductors,[1] amorphous silicon (α-Si),[2] and semi-conducing oxide.[3] Among these candidates, amorphous silicon has attracted much attention because of its wide range of applicability in large area electronics, lower cost and ease of fabrication.[4] Along with finding new materials, it is necessary to develop a low temperature fabrication process capable of producing high performance TFTs (e.g., high carrier mobility and low resistances at source and drain) using glass as a substrate. SPC of α-Si is a method for manufacturing poly-Si films with low cost and excellent uniformity.[5] Although some heat-proof glass could accept annealing temperature over 600°C,[6] it is generally considered to be harsh condition to use glass as the substrate material. In addition, laser annealing, rapid thermal annealing (RTA), and metal-induced crystallization have been also used as annealing techniques for recrystallization and dopant activation in the amorphous or implanted Si layer. While RTA achieves the best results for short durations of processing, the lamp photons are not only heating the Si layer but also stimulate unintended defect formations which cause dopant diffusion.[7] Metal-induced crystallization in the short channels leads to unwanted contaminations of the active regions.[8] Furthermore, MWA were demonstrated to process annealing with lower crystallization temperatures and short dwell times than the SPC process.[9,10] Therefore, the devices with MWA can reduce the impacts of punch-through, DIBL to obtain nano-scaled transistors with good short channel control.[11] In addition, this technique appears to be a promising replacement for RTA for the semiconductor industry. In this study, TFTs on the amorphous-Si films were fabricated using MWA. The MWA process can reduce the crystallization temperature of amorphous Si, lowering the thermal budget of the entire process while enhancing substrate applications. In addition, the shrinkage of the device size may enhance the aperture rate.

Experimental

A 6-in. (100) bulk silicon wafer was used as the starting material. After a 500 nm-thick silicon dioxide (SiO_2) layer was thermally grown as a buried oxide, a 50-nm-thick undoped amorphous Si film was then deposited using low-pressure chemical vapor deposition (LPCVD) as a active layer with 350 mTorr pressure and at 550°C. The active region was defined by electron-beam lithography. Then, a 50-nm-thick tetraethoxysilane (TEOS) oxide layer was deposited by plasma enhance chemical vapor deposition (PECVD) at 350°C as a gate dielectric, and was followed by the deposition of a 100-nm-thick TiN layer by physical vapor deposition (PVD). After gate definition by anisotropic etching, the self-aligned source and drain were implanted with ^{31}P (15 keV at 1×10^{15} cm^{-2}) for n-MOS TFTs and followed by different dopant activation techniques. MWA was carried out using a 5.8-GHz microwave for 30 minutes, where the maximum temperature of the process wafer reaches about 530°C. The duration of MWA process was defined at the moment when the microwave was turned on. In addition, the split of RTA at 900°C for 30 s was also demonstrated as the control split.

Results and Discussion

The transfer characteristic (I_D-V_G) of polycrystalline Si TFTs at various drain voltages, V_D, is shown in Fig. 1. The channel width and channel length were 10 and 270 nm, respectively. The drain voltages were 0.5 and 2 V, respectively. The drain induced barrier lowering, DIBL, is 4.09 V and 4.25 V by MWA and RTA. The threshold voltage, V_{TH}, is defined as the gate voltage at which the drain current reaches 40 nA × W/L under $V_D = 0.5$ V. V_{TH} was calculated to be about 21 V by MWA and 19.2 V by RTA.

In addition, transconductance (G_m) of the TFTs by MWA is higher than that by RTA. For W/L = 10 μm / 270 nm, the field effect mobility (μ_{EF}) was calculated to be 3.34 cm^2/V-s by MWA and 1.51 cm^2/V-s by

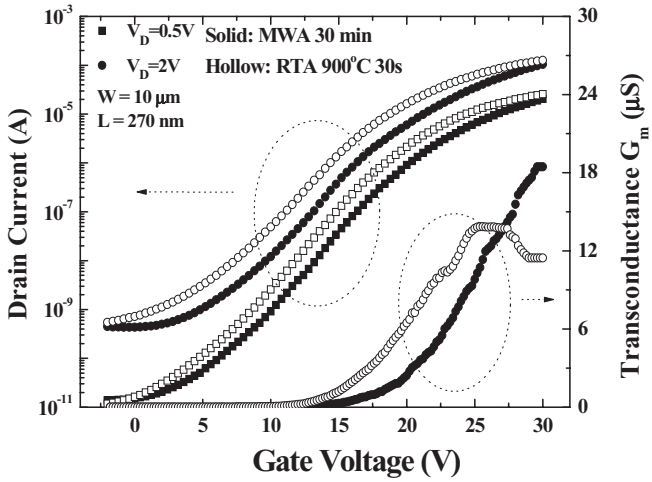

Fig. 1. Transfer characteristics (I_D-V_G and G_m) of n-MOS TFTs annealed by RTA and MWA at $V_D = 0.5$ and 2 V, respectively. W/L = 10 μm / 270 nm.

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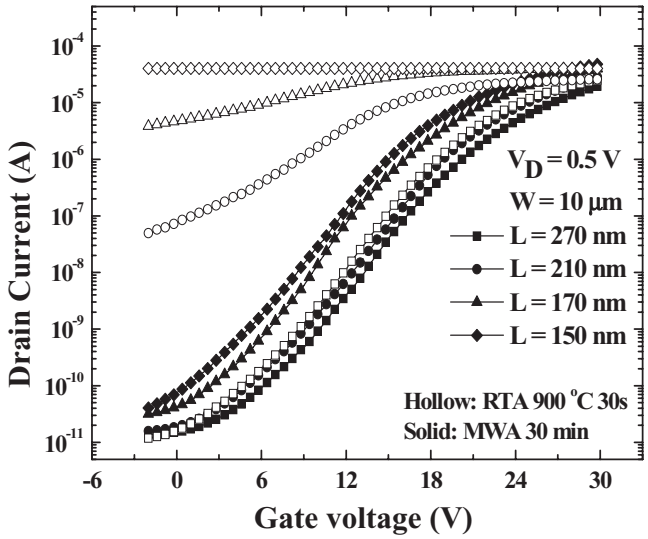

Fig. 2. The transfer characteristics (I_D-V_G) of n-MOS TFTs with different gate length (W = 10 μm) annealed by RTA and MWA. By RTA, since the gate length is below 210 nm, punch-through would dominate the electrical characteristics. By MWA, short channel effects can be suppressed, even when the gate length L is scaled down to 150 nm.

RTA 900°C 30s. The field effect mobility μ_{FE} is extracted from the maximum transconductance. Therefore, the electrical characteristics of amorphous TFTs could be improved by MWA.

Figure 2 shows the electronic characteristics of n-MOS TFTs with different gate lengths annealed by RTA at 900°C for 30 s and by MWA for 30 min, individually. In Fig. 3a, the hollow points were plotted according to the annealing results by RTA at 900°C for 30 s and the I_{on}/I_{off} ratio is approximately 10^6 (I_{on} @ V_G = 27 V, I_{off} @ V_G = 0 V) with L_G = 270 nm. with short gate length less than 170 nm, the off current and the punch-through behavior were shown to be increased, for which the I_{on}/I_{off} ratio is approximately 10^1 for L = 170 nm. Therefore, with a 50-nm-thick gate oxide, it is difficult to fabricate short channel TFTs using the high-temperature RTA process. However, in MWA processes, the punch-through effect can be suppressed due to the low-temperature annealing. In addition, the

Table 1. Summary of the comparisons of important parameters of TFTs from this and other studies.[12–15]

W/L	This work 10 μm/ 0.27 μm	12 40 μm/ 20 μm	13 50 μm/ 10 μm	14 30 μm/ 6 μm	15 200 μm/ 50 μm
V_D (V)	1	10	0.1	20	10
V_{TH} (V)	16.5	10	0.1	20	10
μ_{FE} (cm^2/V-s)	3.11	0.23	0.35	0.6	1.2
I_{off} (pA)	31	1	1	10	2
Ion (μA)	33	0.01	0.1	10	2
I_{on}/I_{off}	1×10^6	1×10^4	1×10^5	1×10^6	1×10^6

I_{on}/I_{off} ratios are approximately 10^8 (I_{on} @ V_G = 27 V, I_{off} @ V_G = 0 V) for the n-MOS TFTs fabricated using MWA with Width/Length = 10 μm/150 nm. It appears that the low-temperature MWA process can suppress the short channel effects, even when the gate width (W) reaches 10 μm.

Figure 3a shows the XRD intensity versus the amorphous silicon films after different annealing methods. The intensity and crystal orientations of the poly-Si from XRD were almost identical. In addition, the MWA can induce larger poly grain sizes (~36 nm) than RTA (~31 nm), which is thought to be the reason for the higher field effect mobility by MWA. The insert in Fig. 3b shows the cross-sectional transmission electron microscopy (TEM) micrograph of the α-Si TFT structure. Finally, Table 1 concludes a summary of the comparisons of important parameters of TFTs from this study and other References 11–14. It shows the superior performance of MWA for gate length shrinkage, field-effect mobility and I_{on}/I_{off} ratio improvements.

Conclusions

Extra microwave activation technique can improve the electronic mobility and suppress punch-through characteristics and short-channel effects, as demonstrated for short channel polycrystalline Si nMOS TFTs. In addition, crystallization by MWA was shown to have larger grain size than crystallization by RTA, enhancing the field effect mobility. Finally, this technique is promising for realizing the high utility rate for short channel TFTs required for applications of AM-LCDs.

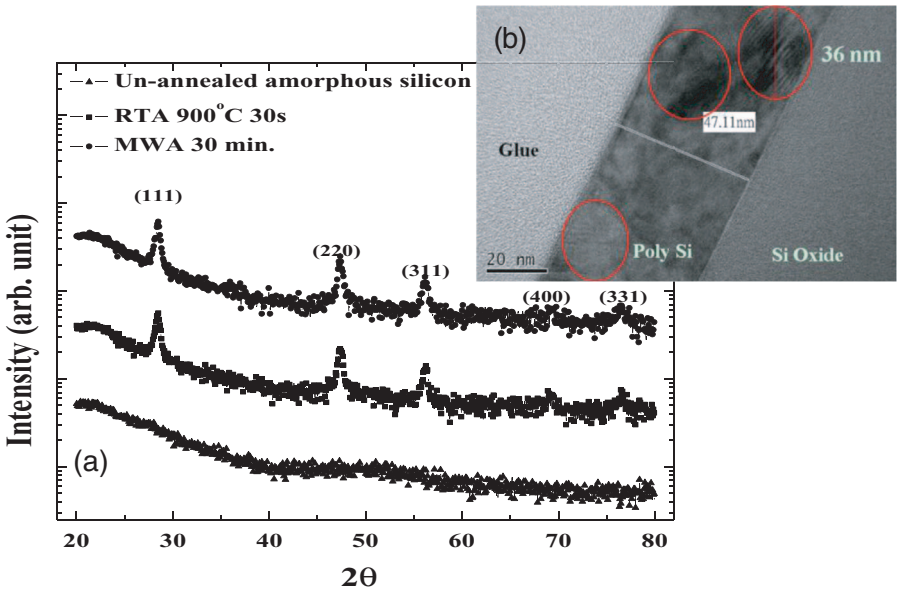

Fig. 3. (a) shows the XRD spectra for different annealing conditions and (b) the cross-sectional transmission electron microscopy (TEM) micrograph is the channel of amorphous Si TFT crystallized by MWA, and the red circle was 36 nm of poly grain.

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