Impacts of Nanocrystal Location on the Operation of Trap-Layer-Engineered Poly-Si Nanowired Gate-All-Around SONOS Memory Devices

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***Abstract*—Trap-layer-engineered poly-Si nanowire silicon–oxide–nitride–oxide–silicon (SONOS) devices with a gate-all-around (GAA) configuration were fabricated and characterized. For the first time, a clever method has been developed to flexibly incorporate Si-nanocrystal (NC) dots in different locations in the nitride layer. Three types of poly-Si GAA SONOS devices with Si-NC dots embedded in the block oxide/nitride interface, the middle of the nitride, and the nitride/tunnel oxide interface, respectively, by *in situ* deposition were fabricated and investigated in this paper. Our results indicate that the optimal NC location appears to be somewhere between the middle and bottom interfaces of the nitride layer.**

***Index Terms*—Gate-all-around (GAA), nanocrystal (NC), nanowire (NW), poly-Si, silicon–oxide–nitride–oxide–silicon (SONOS).**

I. Introduction

In THE PAST several decades, the floating-gate (FG)-type cell structure has dominated the mainstream nonvolatile-semiconductor-memory market [1]. However, issues such as the strong FG coupling effect between neighboring cells [2] and stress-induced leakage current (SILC) [3] in the tunneling oxide have hindered the future scaling of the FG-type technology. In line of this, the charge-trapping-type cell structure, specifically silicon–oxide–nitride–oxide–silicon (SONOS), has received renewed keen interest for replacing FG Flash cells owing to its excellent immunity to SILC and FG coupling effects. Unlike FG Flash cells, the charges are stored in discrete traps located in the nitride of the SONOS cell [4]; therefore, the tunneling oxide can be further scaled down to allow the lowering of operation voltage and/or improving program/erase (P/E) speed.

Recently, poly-Si-based SONOS device has attracted much attention because of its full process compatibility with 3-D integration [5], [6]. Various approaches have been proposed for improving SONOS device performance such as enhancing gate controllability using multigated schemes such as gate-all-around (GAA) [7], replacing a block oxide layer with a high-k dielectric [8], or adopting a trap-layer-engineering (TLE) scheme [9]–[11]. The concept of TLE was originally proposed by incorporating the tungsten nitride nanodots in the nitride layer. The incorporation of silicon nanocrystal (NC) dots at the top block oxide/nitride interface [10] or in the middle of the nitride [11] has also been proposed and investigated. However, a comprehensive study on the effects of NC-dot locations in a trapping layer on device characteristics is still lacking. In this paper, we have fabricated and investigated several types of poly-Si GAA SONOS devices with Si-NC dots embedded in various locations in the nitride layer by *in situ* deposition. Particular attention was paid on the effects of the Si-NC-dot location on device operation characteristics.

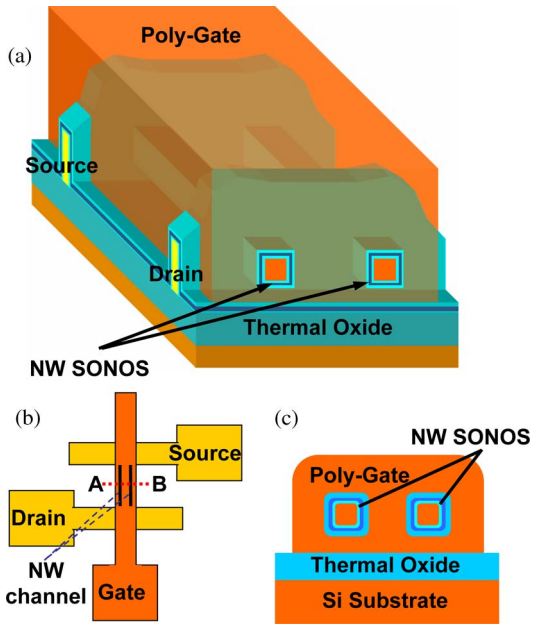

Fig. 1. (a)Schematic structure of the proposed device. (b) Layout of the device. (c) Cross-sectional view of the NW SONOS along line AB in (b).

II. Device Structures and Fabrication

Figs. 1(a)–(c) shows the stereo, top, and cross-sectional views, respectively, of the proposed GAA nanowired (NW) device structure. Basically, the fabrication process is similar

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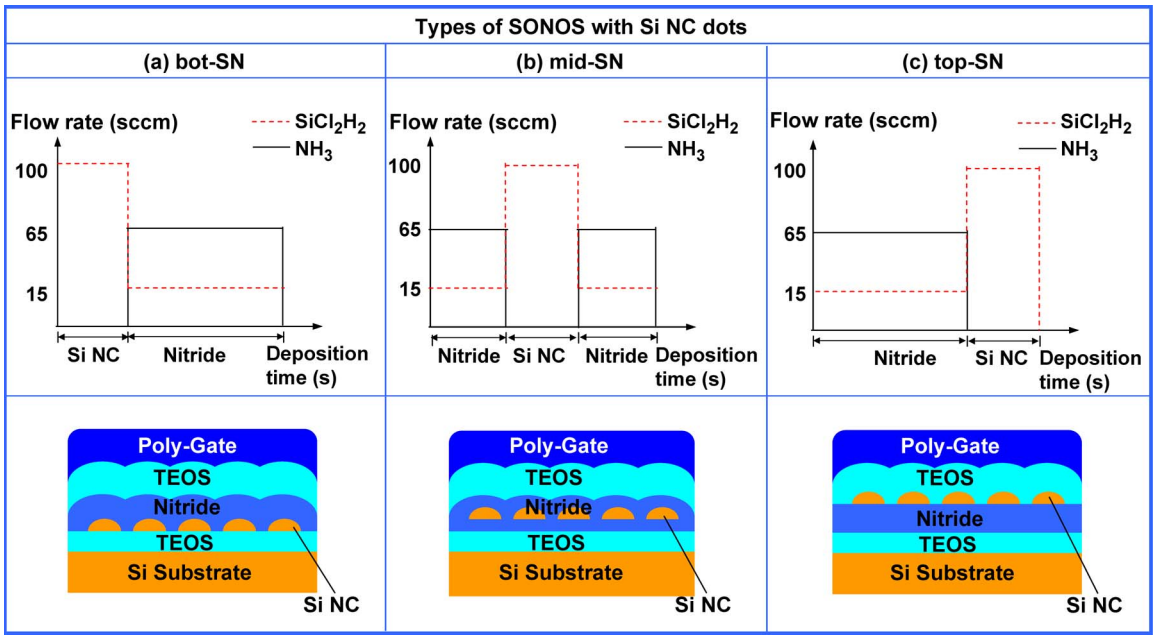

Fig. 2. Flow rate and schematic diagram of three types of devices incorporated with Si-NC dots. Bot-SN: Si-NC dots are located at the interface of the tunneling oxide and the nitride. Mid-SN: Si-NC dots are embedded in the nitride. Top-SN: Si-NCs are located at the interface of the nitride and the block oxide.

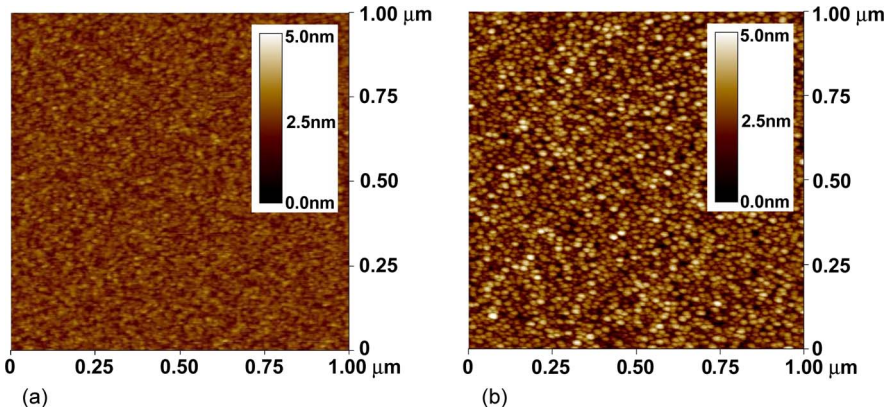

Fig. 3. $1 \times 1\ \mu m^2$ AFM image of nitride films (a) without and (b) with Si-NC dots formed on the surface. The surface roughness (root-mean-square value) is 0.338 nm in (a) and 0.791 nm in (b). The sample in (b) has been treated with a DCS exposure time of 45 s, and the density of Si-NC dots is $2.4 \times 10^{11}\ cm^{-2}$.

to that described in one of our previous papers [12], except for the implementation of the TLE scheme by incorporating the Si-NC dots in the nitride layer. Briefly, after forming the silicon NWs, a 3.5-nm tunneling oxide was first deposited, which was followed by nitride deposition with low-pressure chemical vapor deposition (LPCVD). By cleverly adjusting the flow rates of $SiCl_2H_2$ [using a distribution control system (DCS)] and NH_3 during the LPCVD–nitride deposition step [see Figs. 2(a)–(c)], the Si-NC dots can be *in situ* incorporated into various locations in the nitride layer in a flexible and controllable manner. As shown in Figs. 2(a)–(c), wafers were split into three groups, which were denoted as bot-SN, mid-SN, and top-SN, respectively, according to the position of the Si-NC dots in the nitride. For illustration, we take the mid-SN split shown in Fig. 2(b) as an example. The TLE process consists of three consecutive steps in the LPCVD furnace to form a bottom nitride, Si-NC dots, and a top nitride, consecutively. In the first step, a 4-nm-thick bottom nitride film is deposited with DCS (15 sccm) and NH_3 (65 sccm) gases at 780 °C. Subsequently, by turning off the NH_3 gas flow and increasing the flow rate of the DCS to 100 sccm, Si-NC dots are *in situ* formed on the surface of the deposited nitride. The duration of this period is 45 s. Then, a 4-nm top nitride is capped on the Si-NC dots. Similarly, the gas flow charts for the TLE of bot-SN and top-SN are illustrated in Fig. 2(a) and (c), respectively. After the TLE process, all wafers were combined to receive 12-nm-thick tetraethyl orthosilicate (TEOS) oxide deposition as the block oxide. An *in situ* doped poly Si of about 150 nm was then deposited and patterned to serve as the gate electrode. For comparison, standard (STD) GAA-NW-SONOS devices with ONO of 3.5/8/12 nm were also fabricated and characterized.

The atomic-force microscopic (AFM) image of nitride samples with and without Si-NC dots formed on the surface are shown in Fig. 3(a) and (b), respectively. In contrast to the smooth bare nitride sample, the abundance of protuberant Si-NC dots with an estimated density of $2.4 \times 10^{11}\ cm^{-2}$ is clearly visible in Fig. 3(b). Note that, for the same process condition forming the NC dots on a TEOS oxide surface, the

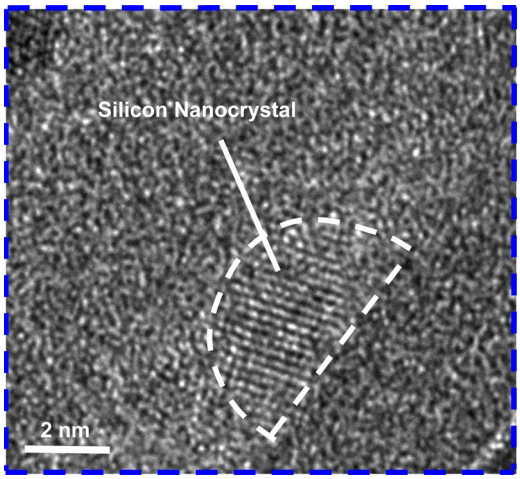

Fig. 4. Cross-sectional TEM picture of a Si-NC dot embedded in the nitride.

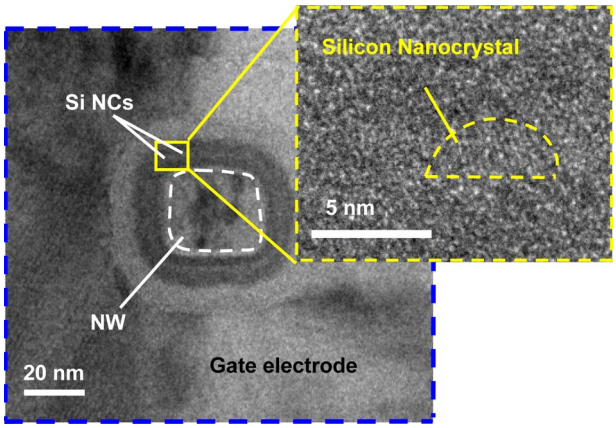

Fig. 5. Cross-sectional TEM picture of a mid-SN device. Inset shows the enlarged view of an embedded Si-NC dot in the nitride.

density is around 2.6×10^{11} cm^{-2} (data not shown), which is close to the result shown in Fig. 3(b). Fig. 4 depicts a high-resolution transmission-electron-microscopic (TEM) image of a test sample showing a hemispherical Si-NC dot formed on the nitride with the aforementioned approach. Fig. 5 exhibits the cross-sectional TEM image of a mid-SN device. It can be seen that the silicon NW is rectangular in shape with rounded corners and the width is about 30 nm. The inset shows an enlarged view of the TLE nitride layer in which a hemispherical Si-NC dot is contained.

III. Basic Electrical Characteristics of Poly-Si NW SONOS Devices

Fig. 6 shows the I_D–V_G curves of the STD and Si-NC NW SONOS devices with $L = 0.4$ μm. It can be seen that the subthreshold swing (SS) of the STD device is slightly lower than those of the Si-NC splits. The discrepancy of the SS can be explained by the following two reasons. First, the embedded Si-NC dots increase the effective oxide thickness (EOT). This is confirmed from the measurements performed on the planar capacitors where the EOT is found to be 18.2 nm for the STD split and 19.1–19.7 nm for the samples incorporated with NCs. Second, after depositing the Si NC, the surface is roughened. As

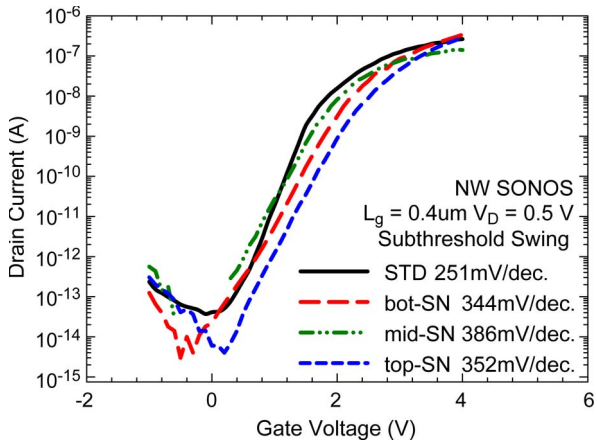

Fig. 6. Transfer characteristics of STD, bot-SN, mid-SN, and top-SN devices, all with a channel length of 0.4 μm and measured at $V_d = 0.1$ V.

indicated by the AFM images shown in Fig. 3(a) and (b), the surface roughness (root-mean-square value) indeed increases from 0.338 nm for the sample without NCs to 0.791 nm on the sample with NCs formed. Consequently, the EOT of the Si-NC devices is not uniform across all gated area, leading to a nonnegligible variation in EOT across the channel region, which may in turn cause a fluctuation of the channel potential, further degrading the SS. Based on the aforementioned two reasons, it is reasonable to explain why the SS of the STD split is better than those of the Si-NC splits.

IV. Programming/Erasing Characteristics

For P/E operation, Fowler–Nordheim injection was employed by applying a positive or a negative voltage to the gate electrode for program or erase operation, respectively, with the source and the drain grounded. For the erase tests, all devices were programmed beforehand with a 2.5-V shift of $V_{\rm th}$ with respect to the fresh state. The program characteristics of the STD device are shown in Fig. 7(a), whereas Fig. 7(b)–(d) depict the program characteristics of the bot-SN, mid-SN, and top-SN devices, respectively. Owing to the thinner EOT, the STD device exhibits the fastest $V_{\rm th}$ increase rate among all splits in the very early stage of programming (e.g., $\ll 10^{-7}$ s). However, when the program time is sufficiently long, both bot-SN [see Fig. 7(b)] and mid-SN [see Fig. 7(c)] devices show faster rates over the STD control. For the STD device, it has been pointed out previously that, during programming, the centroid of the trapped electrons in the nitride layer tends to migrate from the bottom interface toward the middle of the nitride layer [9]. Nevertheless, Si-NC dots in the bot-SN and mid-SN devices provide additional trapping sites in the bottom nitride interface and the nitride center, respectively; therefore, more electrons can be trapped in positions closer to the channel than the STD control during programming. As a result, a larger $V_{\rm th}$ shift rate and a larger $V_{\rm th}$ value are resulted in Fig. 7(b) and (c). Furthermore, the available trapping sites also increase due to the incorporation of the Si-NC dots as evidenced by the larger $V_{\rm th}$ window with prolonged stressing time for both the bot-SN and mid-SN devices.

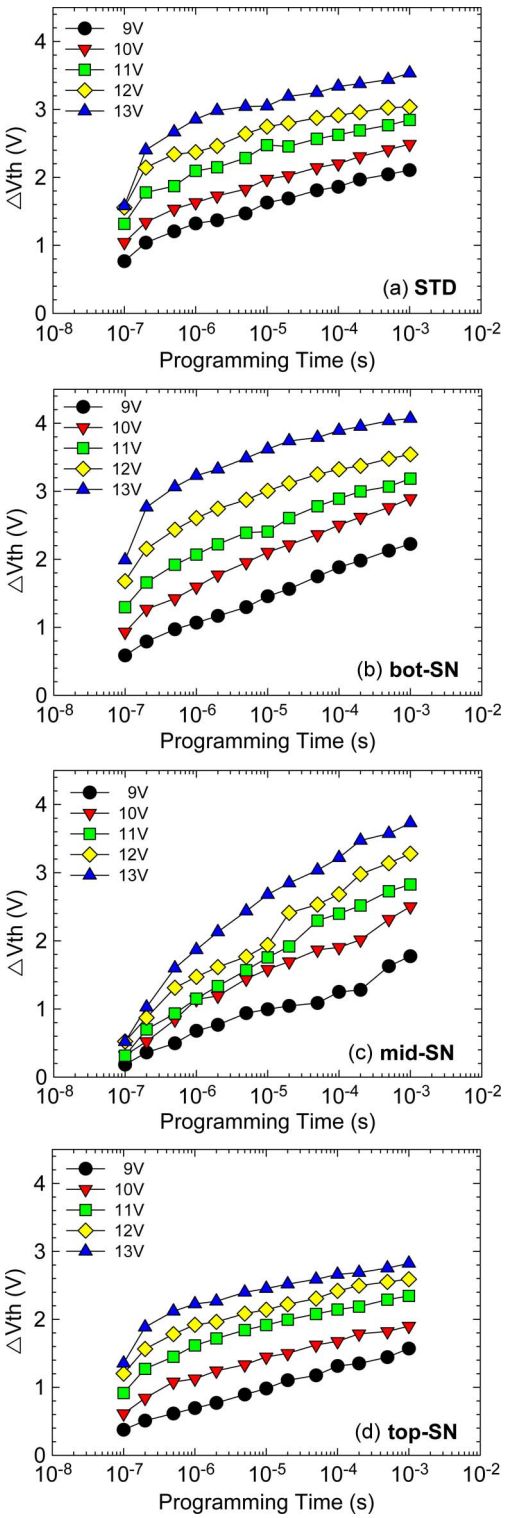

Fig. 7. Program characteristics of (a) STD, (b) bot-SN, (c) mid-SN, and (d) top-SN devices, all with a channel length of 0.4 μm and a gate bias that varies from 9 to 13 V.

For the top-SN device, as shown in Fig. 7(d), the $V_{\rm th}$ shift rate is similar to that of the STD device. The buildup of negative charges in the middle of the nitride during programming may hinder further injection of electrons from the channel; therefore, most of the top Si-NC dots would remain vacant and neutral. Owing to the thicker EOT of the top-SN device, the program window is smaller than that of the STD device. Fig. 8 shows the transfer curves of all splits before and after programming operation ($V_g = +13$ V and $t = 10^{-3}$ s). It can be seen that the bot-SN device exhibits the largest window among all splits.

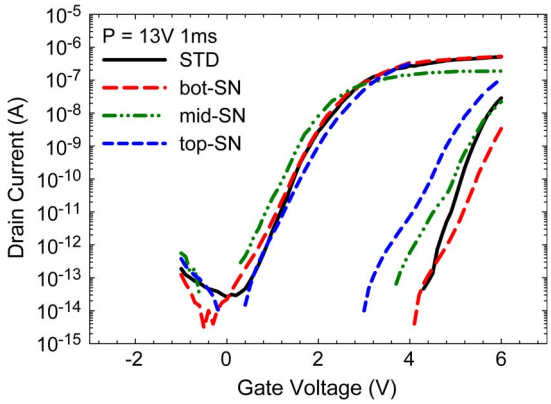

Fig. 8. Transfer characteristics of all splits of devices before and after programming with V_g of 13 V and a stress time of 1 ms.

Fig. 9(a)–(d) shows the erase characteristics of the STD, bot-SN, mid-SN, and top-SN devices, respectively. Compared with the STD device, the bot-SN one shows a faster rate and a mitigated saturation behavior [see Fig. 9(b)]. This is attributed to the fact that more trapped electrons are located closer to the channel. For the mid-SN device [see Fig. 9(c)], the $V_{\rm th}$ shift rate is initially slow and only weakly dependent on the gate bias (see Stage I in the figure) but becomes much faster at a certain moment, which is closely related to the magnitude of gate bias (i.e., Stage II). Such a transition can be understood with the qualitative band diagrams shown in Fig. 10 and Fig. 11(a) and (b). Fig. 10 shows the situation of a programmed mid-SN device. The Si-NC dots incorporated in the middle of the nitride form quantum wells, which provide trapping sites with an energy level lower than the portion of the trapping sites located inside the nitride. After programming, most of the electrons are believed to be trapped inside the deep levels in the Si-NC dots or the defect sites located in the middle of the nitride, resulting in the rise of potential wherein, as shown in Fig. 10. In Stage I [see Fig. 11(a)] of erase operation, the electrons trapped inside the Si-NC dots can either tunnel back to the channel directly, which would lower $V_{\rm th}$, or transfer to vacant levels in the nitride, which tend to increase $V_{\rm th}$. Since the two processes have an opposite effect on the $V_{\rm th}$ shift and tend to cancel out each other, the overall shift rate is limited. In addition, as the gate bias is varied, the major change in voltage drop occurs in the block oxide due to the accumulation of a large amount of trapped electrons; therefore, the $V_{\rm th}$ shift rate is not strongly dependent on the gate bias [see Fig. 9(c)]. While in Stage II, most of the electrons trapped in the Si-NC dots have vacated; therefore, the ejection of electrons to the channel from the trapping sites located in the nitride becomes dominant, as shown in Fig. 11(b), resulting in an accelerated rate in the $V_{\rm th}$ shift shown in Fig. 9(c).

For the top-SN device [see Fig. 9(d)], it exhibits rates comparable to those of the STD one, but $V_{\rm th}$ begins to shift upwards as the erase time is sufficiently long. This upward trend is explained by the qualitative band diagrams shown in Fig. 12(a)

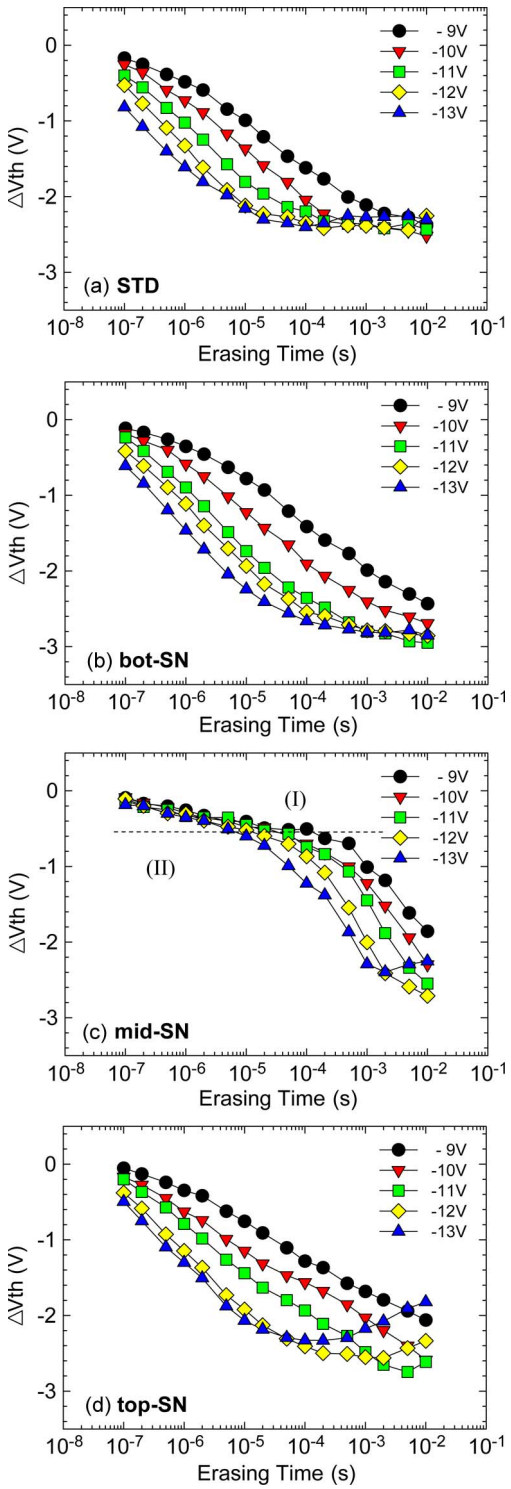

Fig. 9. Erase characteristics of (a) STD, (b) bot-SN, (c) mid-SN, and (d) top-SN devices, all with a channel length of 0.4 μm and a gate bias that varies from -9 to -13 V.

and (b) for the top-SN devices during erase operation. Fig. 12(a) corresponds to the early stage of operation during which the trapped electrons are released to the channel, resulting in $V_{\rm th}$ lowering. Later, as shown in Fig. 12(b), as most of the trapped electrons stored in the nitride have vacated, the field strength in the block oxide will increase, causing electron injection from the gate. The injected electrons then get trapped in the Si-NC dots and cause a $V_{\rm th}$ increase.

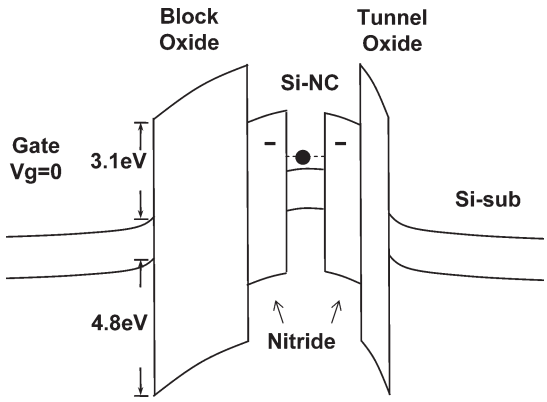

Fig. 10. Band diagrams of the programmed mid-SN device.

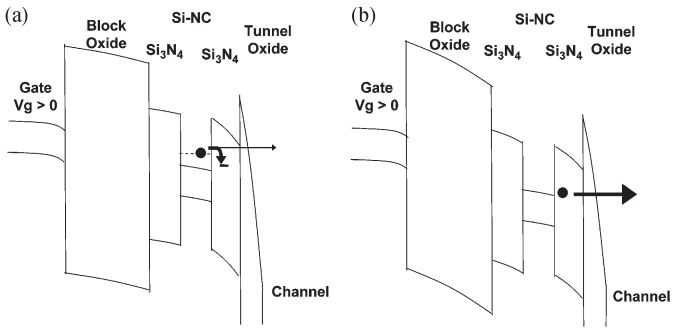

Fig. 11. Band diagrams of the mid-SN device during erasing at (a) Stages I and (b) II. At Stage 1, the electrons trapped inside the Si-NC dots can either tunnel back to the channel directly or transfer to a vacant level in the nitride.

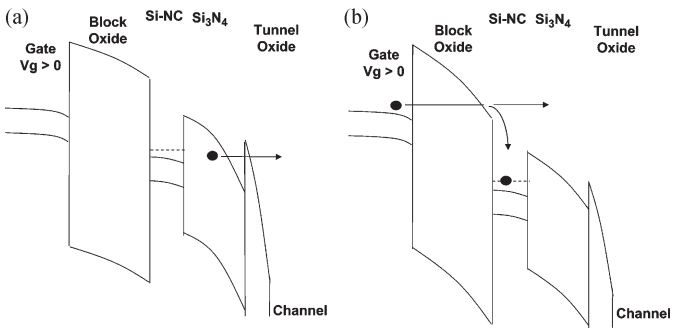

Fig. 12. Band diagrams of a top-SN device during erasing. (a) Electrons are detrapped from the nitride layer. (b) Electrons injected from the gate as most of the electrons stored in the nitride have vacated. Some injected electrons are trapped in the Si-NC dots.

V. Endurance and Retention Characteristics

For the reliability tests, different P/E conditions were applied to different splits in order to obtain the same memory window of about 2 V for all splits. Fig. 13 shows the retention characteristics of all splits measured at 25°C and 85 °C. It can be seen that the mid-SN split shows the best retention performance among all splits. This is believed to be due to the deeper storage levels for electrons introduced by Si-NC dots embedded in the nitride. In contrast, the bot-SN device exhibits a retention behavior similar to that of the STD control. This is because the trapped electrons tend to leak out because, compared with other splits, they are located closer to the channel, although the incorporated Si-NC dots do provide deeper levels for storing the electrons. Finally, the endurance characteristics for all splits are

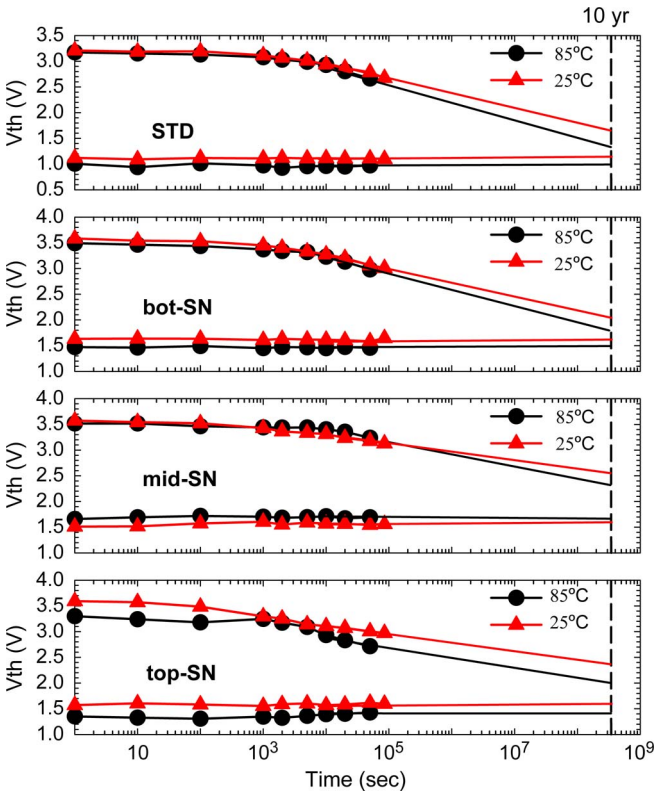

Fig. 13. Data retention characteristics of the STD device and various Si-NC devices. The memory window is initially set at about 2 V for all devices.

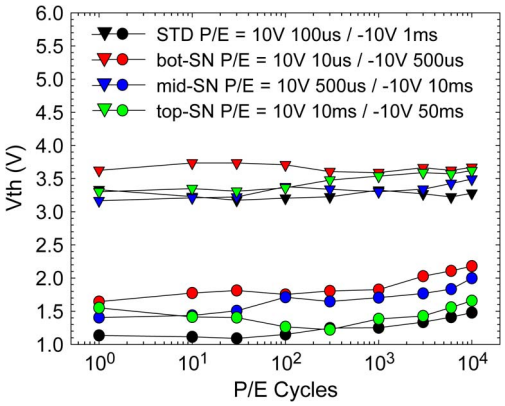

Fig. 14. Endurance characteristics of the STD device and various Si-NC devices.

TABLE I
COMPARISON BETWEEN THE STD AND Si-NC DEVICES

★ Excellent ○ Good △ Fair.

	STD	bot-SN	mid-SN	top-SN
Program Rate (>10^{-7}s)	○	★	△	△
Erase Rate	○	★	△	△
Erase Saturation	○	★	○	△
Window Size	△	★	○	△
Retention	△	△	★	○
Endurance	○	○	○	○

shown in Fig. 14. It can be seen that no significant differences are observed among the devices. A comparison of the operation performance of all splits is summarized in Table I.

VI. CONCLUSION

In this paper, three types of poly-Si GAA-NW-SONOS devices with Si-NC dots embedded in the block oxide/nitride interface, middle of the nitride, and tunnel oxide/nitride interface, respectively, have been successfully fabricated and carefully characterized to gain insights into the effects of NC-dot locations on the device memory characteristics. We found that the memory devices exhibit drastic different P/E characteristics in accord with their Si-NC-dot locations. During programming, the mean location of trapped electrons would be affected by Si-NC dots, thus inducing a faster $V_{\rm th}$ increase rate in the bot-SN split. Moreover, these Si-NC dots provide extra trapping sites that enable a larger memory window in both bot-SN and mid-SN splits. While for the mid-SN devices, we found that these Si-NC dots render the trapped electrons harder to detrap. With prolonged erasing time, the gate-injected electrons are trapped in the Si-NC dots, resulting in a $V_{\rm th}$ increase as is observed in the top-SN devices. To summarize, the bot-SN split shows the best P/E characteristics, whereas the mid-SN split shows the best retention characteristics. Based on these findings, we conclude that the most optimal NC-dot location should be somewhere between the middle and the bottom interface of the nitride layer.

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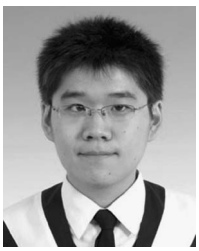

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