Semiself-Protection Scheme for Gigahertz High-Frequency Output ESD Protection

Jian-Hsing Lee, Shao-Chang Huang, Hung-Der Su, and Ke-Horng Chen

***Abstract*—In this paper, a semiself-protection scheme is proposed and developed for gigahertz output electrostatic-discharge (ESD) protection. The output transistor acts as a trigger device to trigger the ESD protection device, and then, it is turned off when the ESD protection device turns on. Thus, the capacitance of a gigahertz high-frequency output pad can be minimized because this scheme is without any additional trigger device or any passive component.**

***Index Terms*—Electrostatic discharge (ESD), radio frequency, silicon-controlled rectifier (SCR).**

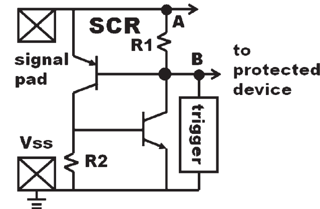

Fig. 1. SCR has the triggering device behind a resistor. The protected device needs to connect to node B and not to Node A.

I. INTRODUCTION

THE electrostatic-discharge (ESD) performance of a silicon-controlled rectifier (SCR) is much superior than that of a grounded-gate (GG) n-channel metal–oxide–semiconductor field-effect transistor (n-MOSFET) because of its high-current and low-voltage characteristics. Designed with a much smaller dimension, SCRs can obtain the same or better ESD performance compared with a GGNMOS. SCRs have become a good ESD protection device for radio-frequency or high-frequency (HF) circuit designs.

Although an SCR has robust ESD performance, it cannot prevent an ESD from damaging protected devices appropriately due to its high trigger voltage V_{t1} [1]. The protected device could be damaged before the SCR turns on. Thus, many kinds of triggering devices are designed to reduce the V_{t1} of an SCR. The triggering devices include n-MOSFETs [1]–[4], p-n-p bipolar transistors [5], p-channel MOSFETs [6], and diode-string structures [7]. The triggering device often needs to be incorporated with a resistor (R1 in Fig. 1) to prevent the high ESD current from damaging integrated circuits (ICs). The resistor might be the well-shunt resistor (R1 in Fig. 1) of an SCR [1], a discrete resistor [2], or the silicide-blocking resistor of a triggering device [3], [4]. Apparently, a resistor will induce a voltage across the resistor when the current flows through the triggering device. This increases the device's V_{t1}; thus, an SCR cannot prevent an ESD from damaging protected devices if the protected devices are in parallel with the SCR (node A in Fig. 1) [8]. Regardless of the input gate [1] or the output drain terminal [2], the protected devices had better connection to the node after the resistor (node B in Fig. 1) instead of the node before the resistor (node A in Fig. 1). However, a resistor can induce noise, reflection, a secondary harmonic, and power gain loss at HF applications. Thus, putting a transceiver and a receiver behind a resistor is not allowed for most HF designs.

It has been reported that the structures of a GGSCR [3] and a p-n-p triggering SCR [5]) allow a signal pad to connect to a protected device without passing through a resistor. However, both structures cannot be used for driving circuits. It is because the triggering device of the GGSCR [3] has a ballast resistor on the drain terminal and a series resistor on the source terminal. Although the triggering devices of the modified p-n-p triggering SCRs [5], [6] are revised to MOSFETs, they are all located behind the SCR's well-shunt resistors. Furthermore, diode-triggering SCR structures have been discussed in [9] and [10]. Silicon-on-insulator SCRs, 3-D technology computer-aided design, and an insulated-gate bipolar transistor plugged in an SCR are described in [11]–[13]. However, all the above SCR structures have the disadvantages of bad (or no) output driving capabilities.

If an n-MOSFET designed with the minimum design rules can be placed in parallel with an SCR, it can be used as the output transistor during IC normal operation. The simulation of designing an n-MOSFET in parallel with an SCR is reported in this paper. With the proper layout for the n-MOSFET and the SCR, the n-MOSFET can be turned only on at the initial transient time and can be turned off after the SCR is triggered on. Due to the short turn-on time, Joule heating (power × time) caused by an ESD is too small to damage the output transistor. Since the output transistor can be turned on at a short time and most ESDs are dissipated by the primary ESD protection device SCR, this protection scheme is called the semiself-protection (SSP) scheme.

Manuscript received December 28, 2010; revised March 30, 2011 and April 8, 2011; accepted April 11, 2011. Date of publication May 23, 2011; date of current version June 22, 2011. The review of this paper was arranged by Editor M. J. Kumar.

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Digital Object Identifier 10.1109/TED.2011.2143717

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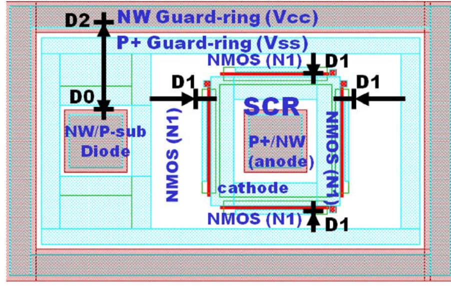

Fig. 2. Layout for the SSP-ESD device.

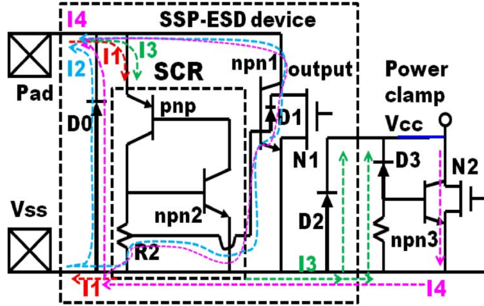

Fig. 3. Equivalent circuit and current paths for SSP-ESD devices under four different zapping modes.

The technology of this paper is a 0.18-μm 1.8/3.3-V silicide complementary MOS (CMOS) process. Although the architectures in this paper are verified by using 1.8-V devices with a gate-oxide thickness equal to 32 Å, it can also be modified as the 3.3-V operation. This paper is processed on a dual-well (p-well and n-well) process and a p-type wafer. Except for n-well regions, they are p-well regions.

II. Device Structure and Analysis

A. SSP ESD Device

Fig. 2 shows the layout of the SSP-ESD device. The SSP-ESD device includes the following:

1) an n-type well (NW) to the p-type substrate diode (D0);
2) an SCR and the output transistor (n-MOSFET) N1 and its parasitic diode (D1);
3) p+ and NW guard rings;
4) The parasitic diode (D2) between the two guard rings.

Diodes D0 and D1 are designed for negative ESD stress. The SCR with the output transistor N1 is designed for positive ESD stress. The NW and p+ guard ring are designed for ICs' latch-up prevention and for PAD-$V_{\rm CC}$ ESD protection under positive ESD stress.

Fig. 3 shows the equivalent circuit and the current paths of the SSP-ESD device with a power clamp (PCL) device under four kinds of ESD zapping modes. The four kinds of ESD zapping modes are: (+) PAD-$V_{\rm SS}$, which is the positive ESD event at the signal pad with respect to $V_{\rm SS}$; (−) PAD-$V_{\rm SS}$, which is the negative ESD event at the signal pad with respect to $V_{\rm SS}$; (+) PAD-$V_{\rm CC}$, which is the positive ESD event at the signal pad with respect to $V_{\rm CC}$; and (−) PAD-$V_{\rm CC}$, which is the negative ESD event at the signal pad with respect to $V_{\rm CC}$. Although the SSP-ESD device is only designed for (+/−) PAD-$V_{\rm SS}$ protections, it can also provide (+/−) PAD-$V_{\rm CC}$ ESD protections as it cooperates with the PCL device. The discharge current paths of the SSP-ESD device with the PCL device under the four kinds of ESD zapping modes can be depicted as follows. For (+) PAD-$V_{\rm SS}$, current I1 flows from the signal pad through the SCR of the SSP-ESD device to $V_{\rm SS}$. For (−) PAD-$V_{\rm SS}$, current I2 flows from $V_{\rm SS}$ through the diodes D0 and D1 of the SSP-ESD device to the signal pad. For (+) PAD-$V_{\rm CC}$, current I3 flows from the signal pad through the SCR of the SSP-ESD device and the combined paths of the diode D2 of the SSP-ESD device and the diode D3 of the PCL device to $V_{\rm CC}$. For (−) PAD-$V_{\rm CC}$, current I4 flows from $V_{\rm CC}$ through the parasitic bipolar n-p-n 3 of the PCL device and the diodes D0 and D1 of the SSP-ESD device to the signal pad. The SCR anode area size is 6 μm × 6 μm.

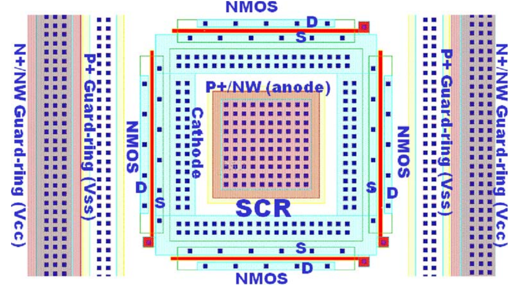

Fig. 4. Detailed layout for the SSP-ESD device in Fig. 3.

B. SCR

Fig. 4 shows the detailed layout for the SCR of the SSP-ESD device. Unlike the NW of the conventional SCR [1]–[13] with the n+ and p+ diffusions, the NW of this SCR only has the p+ diffusion. Without the n+ diffusion in the NW, the p-n-p bipolar transistor is an open base transistor (see Fig. 3). From the testing results, the SCR still can be turned on by an ESD without wasting layout areas for forming a base resistor. Thus, the SCR can be turned on by an ESD more easily and does not need to waste layout areas to form a base resistor. Without wasting the area, the SCR dimension can be minimized. Thus, it can get smaller capacitance compared with the conventional SCR. In addition, the shape of the SCR is designed as a square type for getting the smallest layout perimeter under an assigned layout area. This kind of design can also obtain a smaller sidewall capacitance value. The SCR's cathode is designed as a ring and surrounds the SCR's anode. The output transistor is composed of four 1.8-V n-MOSFETs, which are outside and surround the SCR's cathode.

Except for the space between contacts, the output transistor is designed with the minimum layout rules to minimize its total capacitance. The finger width and the total channel width of the output transistor are equal to 10 and 40 μm, respectively. The source of the output transistor is located close to the cathode of the SCR than the drain of the output transistor. This kind of architecture can make the high ESD current not flow through the output transistor when the SCR turns on since the output transistor is outside the SCR (see Fig. 5). Unlike the conventional n-MOSFET trigger devices of the SCRs [2], [4], [8] with

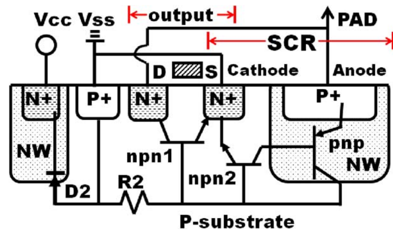

Fig. 5. Cross section and the equivalent circuit for the SSP-ESD device in Fig. 4.

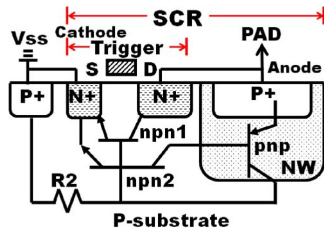

Fig. 6. Equivalent circuit for the MLVTSCR.

the silicide-blocking drain regions, the trigger device (output transistor) of the SSP-ESD device is a fully silicide device. Instead of the silicide-blocking drain regions, the contacts on the source and drain (S/D) regions of the output transistor are designed with the stagger S/D contact type and a large contact-to-contact space [14]. Without the silicide-blocking layer, the drain contact to the poly-gate space and the source contact to the poly-gate space can be designed with the minimum process rules. This scheme can get the smallest capacitance and series resistance for the n-MOSFET trigger device. With low capacitance and resistance, such a trigger device can be used as the output transistor for HF operation.

C. Simulated Current for the SCR

Fig. 6 shows the cross section and the equivalent circuit of the modified low-voltage-triggered SCR (MLVTSCR) [4]. The difference between an LVTSCR [1] and the MLVTSCR is that the drain region of the MLVTSCR does not overlap the NW and connects to the pad directly. The SSP ESD is a new version of the MLVTSCR. For this kind of an SCR, the source of the trigger device shares the same region with the cathode of the SCR. In addition, the drain region of the triggering device is located between the SCR cathode and the SCR anode. Apparently, the triggering device is within the SCR. TSupprem 4 for the process simulation and the device formation and MEDICI for the electrical simulation are adopted in this paper.

From the simulation result in Fig. 7(a), the current flows from the drain region of the triggering device to the source region of the triggering device and the V_{SS} p+ diffusion at the transient before the trigger. This implies that the n-p-n bipolar transistor of the triggering device will be turned on first. Then, the current can also flow from the p+ diffusion in the NW to the V_{SS} p+ diffusion except the n-p-n bipolar current [see Fig. 7(b)]. This implies that the p-n-p bipolar transistor has been triggered to the ON-state at this transient. As the stress current increases, the currents not only flow from the p+ diffusion of the NW but

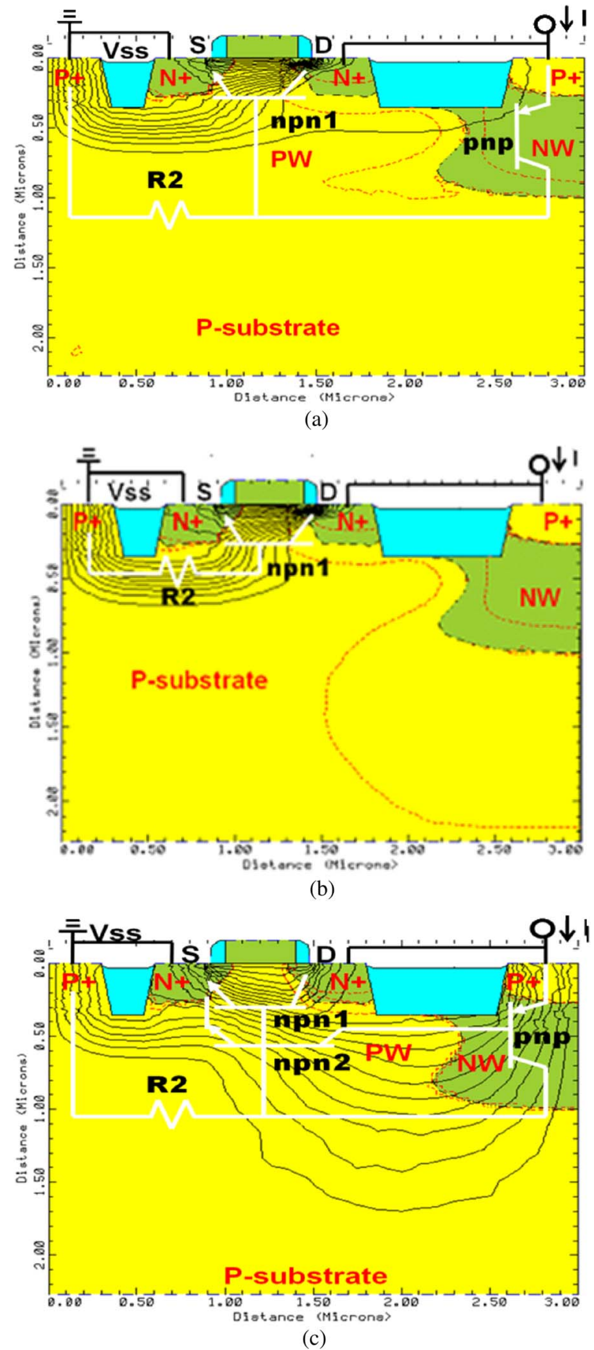

Fig. 7. Simulated current flowing lines of the MLVTSCR transients. (a) Before the trigger. (b) At the trigger. (c) After the trigger.

also flow from the drain region of the triggering device to the source region of the triggering device and the V_{SS} p+ diffusion [see Fig. 7(c)].

Both the SCR and the triggering device are turned on to drive the MLVTSCR into a stable snapback region after the triggering transient because the cathode is closer to the drain region than the anode. If the electrons can flow from the SCR cathode to the SCR anode, they will be able to flow to the drain region of the triggering device. For such an SCR, the ESD current flows through the triggering device even when the SCR has turned on. For preventing output devices from ESD damage, the drain region of the triggering device is often designed with a ballast

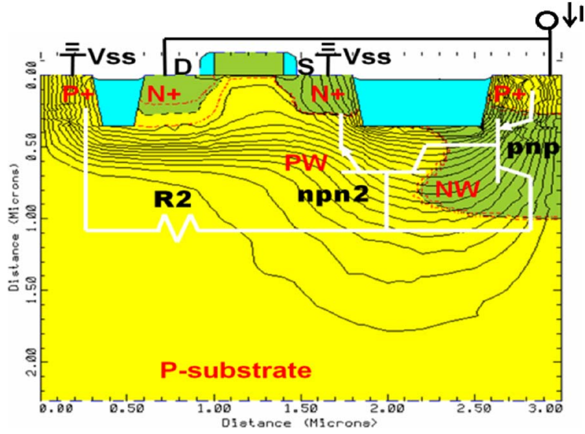

Fig. 8. Simulated current flowing lines for the SSP-ESD device at the transients after the trigger.

resistor. However, adding a ballast resistor is not allowed for the output transistor under the gigahertz application.

If the S/D terminals are exchanged, the triggering device will be located outside the SCR, as shown in Fig. 5. For the transients before and at the trigger, the ESD behaviors of this new architecture are the same as those of the MLVTSCR, but the S/D regions are exchanged. However, for the transient after the trigger, the ESD behavior of the new architecture is apparently different from that of the MLVTSCR, as shown in Fig. 8; it shows that the current can only flow through the SCR and not through the triggering device.

When the SCR is turned on, the triggering device could be turned off and kept far away from the ESD stress. It implies that most ESD charges are dissipated by the SCR, and only few ESD charges flow through the triggering device at the beginning of the ESD pulse. Due to the short turn-on time, there is no time to generate enough Joule heating for damaging the triggering device. Thus, the triggering device can be used as the output transistor without sacrificing its HF characteristics. Since the output transistor can protect itself before the SCR turns on and can be protected when the SCR turns on, this protection scheme is called the SSP scheme.

Furthermore, the big differences between Figs. 7(c) and 8 are that there are high current densities (as the current flow lines) in the Fig. 7(c) NMOS transistor, but there are none in Fig. 8.

III. Experimental Result and Discussion

A. ESD Behavior of the SSP-ESD Device

In order to investigate the ESD behavior of the SSP-ESD device, a digital oscilloscope with a 500-MHz bandwidth and a 2 GSa/s sample rate is used to measure the voltage and current waveforms of the SSP-ESD device during a human-body-model (HBM) zapping event.

Fig. 9 shows the real-time I–t and V–t characteristics of the SSP-ESD device under the +100- and +200-V/V_{SS} HBM zapping events. For the HBM +100-V/V_{SS} zapping event, the current waveform sharply rises to its peak value $(100\ \mathrm{V}/1.5\ \mathrm{K}\Omega \cong 66\ \mathrm{mA})$, and then, it decays with a resistance–capacitance time constant (~150 ns). About the voltage waveform, there are two snapback regions. The first snapback (the voltage is about 4.5 V) occurs at the time from 20 to 80 ns; it comes from the turning on of the n-p-n bipolar transistor. The second snapback (the voltage is about 1.5 V) occurs after 80 ns; it comes from the turning on of the SCR. The above verifies that the n-p-n bipolar transistor can be turned on to clamp the pad voltage first, and then, the SCR can be triggered on for the SSP-ESD device during the ESD zapping event. However, for the + 200 V/V_{SS} HBM zapping event, there is only one snapback voltage (1.5 V) from the turning on of the SCR. This implies that the SCR can be triggered to the ON-state instantaneously if the zapping voltage is larger than +200 V.

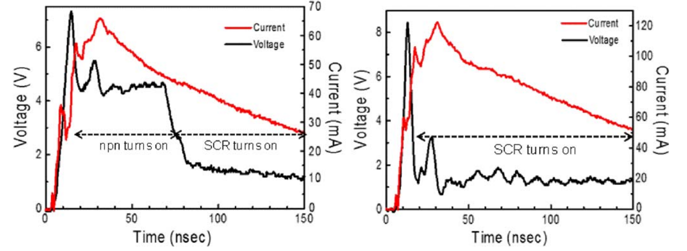

Fig. 9. Real-time I–t and V–t characteristics of the SSP-ESD device under (left picture) the +100 V/V_{SS} HBM zapping event and (right picture) the +200 V/V_{SS} HBM zapping event.

Before the snapback, the voltage rapidly rises until the device avalanche breakdown occurs at the drain junction of the triggering device in Fig. 9. Although the voltage can reach as high as 8 V, the transient of 8 V cannot damage the gate oxide because the gate-oxide transient endurance voltage is much larger than the gate-oxide direct-current (dc) endurance voltage in the 0.18-μm process [15]. This induces substrate-current generation. As the substrate current flows through the p-type substrate and raises the substrate voltage up to a value larger than 0.7 V, the source junction is forwarded to inject the electrons. Subsequently, the injected electrons diffuse through the base region and are collected by the collector [16]. The corresponding transit time is [17]

$$T_B = W_B^2/2D_B \tag{1}$$

where W_B is the base width and D_B is an electron diffusion constant.

It has been reported that the substrate potential is proportional to the ESD zapping voltage [18]. The higher the zapping ESD voltage is, the more the source junctions are forwarded. At a low zapping voltage, only the junction close to the poly gate, as shown in Fig. 7(a), is forwarded. Apparently, the spacing between the forwarded junction and the drain region of the triggering device is shorter than the spacing between the forwarded junction and the SCR's anode. Based on (1), the electrons will reach the drain region of the triggering device before arriving at the SCR's anode. This can explain why the n-p-n bipolar transistor can be turned on before the SCR turns on for the SSP-ESD device under the +100-V HBM zapping event, as shown in Fig. 9(a).

At a large zapping voltage, all source junctions are forwarded. The spacing between the forwarded junction and the drain region of the triggering device is almost equal to the

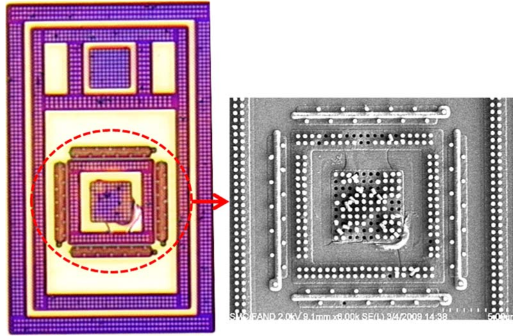

Fig. 10. SEM picture for the SSP-ESD device after the $+3.5$ kV/V_{SS} HBM zapping event.

spacing between the forwarded junction and the SCR's anode. From (1), the electrons can reach the drain region of the triggering device and the SCR's anode at the same time to turn on the triggering device and the SCR simultaneously. Subsequently, the SCR will become the major ESD current path, and only one snapback voltage V_{SB} can be observed in Fig. 9(b) since the SCR of the SSP-ESD device has smaller V_{SB} than n-p-n 1 V_{SB}.

Fig. 10 shows the scanning-electron-microscope (SEM) failure analysis result of the SSP-ESD device after the $+3.5$ kV/V_{SS} HBM zapping event. The failure regions are all located at the regions between the SCR's cathode and the SCR's anode. There are no failures in the triggering device. It is a very good proof that the triggering device of the SSP-ESD device can only be turned on before the SCR turns on and can be turned off after the SCR turns on. Since the triggering device only turns on in a short time, the time is too short to generate enough heat for damaging the triggering device.

B. I_{t2} and ESD Tests for the SSP-ESD Device

To gain a more detailed insight into the complex interaction between an ESD and the SSP-ESD device, a transmission-line-pulse (TLP) system and an ESD tester are used to evaluate the high-current I–V characteristics and the ESD performance of the SSP-ESD device, respectively. From the TLP measurement, discharge components for each stress mode can be identified.

In addition, the maximum current before the secondary breakdown I_{t2} can also be obtained for correlating to the threshold voltages of the HBM and the machine model (MM).

Fig. 11 shows the high-current I–V characteristics of the SSP-ESD device under the TLP stress events for four different kinds of stress modes. Except for the TLP/V_{SS} stress mode, all curves show the snapback phenomena. The device is at the OFF-state before the triggering voltage V_{t1}, and then, it is turned on and switches into the snapback regions after V_{t1}. Table I summarizes I_{t2} measured in Fig. 11 and the threshold voltages of the HBM and the MM. In Table I, the silicon data illustrate that I_{t2} is larger than 1.67 A, and HBM and MM threshold voltages can reach 3 kV and 150 V, respectively.

The black-square symbols in Fig. 11(a) and the red-triangle symbols in Fig. 11(b) illustrate the I–V curves of the SSP-ESD and PCL devices, respectively. The PCL device is a fully silicide n-MOSFET with a large total channel width, a staggered S/D contact, and a large contact-to-contact spacing

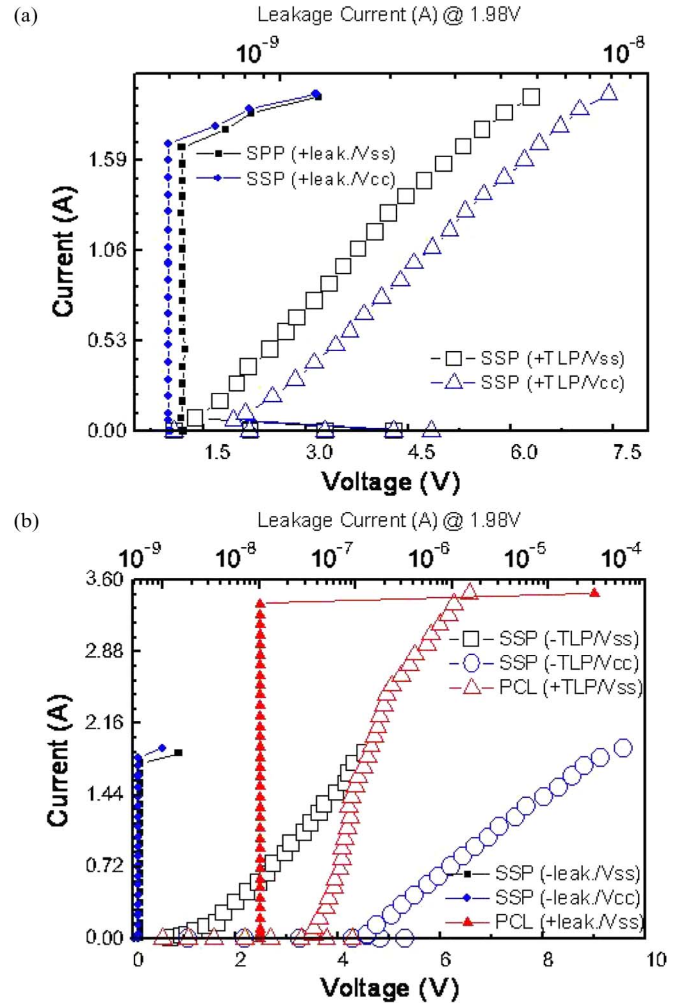

Fig. 11. High-current I–V characteristics of (a) the SSP-ESD device under $+$TLP/V_{SS} and $+$TLP/V_{CC}, (b) the SSP-ESD device under -TLP/V_{SS} and -TLP/V_{CC}, and the PCL device under $+$TLP/V_{SS}.

TABLE I
TLP AND ESD TEST RESULTS FOR THE SSP-ESD DEVICES

	+/Vss	+/Vcc	-/Vss	-/Vcc
TLP	I_{t2}: 1.67A V_{t1}: 4.3V	I_{t2}: 1.69A V_{t1}: 4.84V	I_{t2}: 1.86A V_{t1}: 0.8V	I_{t2}: 1.75A V_{t1}: 5.42V
ESD	HBM: 3kV MM: 150V	HBM: 3kV MM: 150V	HBM: 3.5kV MM: 150V	HBM: 3.5kV MM: 150V

[14]. The V_{t1} of the SSP-ESD device is nearly equal to the V_{t1} of the PCL device, but the snapback voltage V_{SB} is smaller than that of the PCL device. This shows that the triggering device and the SCR of the SSP-ESD device under this stress mode can be turned on in sequence.

The blue-triangle symbols in Fig. 11(a) illustrate the I–V curve of the SSP-ESD device under $+$TLP/V_{CC} stress mode; it is parallel to that of the SSP-ESD device under the $+$TLP/V_{SS} stress mode. Under the same stress current, the voltage difference for the two different stress modes is about 0.8–1 V, which is equal to one diode operation voltage. In Fig. 3, this voltage difference should result from the diodes between V_{SS} and V_{CC}. The diodes are the D2 between the two guard rings and the D3 of the PCL device. Excluding the diodes, the I–V curves of the SSP-ESD device under the two stress modes should

TABLE II
CRITICAL VOLTAGES FOR THE SSP-ESD DEVICES UNDER $-$TLP/V_{SS} AND $-$TLP/V_{CC}, AND PCL DEVICES UNDER THE $+$TLP/V_{SS} BASED ON THE MEASURED RESULTS IN FIG. 11(b)

	V_{t1} or V_T	V_{t1} or V_B	V_F
-SSP/V_{SS}	0.8V	0.97V	4.28V
+PCL/V_{SS}	4.39V	3.54V	4.51V
(-SSP/V_{SS})+(+PCL/V_{SS})	5.19V	4.51V	8.79V
-SSP/V_{CC}	5.42V	4.5V	8.82V

be identical. This verifies that the SSP-ESD device during the $+$ESD/V_{CC} zapping event uses the triggering device and the SCR as well as the diodes to discharge the ESD current, although there is no direct discharge component for this mode. This is why the I_{t2} values and the HBM and MM threshold voltages for the two different stress modes are almost the same, as shown in Table I.

The black-square symbols in Fig. 11(b) illustrate the I–V curves of the SSP-ESD device under $-$TLP/V_{SS} stress events; they present the typical I–V characteristics of a diode. It starts to turn on and rise exponentially if the applied voltage is larger than the diode turn-on threshold voltage V_T. This proves the discharge components for this stress mode including the NW/p-type substrate diode D0 and the parasitic diode D1 of the triggering device in Fig. 3. In Table I, the I_{t2} value and the HBM and MM threshold voltages for this mode are slightly larger than those of the $(+)$ PAD-V_{SS} mode.

The blue-circle symbols in Fig. 11(b) illustrate the I–V curve of the SSP-ESD device under the $-$TLP/V_{CC} stress mode. It presents the snapback phenomena. The voltages for this stress mode are larger than those of the PCL device under the $+$TLP/V_{SS} stress mode. Table II lists the critical voltages of the SSP-ESD device under the $-$TLP/V_{SS} and $-$TLP/V_{CC} stress modes and the PCL device under the $+$TLP/V_{SS} stress mode based on the measured results in Fig. 11(b). It can be found that the voltages of the SSP-ESD device under the $-$TLP/V_{CC} stress mode is almost equal to the summation voltage of the SSP-ESD device under the $-$TLP/V_{SS} stress mode and the PCL device under the $+$TLP/V_{SS} stress mode. This proves that the SSP-ESD device can use the PCL device and its diodes D0 and D1 to sink the current for this mode even if there is no direct ESD protection device for this zapping mode. In Fig. 11(b), the I_{t2} value of the PCL device is much larger than that of diodes D0 and D1 since the PCL device is a huge dimension device compared with the two diodes. Thus, diodes D0 and D1 of the SSP-ESD device will dominate ESD current paths for this zapping mode. This is why I_{t2} values and ESD threshold voltages of the SSP-ESD device for this mode are almost the same as those of the $(-)$ PAD-V_{SS} mode, as shown in Table I.

Furthermore, 1- and 3-ns very fast TLP stresses on $+$PCL/V_{SS} are also derived in Fig. 12. We can observed that V_{t1} increases and I_{t2} decreases when the TLP pulsewidth decreases. However, I_{t2} can reach 1.2 A even when the pulsewidth is only 1 ns. For the charge-device model, SSP devices can pass $+400$ and -450 V in the 48-pin dual in-line package and $+300$ and -350 V in the 208-pin quad flat package.

For shorter pulse durations, by definition, the averaging window is majorly decided by the nonquasi-static region of

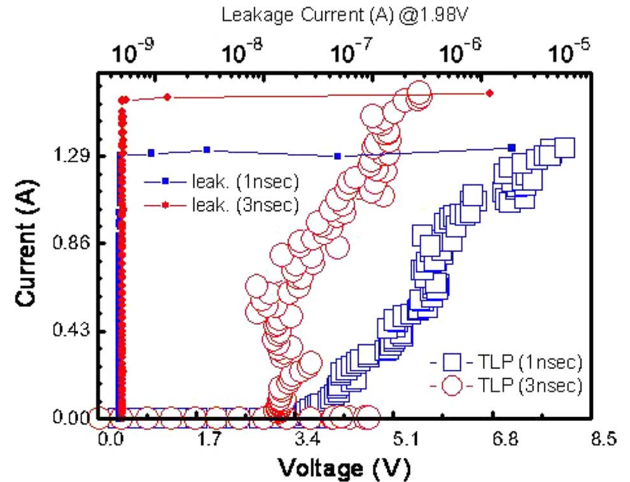

Fig. 12. 1- and 3-ns TLP results.

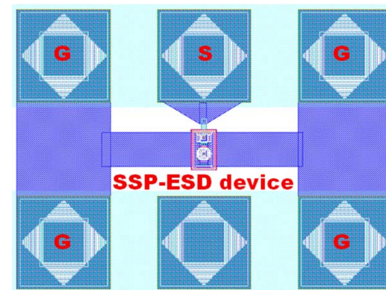

Fig. 13. Scattering-parameter pad set for capacitance measurements.

the pulses. Because, in that region, the SCR has not been fully triggered, the I–V curve will automatically shift toward higher voltages and lower currents.

C. Capacitance of the SSP-ESD Device

In order to extract the capacitance of the SSP-ESD device, a ground–signal–ground fixture, as shown in Fig. 13, is used as the interface of the SSP-ESD device and the probe tips for HF characteristic measurements. In addition, there are open/short fixtures to eliminate the influence of the transition region between the probe, the probe contact, and the SSP-ESD device. The apparatus to measure the capacitance of the SSP-ESD device is an HP-8510C network analyzer. The measured frequency is from 0.2 to 20 GHz, and the dc reversed-biased voltages are from 0 to 3.6 V.

The measured capacitance decreases as dc voltages and frequencies increase, as illustrated in Fig. 14. Under 0 V and 0.2 GHz, the capacitance value is only 76 fF, which differs from the simulation-program-with-IC-emphasis (SPICE)-simulated values of 78 and 2 fF.

From the SPICE simulations, the estimated capacitance values of the output transistor and the ESD protection devices are 47 and 31 fF, respectively. With such a low capacitance value, the ESD protection devices of the SSP-ESD device still effectively can protect the output transistor. The ESD robustness can reach the HBM in 3 kV and the MM in 150 V.

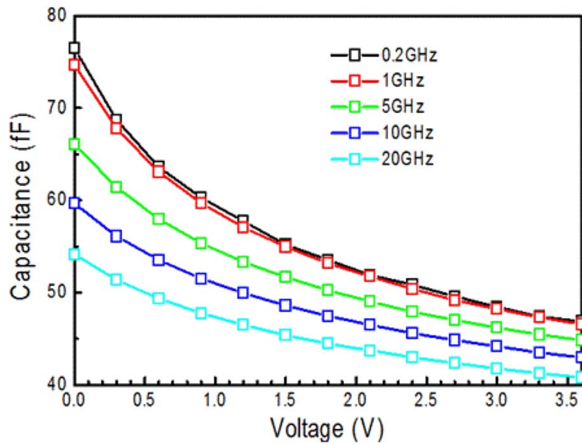

Fig. 14. Total capacitance values of the SSP-ESD device extracted from the HP-8510C network analyzer.

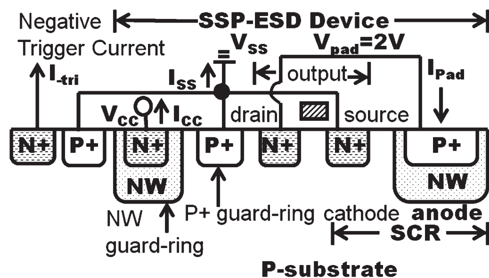

Fig. 15. Test structure and the bias condition for the negative latch-up immunity evaluation of the SSP-ESD device.

D. Latch-Up Immunity for the SSP-ESD Device

For a CMOS IC fabricated on the p-type substrate, the input–output circuits will not suffer the latch-up problem at the positive-charge triggering mode (i.e., the positive charge triggering the p-type substrate) if they are surrounded with a p+ guard ring. It is because the p+ guard ring can effectively suppress the local voltage rise of the p-well potential [19]. The worse case of the latch-up for most ICs is the negative triggering mode [19]. Fig. 15 shows the test structure and the bias condition of the SSP-ESD device for the negative latch-up immunity evaluation. Except for the SSP-ESD device, there are negative triggering node n+ diffusion and grounded p+ diffusion to separate the SSP-ESD device and the negative triggering node. During the negative triggering event, a constant voltage of 2 V is applied to the SCR anode and the drain region of the output transistor. In addition, a negative triggering current is applied to the negative trigger node.

In Fig. 16, I_{Pad}, I_{CC}, and I_{SS} are the currents for pad, power V_{CC}, and ground V_{SS}, respectively. The pad voltage is marked in V_{Pad}. If the NW guard ring is floating, the negative triggering current $I_{-\mathrm{tri}}$ can easily drive SSP devices into the latch-up state at 125°C, as shown in Fig. 16(a). I_{Pad} and V_{Pad} can be kept at 0 A and 2 V when the absolute $I_{-\mathrm{tri}}$ is below 30 mA. As absolute $I_{-\mathrm{tri}}$ increases, I_{Pad} jumps from 0 to the clamped current (100 mA), and V_{Pad} falls from 2 to 1.35 V due to the latch-up occurrence. However, there is no latch-up occurrence on the SSP-ESD device at 125 °C if the NW guard ring connects to 2 V, as shown in Fig. 16(b). Even if absolute $I_{-\mathrm{tri}}$ ramps up

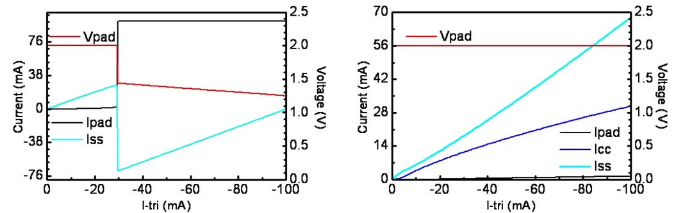

Fig. 16. SSP-ESD device during the negative triggering event when (left) the NW guard ring is floating, and (right) the NW guard ring connects to 2 V.

to 100 mA, V_{Pad} still can be kept at a constant voltage of 2 V. In addition, I_{Pad} is still quite low (< 2 mA) since most $I_{-\mathrm{tri}}$ currents flow to the p+ and NW guard rings. The two guard rings can prevent the current flowing into the SSP-ESD device; therefore, the SCR does not enter the latch-up state. This is why the SSP-ESD device not only has the p+ guard ring but also has the NW guard ring. Except the latch-up prevention, the two guard rings are also important for ESD protection. With the two guard rings, the SSP-ESD device can provide a discharge current path for all ESD modes.

IV. Conclusion

An SSP scheme is developed and demonstrated to protect the output transistor against ESD damage for Gigahertz ICs. Unlike a self-protection scheme, the output transistor does not need the ballast drain resistor. Unlike the nonself-protection scheme, it does not need the triggering device and any passive component since the output transistor is the triggering device.

Traditionally, the output transistor can turn on and share the ESD current with the ESD device during the whole stress period of the ESD zapping event. Thus, the output transistor should be designed with special layout rules to protect ICs from the ESD damage. This paper has placed the drain region of the output transistor far away from the ESD device; thus, the output transistor can turn off after the ESD device turns on.

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