Symmetric Vertical-Channel Nickel-Salicided Poly-Si Thin-Film Transistors With Self-Aligned Oxide Overetching Structures

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***Abstract*—This paper reports the impacts of NH_3 plasma treatment time, oxide overetching depth, and gate oxide thickness on symmetric vertical-channel Ni-salicided poly-Si thin-film transistors (VSA-TFTs) for the first time. OFF-state currents may be improved by increasing the oxide overetching depth. The ON/OFF current ratio may be also improved by increasing the oxide overetching depth. The NH_3 plasma optimum treatment time of VSA-TFTs is significantly shorter than that of conventional top-gate horizontal-channel TFTs. The performance of VSA-TFTs is degraded by NH_3 plasma treatment for too long a time. VSA-TFTs with 15-nm gate oxide thickness display better subthreshold swing (< 150 mV/dec) than VSA-TFTs with 30-nm gate oxide thickness. OFF-state currents can be improved by increasing L_{mask}, even when the oxide overetching depth and the gate oxide thickness are changed.**

***Index Terms*—NH_3 plasma treatment, Ni-salicided, oxide overetching depth, polycrystalline-silicon thin-film transistors (poly-Si TFTs), vertical channel, vertical-channel Ni-salicided poly-Si TFTs (VSA-TFTs).**

I. Introduction

RECENTLY, polycrystalline-silicon thin-film transistors (poly-Si TFTs) have attracted considerable attention because of their diversity of applications, including nanowire transistor, nonvolatile memory, and 3-D circuit integration [1]–[7]. One effective approach to obtaining high-performance poly-Si TFTs and enhancing device density is to scale down the channel length. However, it is difficult to reduce channel length due to the limits of photolithography resolution. Therefore, vertical-channel thin-film transistors (VTFTs) have been widely researched and developed to overcome the limits of photolithography [8]–[10]. In these previous works, VTFTs have shown great potential for 3-D integration since the channel lengths are determined by the thicknesses of the poly-Si or silicon-dioxide film, instead of photolithographic process limitations. However, these works using asymmetric source/drain (S/D) have encountered circuit design difficulties. S/D parasitic series resistance and contact resistance remain problems for device scaling and reduce device performance.

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Conventional top-gate poly-Si TFTs suffer from large OFF-state leakage currents due to their high electric field in the drain depletion region, which results in field emission via grain boundary traps [11], [12]. In order to reduce the leakage currents, a variety of methods have been proposed to reduce the electric field near the drain region, including the lightly doped drain, field-induced drain, high-k spacer offset-gated structure, and Si/Ge T-Gate structure [13]–[17]. Nevertheless, those structures require additional masks or extra materials (HfO_2, Ge), complicating fabrication processes.

It is well known that the numerous grain boundaries and intragranular defects in poly-Si channel film result in the degradation of poly-Si TFT performance. To achieve high-performance poly-Si TFTs, it is necessary to reduce the defects in the poly-Si channel film. Hence, many plasma treatment methods are used to passivate the defects in the poly-Si channel film, including H_2, O_2, N_2, and NH_3 plasmas [18]–[24]. Based on the literatures, the NH_3 plasma treatment offers better performance enhancement, hot-carrier stress endurance, and thermal stability than other plasma treatment methods.

In our previous work, the VSA-TFTs have been successfully fabricated and demonstrated [25]. The parasitic series resistance of S/D and the floating n^+ region may be significantly reduced by Ni-salicidation, resulting in improved ON-state currents. The ON-state currents will not be limited by the parasitic series resistance of S/D and the floating n^+ region when the gate bias is increased. The OFF-state currents can be improved by modifying the oxide overetching, the equivalent dual-gate structure, and the floating n^+ region length without additional masks. The performance can be improved by increasing the NH_3 plasma treatment time in the conventional top-gate horizontal-channel TFTs [23], [24].

However, the effects of NH_3 plasma treatment time on the VSA-TFTs were not investigated in our previous work. In this paper, the n^+ S/D and floating n^+ region of VSA-TFTs were fully Ni-salicided. We study the effects of NH_3 plasma treatment time, oxide overetching depth, and gate oxide thickness on the VSA-TFTs with self-aligned oxide overetching structures for the first time.

II. Experiment

Fig. 1 shows a schematic cross-sectional diagram of VSA-TFTs with 30-nm gate oxide thickness, 50-nm channel thickness, and oxide overetching depths of about (a) 40, (b) 80,

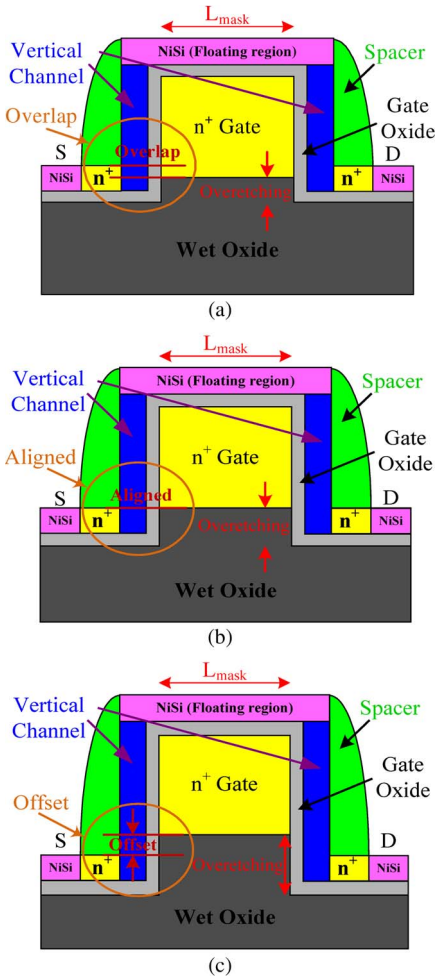

Fig. 1. Schematic cross-sectional diagram of VSA-TFTs with 30-nm gate oxide thickness, 50-nm channel thickness, and oxide overetching depths of about (a) 40, (b) 80, and (c) 120 nm.

and (c) 120 nm. In Fig. 1(a), VSA-TFTs with 40-nm oxide overetching depth showing a roughly 40-nm overlap region between the gate and S/D n^+ edges are designated "overlap VSA-TFTs." VSA-TFTs with 80-nm oxide overetching depth showing an aligned gate and S/D n^+ edges are designated "alignment VSA-TFTs" [see Fig. 1(b)]. VSA-TFTs with 120-nm oxide overetching depth showing a roughly 40-nm offset region between the gate and S/D n^+ edges are designated "offset VSA-TFTs" [see Fig. 1(c)]. Furthermore, VSA-TFTs with 15-nm gate oxide thickness, 50-nm channel thickness, and 80-nm oxide overetching depth are designated "GO-15-nm VSA-TFTs." The GO-15-nm VSA-TFTs also have a 15-nm offset region between the gate and S/D n^+ edges. Conventional top-gate horizontal-channel devices with a gate oxide of 15 nm, a self-aligned n^+ S/D, and Ni-salicided processes were also fabricated to serve as controls. Finally, all the devices were fabricated using NH_3 plasma treatment (NH_3 plasma treatment times will be discussed in Section III). The key processes of VSA-TFTs were discussed in detail in our previous work [25]. We fabricated all devices under identical process conditions, and all process temperatures were below 700 °C.

Fig. 2 shows the cross-sectional transmission electron microscope (TEM) microphotograph of the offset VSA-TFTs with fully Ni-salicided n^+ S/D and an floating n^+ region. In the

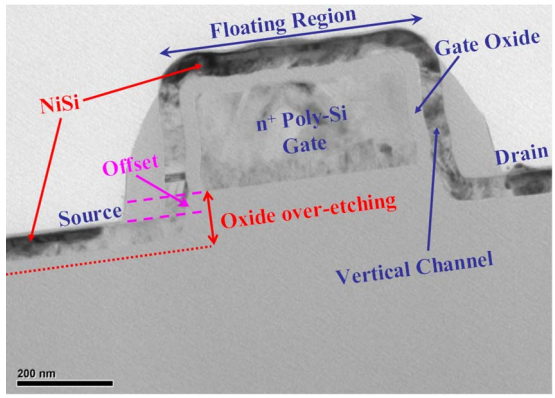

Fig. 2. Cross-sectional TEM microphotograph of offset VSA-TFTs with fully Ni-salicided n^+ S/D and a floating n^+ region.

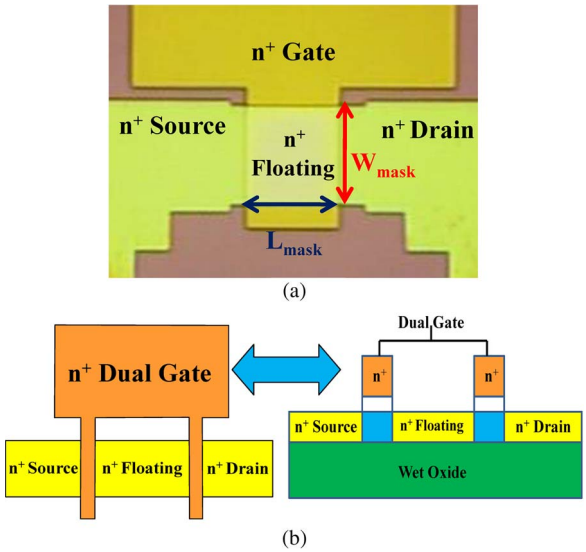

Fig. 3. (a) Top-view optical microscope microphotograph of VSA-TFTs without Ni-salicidation and (b) effective dual-gate structure of VSA-TFTs.

VSA-TFTs, the poly-Si thickness in the channel is 50-nm, and the effective channel length $L_{\rm eff}$ is defined by 2× the total thickness of the poly-Si gate (about 200 nm). The offset between gate and S/D n^+ edges was achieved by modifying wet oxide over etching resulting in about 40-nm offset region. Fig. 3 displays the top-view optical microscope microphotograph of VSA-TFTs without Ni-salicidation and effective dual gate structure of VSA-TFTs. The VSA-TFTs inherently own an effective dual gate structure. The length of floating n^+ region is defined by mask channel length $L_{\rm mask}$, whereas the mask channel width $W_{\rm mask}$ is equal to the effective channel width [see Fig. 3(a)]. The equivalent dual-gate structure [see Fig. 3(b)] can moderate the lateral electrical field in the drain depletion region, significantly reducing leakage currents and increasing the ON/OFF current ratio [26], [27].

III. Results and Discussion

Fig. 4 displays the transfer characteristics of the VSA-TFTs with different NH_3 plasma treatment times, along with an enlarged ON-state currents graph of the VSA-TFTs with different NH_3 plasma treatment times. VSA-TFTs fabricated with a 10-min NH_3 plasma treatment time have lower OFF-state

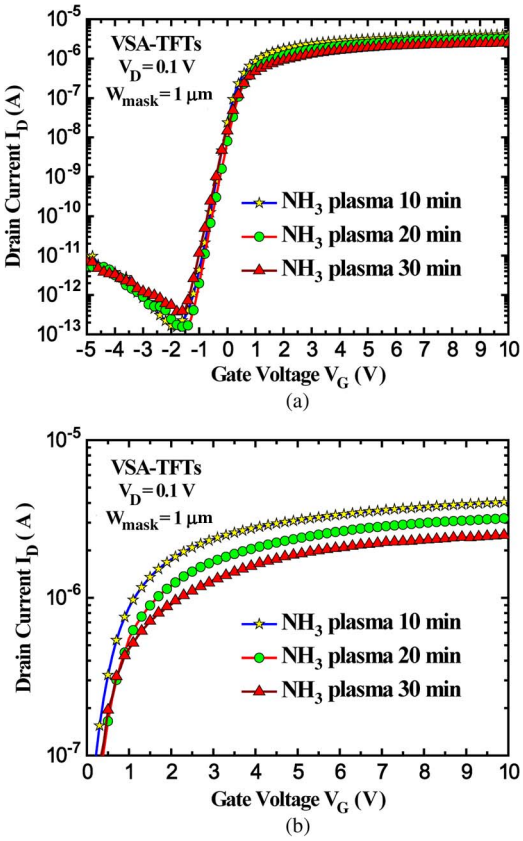

Fig. 4. (a) Transfer characteristics and (b) enlarged ON-state currents graph of the VSA-TFTs with different NH_3 plasma treatment times.

currents (defined as the minimum drain currents) and higher ON-state currents than VSA-TFTs fabricated with other NH_3 plasma treatment times. This is attributed to the hydrogen passivation of the defect states, the nitrogen pileup at the SiO_2/poly-Si interface, and the strong Si–N bond formation that terminates the dangling bonds in the grains and at the grain boundaries in the channel region [23], [24]. Because the poly-Si channels are deposited after the gate oxide in VSA-TFTs, the exposed poly-Si channels are easily damaged under too long NH_3 plasma treatment time, resulting in poor electric characteristics. The mechanisms of the damage to the gate oxide integrity and the SiO_2/poly-Si interface during long NH_3 treatment times include electrostatic charging damages [28]. Therefore, we believe that NH_3 plasma treatment time of 10 min is the optimum condition for the VSA-TFTs in this independent experiment.

By the same token, the hidden poly-Si channels under the top gate in conventional devices require longer NH_3 plasma treatment times to achieve improved characteristics [23], [24]. We used 30-min NH_3 plasma treatment times to passivate the conventional top-gate horizontal-channel TFTs. The NH_3 plasma optimum treatment time of VSA-TFTs is significantly shorter than that of conventional top-gate horizontal-channel TFTs.

Fig. 5 shows the transfer characteristics and the ON-state current distribution of overlap VSA-TFTs with $W_{\mathrm{mask}} = 1\ \mu$m and different L_{mask}. The OFF-state currents can be improved by increasing the L_{mask}. This may be attributed to the mitigation of the OFF-state peak lateral electric field in the drain depletion region [25]. In Fig. 5(b), the ON-state currents are degreased with increasing L_{mask}. The ON-state currents can be main-

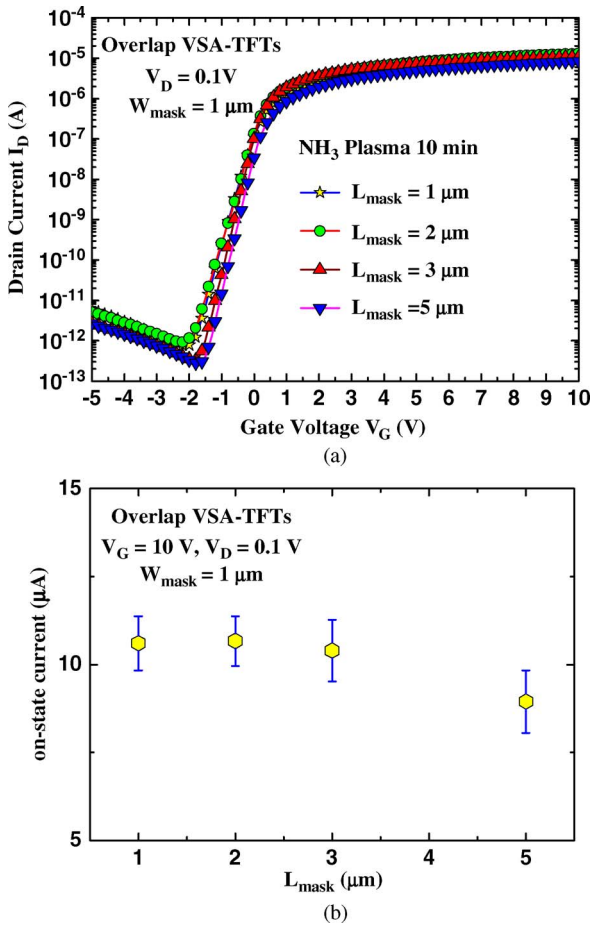

Fig. 5. (a) Transfer characteristics and (b) ON-state current distribution of overlap VSA-TFTs with $W_{\mathrm{mask}} = 1\ \mu$m and different L_{mask}.

tained at approximately the same value from $L_{\mathrm{mask}} = 1\ \mu$m to $L_{\mathrm{mask}} = 2\ \mu$m due to the Ni-silicidation in the floating n^+ region. However, the ON-state currents are slightly degraded when $L_{\mathrm{mask}} = 3\ \mu$m and significantly degraded when $L_{\mathrm{mask}} = 5\ \mu$m. This result is consistent with Fig. 5(a). The series resistance in the floating n^+ region rises with increasing L_{mask}, and therefore, L_{mask} may not be indefinitely increased.

We believe that the value of a subthreshold swing (S.S.) may indicate the gate control ability in the channel. It is easier to lose the gate control ability in shorter channel devices, resulting in degradation of the S.S. The VSA-TFTs with small L_{mask} have shorter effective channel lengths than the VSA-TFTs with large L_{mask}, and thus have more serious short-channel effects. VSA-TFTs with large L_{mask} can suppress the short-channel effect resulting in improved S.S. The overlap VSA-TFTs with $L_{\mathrm{mask}} = 3\ \mu$m have good S.S. (S.S. = 292 mV/dec) and the largest ON/OFF current ratio. Accordingly, the optimum value of L_{mask} is 3 μm in this paper.

Fig. 6 exhibits the transfer characteristics and the enlarged ON-state currents graph of VSA-TFTs with $W_{\mathrm{mask}}/L_{\mathrm{mask}} = 1\ \mu\mathrm{m}/3\ \mu$m and various oxide overetching depths. The OFF-state currents can be improved by increasing the oxide overetching depth. The electric field in the drain depletion region may be diminished as a result of increasing the offset region between the gate and the S/D n^+ edges [13]–[17]. However, the ON-state currents will be reduced by increasing

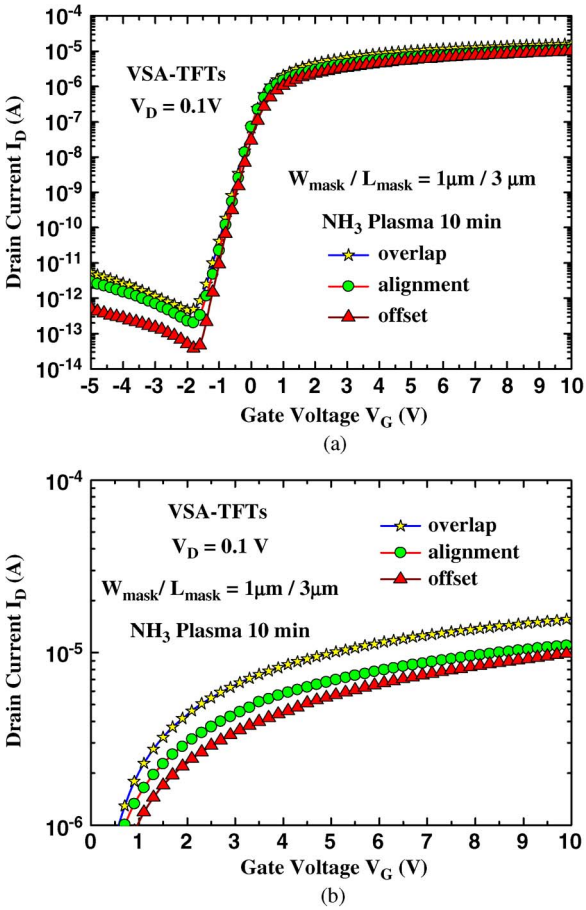

Fig. 6. (a) Transfer characteristics and (b) enlarged ON-state currents graph of the VSA-TFTs with $W_{\mathrm{mask}}/L_{\mathrm{mask}} = 1\ \mu\mathrm{m}/3\mu\mathrm{m}$ and various oxide overetching depths.

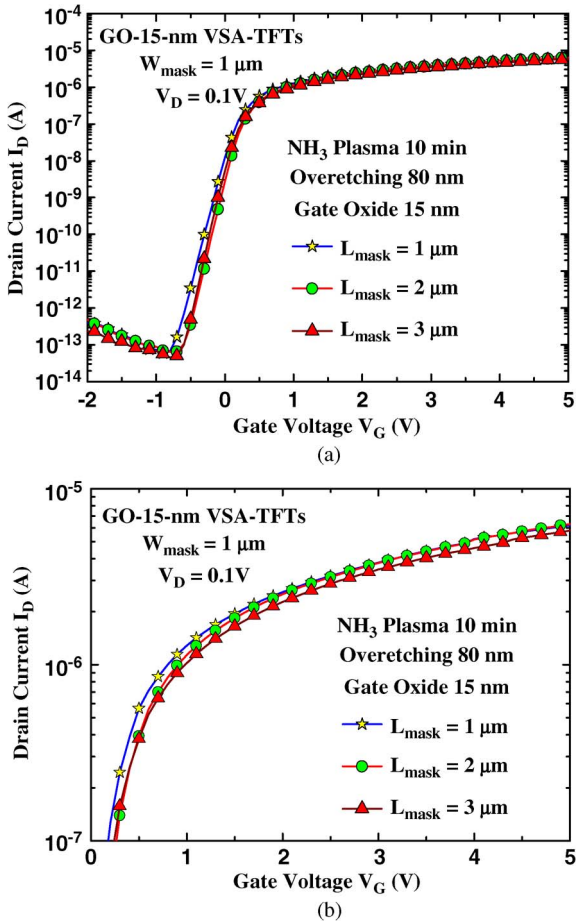

Fig. 7. (a) Transfer characteristics and (b) enlarged ON-state currents graph of the GO-15-nm VSA-TFTs with $W_{\mathrm{mask}} = 1\ \mu\mathrm{m}$ and different L_{mask}.

the oxide overetching depth [see Fig. 6(b)]. The overlap VSA-TFTs have higher ON-state current than the alignment and offset VSA-TFTs due to shorter effective channel length. The offset VSA-TFTs have the lowest ON-state currents, caused by the series resistance in the offset region. The offset VSA-TFTs can suppress the short-channel effect, resulting in improved S.S. Although the ON-state currents of offset VSA-TFTs are slightly smaller than the others, the offset VSA-TFTs display an obvious improvement in the OFF-state currents resulting in the largest ON/OFF current ratio, exceeding 10^8.

Fig. 7 shows the transfer characteristics and the enlarged ON-state currents graph of the GO-15-nm VSA-TFTs with $W_{\mathrm{mask}} = 1\ \mu\mathrm{m}$ and different L_{mask}. The OFF-state currents can be improved by increasing the L_{mask}, and the ON-state currents are nearly identical. The enlarged ON-state currents graph shows that the ON-state currents of the various L_{mask} are different. However, the difference in the ON-state currents for the various L_{mask} is very small. Hence, the ON-state currents can be maintained at the same level from the $L_{\mathrm{mask}} = 1\ \mu\mathrm{m}$ to the $L_{\mathrm{mask}} = 3\ \mu\mathrm{m}$. These results are consistent with Fig. 5 and our previous work, implying that VSA-TFTs can improve the OFF-state currents by increasing L_{mask}, even though the thermal oxide overetching depth and the gate oxide thickness are changed. Moreover, the S.S. of the GO-15-nm VSA-TFTs with $L_{\mathrm{mask}} = 1\ \mu\mathrm{m}$ is 144 mV/dec, the S.S. of the GO-15-nm VSA-TFTs with $L_{\mathrm{mask}} = 2\ \mu\mathrm{m}$ is 130 mV/dec, and the S.S. of the GO-15-nm VSA-TFTs with $L_{\mathrm{mask}} = 3\ \mu\mathrm{m}$ is 127 mV/dec. The GO-15-nm VSA-TFTs with $L_{\mathrm{mask}} = 1\ \mu\mathrm{m}$ have shorter effective channel lengths and more serious short-channel effects than the others, resulting in degradation of S.S. The S.S. of the GO-15-nm VSA-TFTs is better than that of the offset VSA-TFTs (the S.S. of the offset VSA-TFT with $L_{\mathrm{mask}} = 3\ \mu\mathrm{m}$ is 269 mV/dec). In other words, the GO-15-nm VSA-TFTs have better gate control ability than the offset VSA-TFTs due to their thinner gate oxide thickness. Therefore, the S.S. in the VSA-TFTs can be improved by decreasing the gate oxide thickness.

Fig. 8 displays the transfer characteristics of GO-15-nm VSA-TFTs and offset VSA-TFTs with $W_{\mathrm{mask}}/L_{\mathrm{mask}} = 1\ \mu\mathrm{m}/3\mu\mathrm{m}$. The transfer characteristics of conventional TFTs with $W_{\mathrm{mask}}/L_{\mathrm{mask}} = 1\ \mu\mathrm{m}/0.4\ \mu\mathrm{m}$ are also shown for comparison. It is obvious that the GO-15-nm VSA-TFTs and the offset VSA-TFTs outperform conventional TFTs. The conventional TFTs have slightly higher ON-state currents only in the high gate voltage due to their shorter effective channel length.

Several important parameters of GO-15-nm VSA-TFTs, offset VSA-TFTs, and conventional top-gate horizontal-channel TFTs are listed in Table I. I_{on} is defined as the drain current at $V_G = 5$ V and $V_D = 0.1$ V, whereas I_{off} is defined as the minimum drain current at $V_D = 0.1$ V. In Table I, the field-effect mobility of GO-15-nm VSA-TFTs is smaller than that of the offset VSA-TFTs. We believe that the vertical electric field of the channels in the GO-15-nm VSA-TFTs is

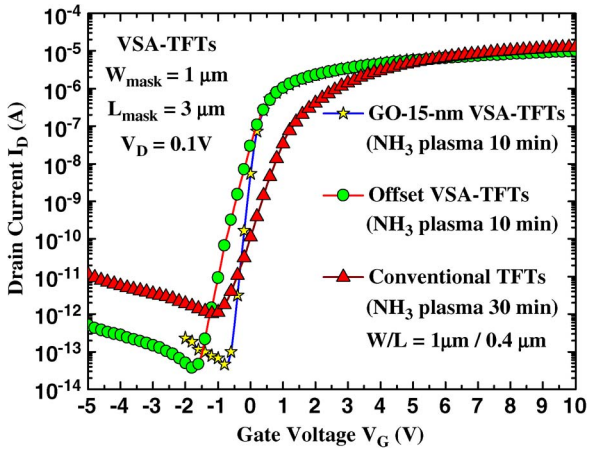

Fig. 8. Transfer characteristics of GO-15-nm VSA-TFTs and offset VSA-TFTs with $W_{\mathrm{mask}}/L_{\mathrm{mask}} = 1\ \mu\mathrm{m}/3\mu\mathrm{m}$. Transfer characteristics of conventional TFTs with $W_{\mathrm{mask}}/L_{\mathrm{mask}} = 1\ \mu\mathrm{m}/0.4\ \mu\mathrm{m}$ are also shown for comparison.

TABLE I
SELECTED IMPORTANT PARAMETERS OF GO-15-nm VSA-TFTs, OFFSET VSA-TFTs, AND CONVENTIONAL TOP-GATE HORIZONTAL-CHANNEL TFTs

	S.S (mV/dec)	Mobility ($cm^2/V{\cdot}s$)	I_{off} (pA)	I_{on} (uA)	on/off ratio
GO-15-nm VSA-TFTs	127	50	0.05	5.76	$>10^8$
Offset VSA-TFTs	269	67	0.04	5.59	$>10^8$
Conventional TFTs	399	29	1.04	4.83	3.8×10^6

higher than that of the offset VSA-TFTs due to their thinner gate oxide thickness resulting in more serious carrier scattering and degraded drain current. Therefore, the drain ON-state currents of GO-15-nm VSA-TFTs are not much higher than that of the offset VSA-TFTs. The VSA-TFTs have higher mobility, lower OFF-state current, and better S.S. than conventional TFTs. It appears that the OFF-state currents of the GO-15-nm VSA-TFTs could be further improved by employing an optimum oxide overetching depth.

IV. CONCLUSION

In this paper, we have investigated the effects of NH_3 plasma treatment time, oxide overetching depth, and gate oxide thickness on VSA-TFTs. VSA-TFTs with 10-min NH_3 plasma treatment time have lower OFF-state currents and higher ON-state currents than VSA-TFTs with longer NH_3 plasma treatment times. The OFF-state currents and ON/OFF current ratio may be improved by increasing the oxide overetching depth. The S.S. can be improved by decreasing the gate oxide thickness; the S.S. of GO-15-nm VSA-TFTs is less than 150 mV/dec. The OFF-state currents can be improved by increasing the L_{mask}, even though the thermal oxide overetching depth and the gate oxide thickness are changed. Compared with the conventional top-gate horizontal-channel TFTs, the VSA-TFTs have better characteristics in S.S., ON/OFF current ratio, and field-effect mobility.

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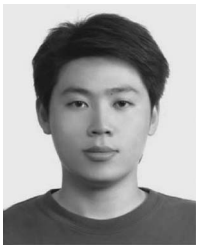

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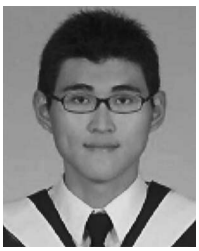

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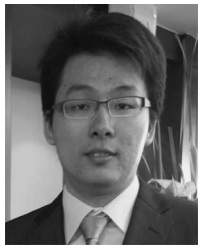

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